

# Advanced electron-beam lithography for 0.5- $\mu\text{m}$ to 0.25- $\mu\text{m}$ device fabrication

by F. J. Hohn  
A. D. Wilson  
P. Coane

High-resolution lithographic capability is required for the fabrication of fully scaled semiconductor devices at minimum dimensions of 0.5  $\mu\text{m}$  to 0.25  $\mu\text{m}$ —the prototype for the semiconductor logic and memory CMOS devices of the 1990s. Electron-beam exposure tools provide this capability. Fully scaled 0.5- $\mu\text{m}$  test devices were fabricated using a modified EL-3 variable shaped-electron-beam system, while 0.25- $\mu\text{m}$  ground-rule lithography was accomplished with a Gaussian round-electron-beam Vector Scan system. An important part of this technology is the selection of lithographic resist system and the process used for pattern definition and transfer. Twelve or more lithographic steps are often needed for circuit devices with the above minimum dimensions. For fully scaled applications, each one of these pattern levels must be defined by electron-beam lithography, and each level may require a

specific lithographic resist. Thus, the electron-beam system and the resist process must be mutually compatible if the required resolution, feature size control, and pattern-level-to-pattern-level overlay accuracy are to be achieved. This paper discusses the successful integration of e-beam lithography and resist technologies and their application to CMOS device fabrication.

## Introduction

Progress in the fabrication of prototype high-density VLSI semiconductor devices has been achieved through the use of electron-beam (e-beam) lithography. Its application to small-structure patterning has resulted in a systematic reduction of minimum feature size and a corresponding increase in the circuit density needed for future memory and logic chips.

For complex circuits twelve or more lithography steps are required. Each successive level must be accurately patterned and precisely overlaid with respect to previously defined patterns. The ability of control pattern definition and overlay is critical to device performance, and is a direct function of the overall e-beam writing accuracy. Table 1 shows how linewidth control and pattern overlay precision become more stringent as minimum dimensions are reduced.

Table 1 indicates that as the minimum feature size decreases there are corresponding increases required in the precision of the linewidth and overlay of the pattern levels.

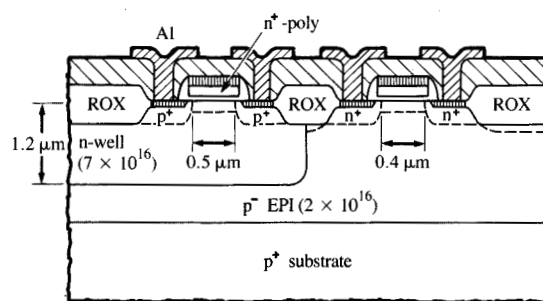
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In general, the feature size control should equal about 20% of the minimum feature size (mfs) and the level-to-level overlay accuracy must be better than 25% of the mfs. This is part of the convention for "fully scaled" devices, where all dimensions and tolerances shrink accordingly. For fully scaled minimum features of  $25\text{ }\mu\text{m}$ , the minimum feature in the  $x$  and  $y$  dimensions shrinks to this dimension (e.g., contact holes), the linewidth control limit is  $0.05\text{ }\mu\text{m}$  ( $500\text{ }\text{\AA}$ ), and the overlay must be within  $0.06\text{ }\mu\text{m}$  ( $600\text{ }\text{\AA}$ ). Therefore, as feature sizes decrease, the fully scaled convention imposes upon e-beam lithography systems further improvement and refinement of e-beam stability, pattern placement, etc.

### Advanced e-beam lithography

The Gaussian round-beam and the variable shaped-beam systems are the two e-beam systems that have been used to make the devices. Since both probe-forming concepts have been extensively described [1-4], only the major performance parameters are presented as background material in this discussion of the fabrication of fully scaled  $0.5\text{-}\mu\text{m}$  CMOS devices and  $0.25\text{-}\mu\text{m}$  NMOS and PMOS devices.

The Gaussian round e-beam system is of the "Vector Scan" design in which the beam is positioned (vector-deflected) directly to the exposure location, and the pattern to be exposed and defined is then completed in a raster-scan fashion. After completion of this pattern, the e-beam is positioned at the beginning of the next pattern, which is also completed in raster-scan mode. This procedure continues sequentially for all patterns. The e-beam system uses a lanthanum hexaboride single-crystal thermionic electron emitter with a three-lens demagnifying configuration with a pre-lens magnetic double deflection, and operates at a beam energy of  $25\text{ keV}$ . The probe size, set by adjusting lens parameters, is typically set to one quarter of the pattern minimum linewidth requirement. Total current density at the cathode is in the range of  $50\text{ to }100\text{ A/cm}^2$ . In order to achieve accuracy and resolution over a typical VLSI chip measuring  $10 \times 10\text{ mm}$ , the chip is patterned by writing a stitched array of  $0.8 \times 0.8\text{-mm}$  subfields. This implies that the actual subfield within which the beam is vector-addressed and exposed is  $0.8 \times 0.8\text{ mm}$  in size. In order to fabricate large chips, a matrix consisting of many of these fields is stitched together. An  $x$ - $y$  stage moves the position of the wafer from subfield to subfield. The  $x$ - $y$  table position is tracked and measured by a laser interferometer and the e-beam position adjusted to maintain placement accuracy of each pattern element. In the Gaussian round-beam system, the sequential exposure of single pixels at a relatively low probe current results in a limited throughput. For this reason, the total number of fabricated chips per wafer is necessarily limited in order to reduce writing time to acceptable levels.



**Figure 1**

Schematic cross section of a CMOS device showing the levels of lithography. The features are not drawn to scale.

**Table 1** Pattern dimensions vs. linewidth control and overlay.

| Minimum feature size ( $\mu\text{m}$ ) | Linewidth control (20% mfs) ( $\mu\text{m}$ ) | Critical level overlay (25% mfs) ( $\mu\text{m}$ ) |
|----------------------------------------|-----------------------------------------------|----------------------------------------------------|
| 1.0                                    | 0.2                                           | 0.25                                               |
| 0.5                                    | 0.1                                           | 0.13                                               |
| 0.25                                   | 0.05                                          | 0.06                                               |
| 0.1                                    | 0.02                                          | 0.025                                              |

The variable shaped-beam system EL-3 [3] is an advanced EL-3 system which was modified for  $0.5\text{-}\mu\text{m}$  ground-rule lithography. This system was used to fabricate fully scaled CMOS devices. A schematic cross section of a CMOS device is shown in Figure 1.

The Vector Scan and EL-3 lithography tools have the capability for  $0.5\text{-}\mu\text{m}$  ground-rule device fabrication. A further refined Vector Scan system has successfully demonstrated  $0.25\text{-}\mu\text{m}$  device capabilities.

### Electron-beam tool and process characteristics

A thorough understanding of all the parameters that influence the accuracy of the pattern definition and transfer process has become increasingly critical to the successful fabrication of VLSI chips. Sources of error which affect the accuracy of electron-beam lithography are manifold, some being specific to electron-beam systems while others are of a more general nature. These error sources must be thoroughly understood and controlled as dimensions continue to be reduced. The more common sources of error are attributed

to 1) electron beam/electron optics, 2) overall system thermal stability, 3) magnetic environment interaction, 4) electron beam/resist/substrate interaction, and 5) resist system/process control.

Each of these parameters is important, and each one could be the limiting factor determining ultimate system performance. Not all of these error sources are completely independent of the others. Compromises in system performance may be necessary. For example, when the beam energy increases, the resolution of the system will usually improve; the electron beam becomes "stiffer," reducing the potential for perturbation of the e-beam by environmental conditions. Both of these factors contribute to an improvement in resolution. However, accurate pattern element definition in resist, especially at high pattern density, is also limited by the well-known proximity effect [5-7]; i.e., adjacent areas not directly exposed to the incident e-beam receive partial exposure from backscattered electrons. The proximity effect is particularly severe for dense patterns with dimensions and spacings of  $1\text{ }\mu\text{m}$  or less. Numerical approximations of this effect are included in the software of the e-beam exposure system, which controls the exposure and assigns the required dose to all shapes.

Figure 2 shows cross sections of resist patterns as they were exposed with and without proximity correction. The images were taken with a scanning electron microscope with the sample tilted at a  $30^\circ$  angle (tilted up with respect to the bottom of the figure). In these micrographs, the bright area is the resist surface, while the dark area is the cross section of the resist. Test patterns were exposed on both Vector Scan and EL-3 systems; the examples shown in Figure 2 are from an EL-3 system. Figure 2(a) shows isolated lines and a spaced line array, without proximity correction, while Figure 2(b) shows the same patterns with proximity correction. The nominal linewidth is  $0.5\text{ }\mu\text{m}$ . The base dose was adjusted such that the isolated lines [the uppermost row in Figures 2(a) and (b)] developed to the nominal dimensions. The same exact dose was provided for exposure of the line-space array and the isolated line in the middle and bottom rows, respectively, of Figure 2(a). Since less overall area is exposed here, the contributing backscatter exposure is less, and the overall exposure dose is insufficient to completely develop the line-space array. For the isolated line—bottom micrograph—almost no development occurred. Algorithms, which were derived for exposure control so that each pattern receives the correct exposure dose regardless of geometrical differences, are resident in the software of the e-beam control systems. As can be seen in Figure 2(b), with these algorithms it is possible to develop the three patterns of Figure 2(a) to their nominal dimensions.

The energy of the incident e-beam also has a profound effect upon the range of the proximity effect. This is discussed by Broers [6] in this issue of the *IBM Journal of Research and Development*.

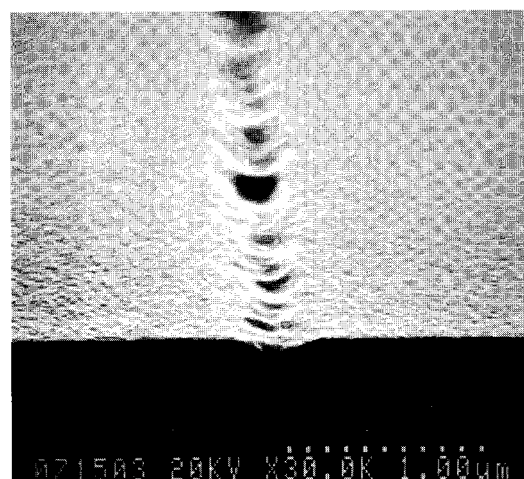
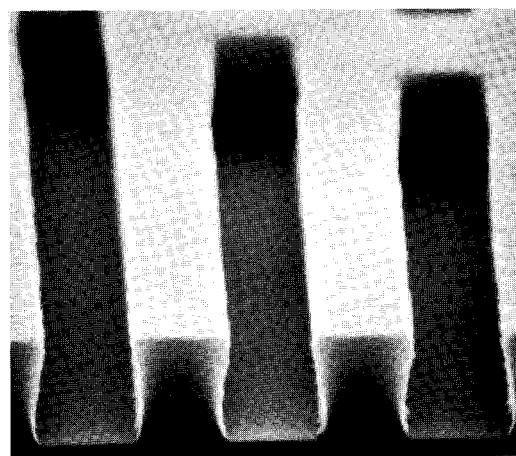
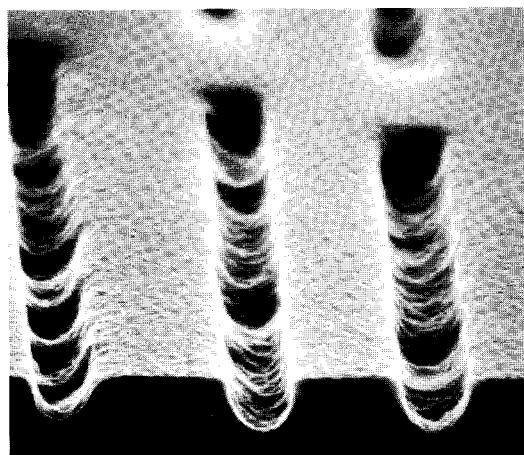
Similar to the proximity effect is the influence of electron-beam probe size (measured as the width at half maximum of an e-beam with a Gaussian distribution of beam current density and as the edge slope definition [8] for a shaped e-beam) on exposed resist profiles. As shown in the scanning electron micrographs of Figure 3 for single-line exposures, the beam size has an effect upon the development of the exposures [9]. The lines shown are nominally  $0.3\text{ }\mu\text{m}$  wide. The e-beam size, as indicated at the top of each micrograph, increases from left to right proceeding from the left uppermost figure to the lower right figure. The micrographs demonstrate conclusively the degradation of the exposed and developed patterns with increasing e-beam size. A change of about  $0.02\text{ }\mu\text{m}$  in beam diameter alters the exposure profiles significantly, as is evident in the middle micrographs.

From the preceding discussion, it is evident that e-beam exposure tools satisfy all of the requirements, i.e., resolution, linewidth, pattern overlay, etc., for submicron ( $0.25\text{-}\mu\text{m}$ ) circuit devices. However, the e-beam tool cannot be viewed as an independent entity, but must be considered as an integral part of a lithographic system in which the resist material and development process are equally important. The resist and process development must be coupled closely with the functional dependencies of the e-beam tool.

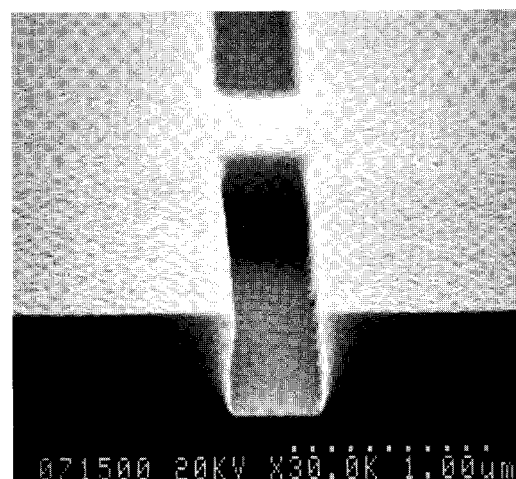
Measurements of linewidth and overlay tolerance must be performed in order to guarantee lithographic accuracy and thereby achieve the required device performance. This is accomplished by measuring resist images with a low-voltage scanning electron microscope with a precision and accuracy of about  $\pm 100\text{ }\text{\AA}$ . As can be seen from the line scan traces at the top of Figure 4, the proper choice of the measurement points is critical in defining linewidths. The line scans are the measured secondary electron currents as the e-beam is scanned across the lines between the two arrows shown in the micrographs. Shown are  $0.4\text{-}\mu\text{m}$  lines spaced  $0.6\text{ }\mu\text{m}$  apart; the right micrograph is an isolated space. This technique has been used to measure a wide spectrum of feature sizes ranging from minimum linewidths of  $0.1$  to  $3\text{ }\mu\text{m}$ .

### Fully scaled $0.5\text{-}\mu\text{m}$ test device fabrication

This section describes and discusses a few of the processing steps in the fabrication of a prototype chip with  $0.5\text{-}\mu\text{m}$  ground rules. All of the electron-beam lithography in this test-device fabrication used the modified EL-3 variable shaped-beam system in the direct-write mode. This provides the advantage of chip-to-chip registration, thus allowing accurate level-to-level overlay. Before the actual exposure of the pattern in any one of the levels, the electron-beam deflection field is calibrated with respect to the four corner marks of the chip field and, if necessary, adjusted accordingly. This calibration of both chip field and exposure field at every chip guarantees that all levels of lithography are registered to the same marks, which in turn provides precise



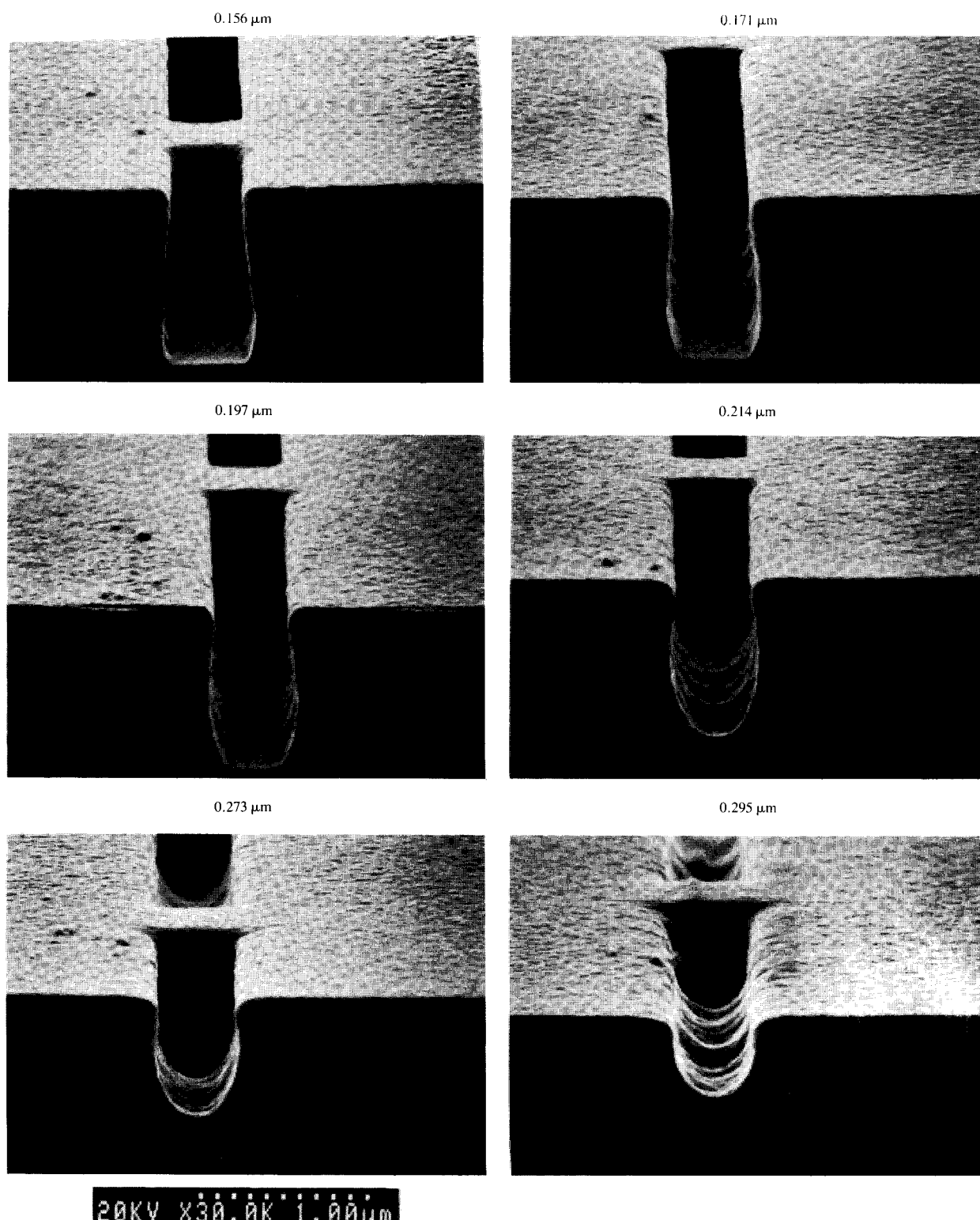
(a)



(b)

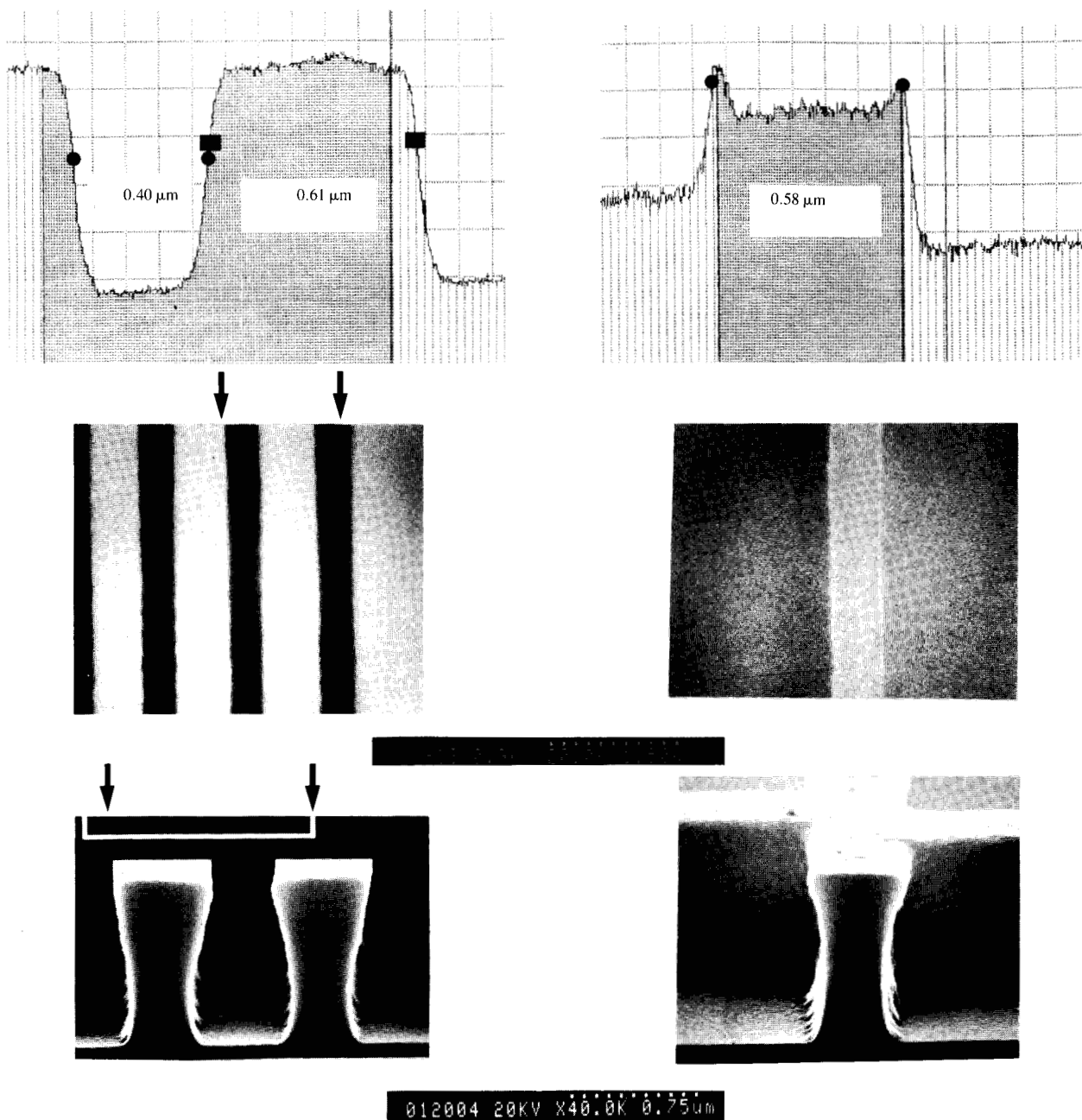
### Figure 2

Comparison of 0.5- $\mu\text{m}$  lithographic images with and without proximity corrections. The uppermost row of Figures 2(a) and 2(b) shows isolated resist lines which were exposed to achieve optimum development. The identical exposure was used for the spaced line array and the single line in Figure 2(a). Similar arrays shown in Figure 2(b) were exposed using proximity correction.



**Figure 3**

The effect on resist profile and resist development as a function of e-beam diameter [9]. The image degradation with increasing beam diameter is clearly apparent. Note that increases in beam diameter as small as  $\approx 0.02 \mu\text{m}$  cause significant changes in the resist images. The nominal linewidth is  $0.3 \mu\text{m}$ .

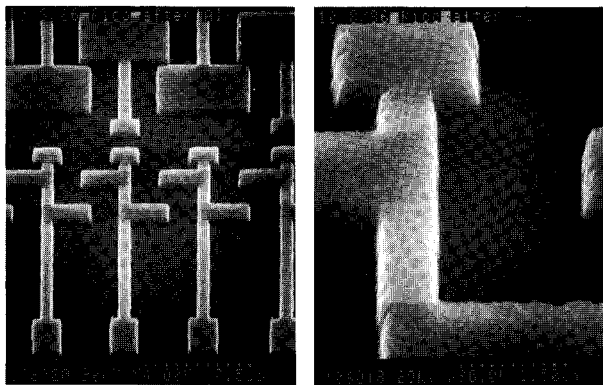


**Figure 4**

Linewidth measurements on resist images using a low-voltage scanning electron microscope. The two top figures are line scans across the patterns shown below. The middle micrographs are top views; the bottom are SEM micrographs of the lines.

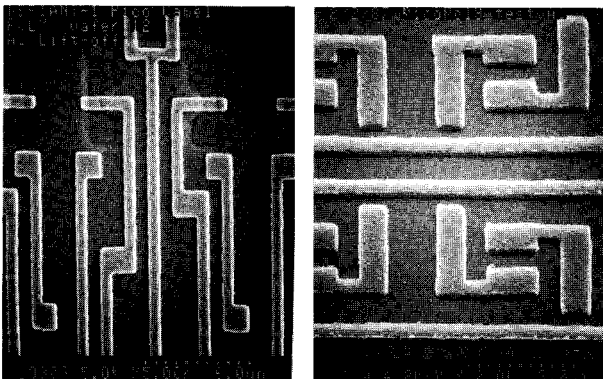
pattern overlay. This implies that a registration level consisting of cluster marks [10] which define the chip size and wafer layout is the first patterning step. Redundant sets of marks are also included in the same lithography step for recovery purposes in case the primary marks are degraded or

destroyed during subsequent processing steps. All other lithography levels are referenced and calibrated to the registration marks before pattern writing, guaranteeing that the overlay precision is within the capability of the electron-beam tool.



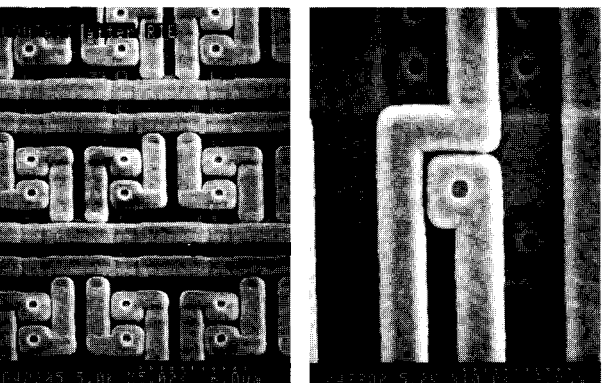
**Figure 5**

0.5- $\mu\text{m}$  e-beam lithography for recessed oxide (ROX) in a fully scaled CMOS device [12].



**Figure 6**

0.5- $\mu\text{m}$  e-beam lithography for CMOS poly-gate definition [12].



**Figure 7**

0.4- $\mu\text{m}$   $\times$  0.4- $\mu\text{m}$  contact holes for a CMOS device.

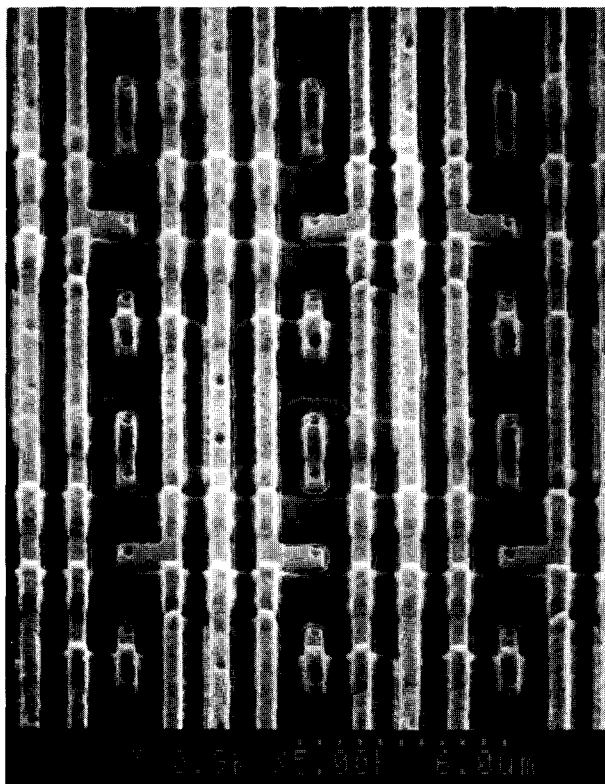
To fabricate device chips, many processing steps, lithography, implants, etc. must be performed in a particular processing sequence. Only those processing steps which utilize e-beam lithography are discussed here. The first lithography step after the registration mark defines the recessed silicon oxide (ROX) level. This pattern level, which delineates the gate, source, and drain areas, is formed through an image-reversal technique which depends on an aluminum lift-off process [11]. The lift-off process generates an undercut resist profile over which a thin aluminum film is deposited over the patterned resist surface; the lift-off of the remaining resist forms a metal etch mask. In **Figure 5** are two scanning electron micrographs of a portion of the device pattern after the lift-off process [12]. The micrograph on the left is of 0.5- $\mu\text{m}$  lines; the right micrograph shows an enlargement of a 0.5- $\mu\text{m}$  line.

An important step in the lithography sequence is the definition of the polysilicon gate region. The metal lift-off image-reversal process is again used. A 1.0- $\mu\text{m}$ -thick resist imaging layer is required for this step. The actual lithography for the polysilicon-level mask after completion of the metal lift-off is shown in the top-view scanning electron micrograph shown on the left in **Figure 6** [12]. On the right, the pattern of a small portion of the array shows a 0.6- $\mu\text{m}$  feature size.

Final device performance is not determined solely by the poly-gate-to-ROX dimensions and overlay, but is also dependent upon the precise control of the size and placement of contact holes in the source, drain, and gate regions. A multilayer resist strategy is used for the imaging and pattern transfer process. A minimum contact hole size of 0.4  $\mu\text{m}$   $\times$  0.4  $\mu\text{m}$  and a contact-to-poly-gate overlay accuracy of 0.1  $\mu\text{m}$  are required for this level. A portion of the reactive-ion-etched contact hole array is shown in **Figure 7**. The right micrograph is an enlargement of the one on the left; a contact hole is shown near the middle of this micrograph.

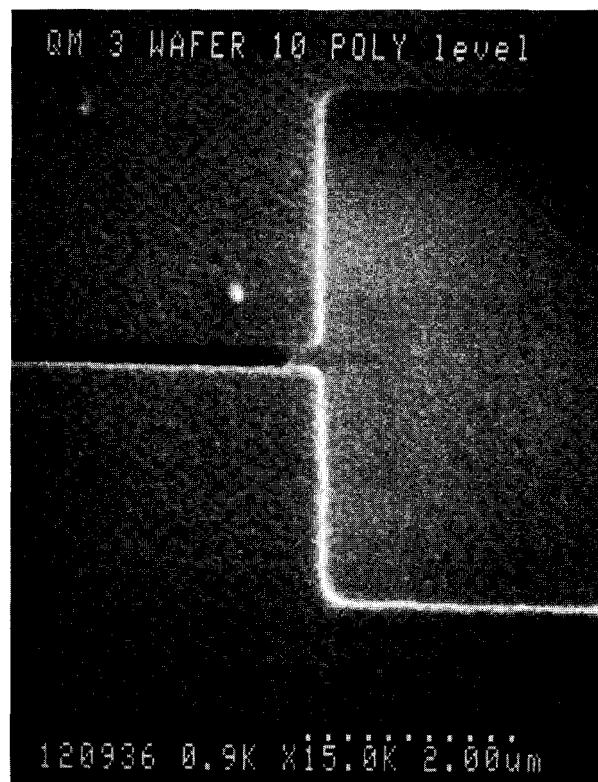
In order to provide interconnection between discrete device elements, a level of metal alloy wiring is defined and accurately overlaid to the contact hole array. A 1.0- $\mu\text{m}$ -thick resist is exposed to produce an undercut profile which provides the lift-off mask required for the formation of the interconnect metallization. The fine-line patterning of this metal level with 0.6- $\mu\text{m}$ -wide lines with a 1.2- $\mu\text{m}$  pitch, as shown in **Figure 8**, provided the means to make dynamic electrical performance measurements on these devices. The performance of a 31-stage ring oscillator was measured, and an average delay time of 75 picoseconds per stage was recorded.

The successful completion of functional CMOS devices demonstrated that device design and device technology, in conjunction with electron-beam lithography techniques, can be used to produce fully scaled 0.5- $\mu\text{m}$  integrated circuit devices. This was achieved by using an EL-3 system. The



**Figure 8**

First metal level for CMOS interconnect pattern showing 0.6- $\mu\text{m}$  lines with a 1.2- $\mu\text{m}$  pitch.



**Figure 9**

0.25- $\mu\text{m}$  resist image. This image is a top view of the resist pattern taken in an SEM before pattern transfer through lift-off process.

higher resolution capability of the Vector Scan Gaussian round-beam system was utilized in NMOS and PMOS test devices with minimum feature dimensions of 0.25  $\mu\text{m}$ . A section of the poly-gate-level lithography for these devices is shown in the SEM top-view micrograph of **Figure 9**. This figure demonstrates that dimensions in CMOS device fabrication can be further reduced.

### Summary

Electron-beam lithography systems of the EL-3 type and the Gaussian round-beam Vector Scan type have been applied to 0.5- $\mu\text{m}$  and 0.25- $\mu\text{m}$  semiconductor device fabrication. An overall integration of lithography tools, processes, and device technology was successfully demonstrated. The acquired knowledge and understanding of potentially limiting factors, such as proximity effect, electron-beam system instabilities, electron beam/substrate interactions, and other error sources affecting electron-beam lithography accuracy, provide the basis for further reductions in minimum dimensions. This continued trend translates directly into increased circuit density and higher performance for chips of the future.

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### References

1. A. N. Broers and T. H. P. Chang, "High Resolution Lithography for Microcircuits," *Research Report RC-7403 (31860)*, IBM T. J. Watson Research Center, Yorktown Heights, NY, 1978.
2. T. H. P. Chang, M. Hatzakis, A. D. Wilson, A. J. Speth, A. Kern, and H. Luhn, "Scanning Electron Beam Lithography for Fabrication of Magnetic Bubble Circuits," *IBM J. Res. Develop.* **20**, 376 (1976).
3. H. C. Pfeiffer, "Variable Spot Shaping for Electron Beam Lithography," *J. Vac. Sci. Technol.* **15**, 887 (1978).
4. T. Matandon, "Submicrometer Electron Beam Direct Writing Technology for 1-Mbit DRAM Fabrication," *IEEE J. Solid State Circuits* **SC-20**, 144 (1985).
5. M. Parikh, "Corrections to Proximity Effects in Electron Beam Lithography," *Research Report RC-2254 (30447)*, IBM T. J. Watson Research Center, Yorktown Heights, NY, 1978.

6. A. N. Broers, "Resolution Limits for Electron-Beam Lithography," *IBM J. Res. Develop.* **32**, 502 (1988, this issue).
7. T. H. P. Chang, D. P. Kern, E. Kratschmer, K. Y. Lee, H. E. Luhn, M. A. McCord, S. A. Rishton, and Y. Vladimirovsky, "Nanostructure Technology," *IBM J. Res. Develop.* **32**, 462 (1988, this issue).
8. H. C. Pfeiffer, T. R. Groves, and T. H. Newman, "High-Throughput, High-Resolution Electron-Beam Lithography," *IBM J. Res. Develop.* **32**, 494 (1988, this issue).
9. M. G. Rosenfield, J. J. Bucchignano, S. A. Rishton, D. P. Kern, L. M. Kettell, W. M. Molzen, F. J. Hohn, R. Viswanathan, and J. M. Warlaumont, "Submicron Electron Beam Lithography Using a Beam Size Comparable to the Linewidth Tolerance," *J. Vac. Sci. Technol. B* **5**, 114 (1987).
10. S. J. Gillespie, C. G. Bremer, and P. P. Boulay, "Extensions to 0.5  $\mu\text{m}$  Lithography on EL-3," *Proceedings of Microcircuit Engineering '84*, Berlin, W. Germany, A. Heuberger and H. Beneking, Eds., Academic Press, Inc., New York, 1984.
11. M. Hatzakis, "Electron Resist for Microcircuit and Mask Production," *J. Electrochem. Soc.* **116**, 7 (1969).
12. P. J. Coane, P. Rudeck, L. K. Wang, and F. J. Hohn, "Electron Beam/Optical Mixed Lithography at Half-Micron Ground Rules," *Proceedings of Microcircuit Engineering '86*, Interlaken, Switzerland, H. W. Lehmann and Ch. Bleiker, Eds., North-Holland Publishing Co., Amsterdam, 1986.

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**Fritz J. Hohn** *IBM Research Division, T. J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598.* In 1977 Dr. Hohn received his Ph.D. in physics—experimental electron optics/electron backscattering—from the Technical University of Berlin. He began work at the T. J. Watson Research Center in 1978 as a postdoctoral intern, joining IBM in 1980. His technical work includes the development of a high-brightness LaB<sub>6</sub> single-crystal electron gun for e-beam fabrication systems, the optimization of a low-voltage electron gun, and the feasibility demonstration of a dual-potential e-beam test technique. In 1985, he transferred to the East Fishkill e-beam technology area as manager of e-beam test systems, continuing work on electron-beam testing of large-area packaging substrates. Dr. Hohn moved to the T. J. Watson Research Center in 1985, assuming responsibility as manager of the electron-beam lithography group. He has published many papers and made presentations in all these fields, and holds numerous patents and patent applications.

**Alan D. Wilson** *IBM Research Division, T. J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598.* Mr. Wilson received his B.S. degree in electrical engineering in 1959 from the University of Utah. In 1960 he received an M.E.E. degree from Cornell University and then joined IBM at its development laboratory in Endicott, New York. He worked on the failure of electrical and mechanical computer components and did research on incandescent tungsten. Later, his research was on holographic interferometry: theory and application. In 1972, Mr. Wilson joined the Research Division of IBM to participate in the development of vector scan electron-beam lithography. He was responsible for development of the electronic control systems, autoregression techniques, laser-controlled stages, and system software. In 1980 he assumed responsibility for development of an X-ray stepper and alignment system for use on a storage ring beamline. He is currently manager of chip lithography, which includes the X-ray program, electron-beam lithography, and ion-beam lithography for submicron dimensions. Mr. Wilson is a member of the Optical Society of America and the Society of Photo-Optical Instrumentation Engineers. He received a Best Paper Award from the IEEE in 1972, and has also received five Outstanding Achievement Awards and three patent level awards from IBM. Mr. Wilson has been awarded patents in the fields of optics, solid-state devices, and lithography technology.

**Philip J. Coane** *IBM Research Division, T. J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598.* Mr. Coane is a Research Staff Member and project manager of the shaped-beam lithography systems group in the Silicon Technology Department at the T. J. Watson Research Center. Prior to joining IBM in 1978, he was a technical staff member at Hughes Research Laboratories for fifteen years, working on ion-propulsion systems and the application of electron beams to the fabrication of exploratory surface acoustic wave transducers and gallium arsenide field-effect transistors. Since 1978, his work has been primarily concerned with the application of electron beams to the microfabrication of advanced submicrometer CMOS and bipolar semiconductor devices. Mr. Coane received an A.Sc. in electronics engineering in 1969 from Los Angeles Pierce College and a B.Sc. in physics in 1974 from California State University at Northridge. He holds several patents and has authored or co-authored numerous publications in the field of electron-beam technology. Mr. Coane is a member of the Society of Photo-Optical Instrumentation Engineers.