

High-throughput, high-resolution electron-beam lithography

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The introduction of the shaped-beam imaging technique has greatly enhanced the exposure efficiency of electron-beam lithography systems. IBM's EL systems provide the throughput needed for lithography applications in semiconductor fabrication lines. The resolution of these systems has been steadily improved over the past 15 years in support of the semiconductor lithography trend toward submicron dimensions. This paper describes the latest version (EL-3 system) capable of fabricating 0.25- μ m features. The technical challenges of submicron e-beam lithography are discussed, and practical solutions together with experimental results are presented.

Introduction

Electron-beam (e-beam) lithography has played an important role in advancing the science and technology of very small semiconductor and metal device structures. Electron beams were originally applied to the fabrication of integrated circuits by microlithography in order to attain

resolution beyond the capability of light optics [1, 2]. This is similar to the motivation which led to the electron microscope. The electron wavelength is 4 to 5 orders of magnitude shorter than the illumination used in optical exposure systems. The shorter electron wavelength provides resolution which is, for practical purposes, unlimited. The practical resolution limits in e-beam lithography are determined instead by the interaction of the beam electrons—with each other [3], with the resist, and with substrate material as well. By using thin-membrane substrates to minimize electron scattering and the resulting proximity effect [4], device fabrication has been demonstrated to dimensions as small as 12 nm [5].

The first large-scale industrial application of electron-beam lithography did not make use of its high resolution capability; instead it exploited the ability of electron probe systems to directly generate patterns at high speed under computer control [6]. Electron beams were first used to fabricate photo-masks for conventional optical lithography [7]. This became the mask technology of choice throughout the semiconductor industry because e-beams provided the required speed, flexibility, resolution, and accuracy.

However, the ultimate goal is to write directly on the wafer, eliminating the expensive, time-consuming mask steps entirely. A fundamental advantage of direct writing is the capability to use the writing e-beam probe to precisely measure and correctly position device patterns on the wafer. Direct writing permits the most effective use possible of the e-beam pattern generation capability. An example of a high-density circuit pattern fabricated by direct-write lithography

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is shown in **Figure 1**. It is a high-density SRAM memory circuit employing fully scaled 0.5- μm CMOS technology. Fabrication of device structures of 0.25 μm and below is discussed by Hohn et al. in this issue [8].

Evolution of electron-beam lithography

Electron-beam lithography has a long history. Work at the IBM Thomas J. Watson Research Center began in the early 1960s, and submicron structures were subsequently fabricated with scanning electron microscope (SEM) systems [9, 10]. However, the unique flexibility for maskless pattern generation has an associated drawback. The image elements or pixels must be exposed serially. The number of pixels is large, typically several orders of magnitude more than in a high-quality electron micrograph. These factors impose a severe limitation on exposure efficiency and speed. The development of the shaped-beam approach enhanced the exposure efficiency and made electron-beam lithography a reality in semiconductor production lines [11]. This approach derives its name from the fact that the beam is imaged to a rectangular-shaped spot on the writing surface, allowing several pixels to be printed in parallel. By contrast, the earlier single-pixel mode employs a spot which is "shapeless," since it defines the resolution limit of the electron-optical system. The evolution of high-throughput electron-beam lithography (EL) systems began with the shaped-e-beam concept and the development of the first shaped-e-beam prototype in the late 1960s [12]. This early prototype demonstrated the feasibility of shaped-e-beam exposure, and the throughput advantage of the parallel-pixel projection technique over the conventional Gaussian round-beam approach. The successful completion of this work led to the development of the first-generation, high-throughput, direct-write production tool EL-1. **Figure 2** illustrates the evolution of EL tools and shows how the minimum device feature size decreased with time.

The primary application of the EL tools, which provided incentive for their development, was for the production of Application Specific Integrated Circuit (ASIC)-type devices. The tool installations, however, ranged from research laboratories to product development facilities and semiconductor manufacturing lines. The first EL-1 tool was installed in the IBM East Fishkill Semiconductor Development Laboratory in 1973. The first manufacturing installation was in the Quick Turn Around Time (QTAT) production line in 1976 [13]. Semiconductor product ground rules at that time were minimum pattern dimensions of 2.5 μm , and were exposed with a fixed shaped beam of $2.5 \times 2.5 \mu\text{m}$. The second-generation tool, EL-2, which used a variable shaped-beam technique, permitted extension to smaller dimensions (1.25 μm) with enhanced exposure efficiency [14]. Several hundred pixels could now be exposed in parallel. The EL-2 tools were used for semiconductor development of 1.25- μm minimum device features.

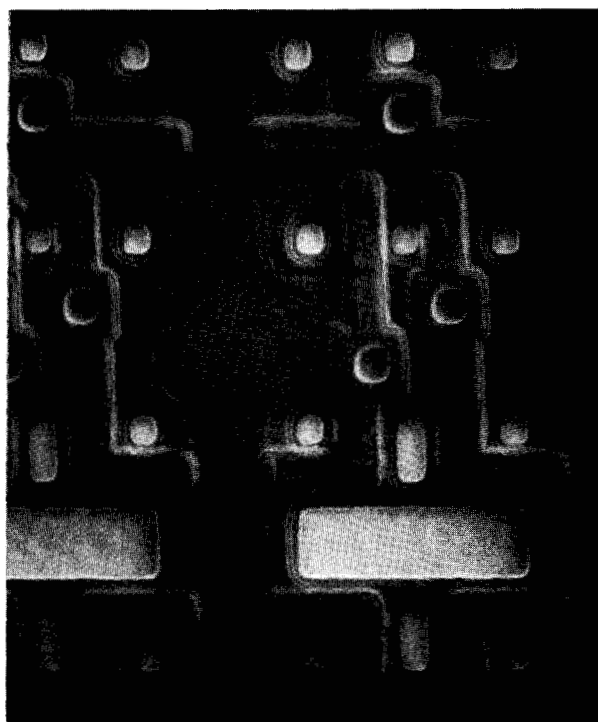


Figure 1

Contact hole e-beam lithography. The isolated square features are contact via holes 0.40 μm in size. The dark lines under the oxide are 0.5- μm polysilicon gates.

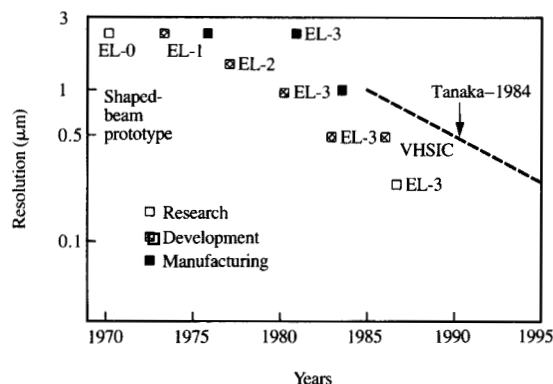


Figure 2

IBM EL tool evolution and lithography trend in the semiconductor industry. The minimum size of device features decreased from 2.5 μm in 1970 to 0.25 μm in 1987.

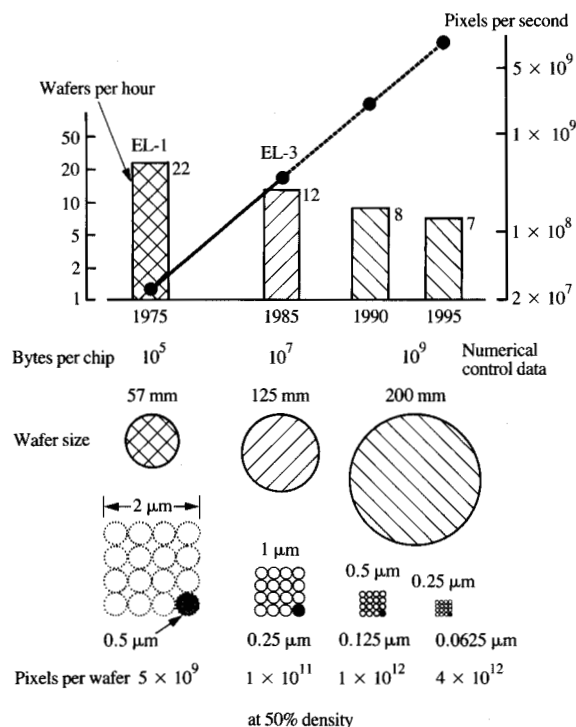


Figure 3

Electron-beam and semiconductor technology evolution. Exposure speed is shown in wafers per hour and in pixels per second, as a function of semiconductor requirements. The parameters are wafer size, pixel size, and numerical control data volume. The numbers to the right of each column indicate wafer throughput per hour.

EL-3, the third-generation tool, the high-throughput version of the variable shaped-beam system [15], was originally designed to cover a lithography range from 1.0 μm to 2.5 μm . The first tool was operational in 1980. By 1983 the EL-3 system had been modified for submicron product development work [16], and the 0.5- μm version became the tool for Very High Speed Integrated Circuit (VHSIC) device production. The latest extension of EL-3 to 0.25- μm lithography applications is the primary subject of this paper. The 0.25- μm version has been operational since the end of 1987. Figure 2 illustrates the remarkable extendability of the shaped-beam direct-write tools. The EL-3 has been greatly enhanced by extending its useful range to 0.25- μm feature sizes.

With the continual increase in the density and complexity of integrated circuits, it is predicted that large-scale manufacture of circuits with 0.25- μm geometries will be practiced in the early 1990s. The immense amount of pattern information needed for devices of this size places even more stringent demands upon the resolution and speed of the e-beam writing tools. Figure 3 illustrates the impact

this will have on EL tools. When EL-1 was introduced in 1975, it provided a throughput of 22 wafers per hour, establishing a new state of the art for e-beam direct-write systems. Ten years later, despite significant technical progress, the throughput had actually declined to 12 wafers per hour, due to a dramatic increase in the amount of pattern information contained on a wafer. Unfortunately for direct-write e-beam systems, the performance of lithography tools is measured in wafers per hour rather than in pixels per second, which would more accurately reflect the exposure speed. In 1975 the wafer size was 57 mm and the minimum feature size was 2 μm , with a pixel resolution of 0.5 μm (represented by the edge acuity of the shaped beam). The total number of exposed pixels per wafer was 5×10^9 for 50% pattern densities. By 1985 the wafer size had increased to 125 mm and the minimum feature size was reduced to 1.0 μm , with a 0.25- μm resolution. The pixel rate of EL-3 had increased approximately an order of magnitude over that of EL-1; however, the number of pixels per wafer had increased 20-fold. The anticipated semiconductor requirements for the 1990s mandate continued increases in pixel rates, in order to provide practical throughputs for production applications of direct-write e-beam tools. The next-generation tool must afford at least one order of magnitude increase in pixel rate, in order to accommodate 200-mm-diameter wafers with $<1/2\text{-}\mu\text{m}$ lithography ground rules. However, it is insufficient to increase pixel rates alone; the rate increase must be accompanied by similar improvements in pattern data handling capability. Numerical control data to define a single chip increased from 0.1 to 10 megabytes in the ten years from 1975 to 1985, and is expected to reach levels of 1 gigabyte by the early 1990s.

Limitations and solutions

As mentioned, the major limitation of e-beam lithography is throughput. The writing speed is proportional to the total e-beam current in the writing probe; hence, for significant writing speed increases there must be concomitant increases in beam current. A fundamental limit on the usable current is imposed by the mutual Coulomb repulsion between beam electrons. The repulsion manifests itself in two ways: The transverse component of the Coulomb force results in lateral blurring of the focused e-beam spot, while the longitudinal component gives rise to a broadening of the distribution of electron energies. The latter, called the Boersch effect [1], results in lateral blurring as well, because of the chromatic aberration of lenses and deflectors. The amount of blurring due to both components increases monotonically with the total beam current I . In practice, one increases I until the blurring becomes just barely tolerable.

Fast electrons experience less Coulomb broadening than slow electrons, due to the shorter transit time through the column at higher beam energy. This suggests another degree

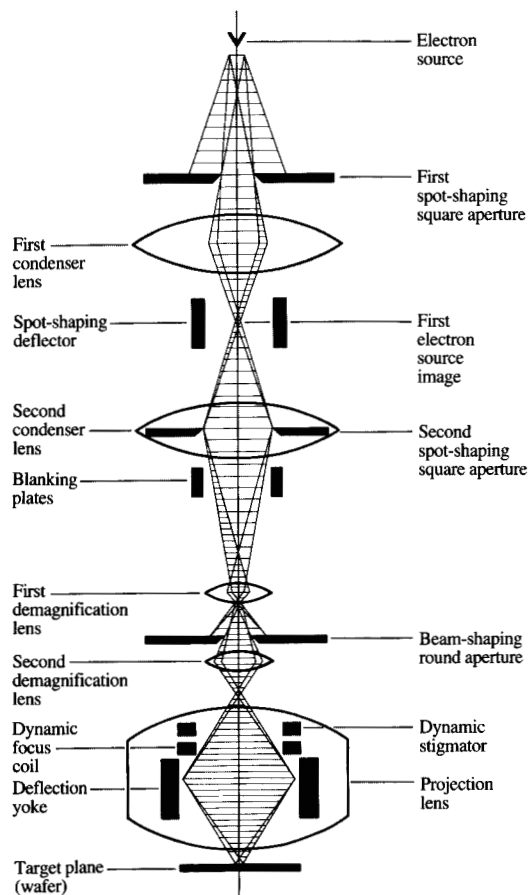


Figure 4

Schematic representation of the variable shaped-beam EL-3 electron-beam column.

of freedom, the accelerating potential V . In fact, the blurring due to Coulomb interaction is roughly proportional to $I/V^{1.5}$. It follows that one can increase the current proportional to the 1.5 power of the accelerating potential with no change of blurring. Next we must assess the impact on writing speed. The writing speed (area/time) is I/D , where D is the dose (charge/area) required to expose the resist. The dose D is proportional to V , since the incident energy absorbed by the resist decreases with increasing electron energy. It follows from these arguments that the writing speed, I/D , increases with the square root of the accelerating potential V . An equivalent way of saying this is that the increase in usable current at higher accelerating potential more than offsets the increase in dose required. It is advantageous from the point of view of writing speed to use high accelerating potential.

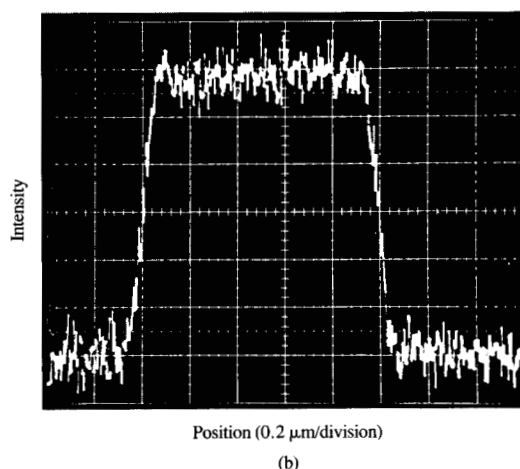
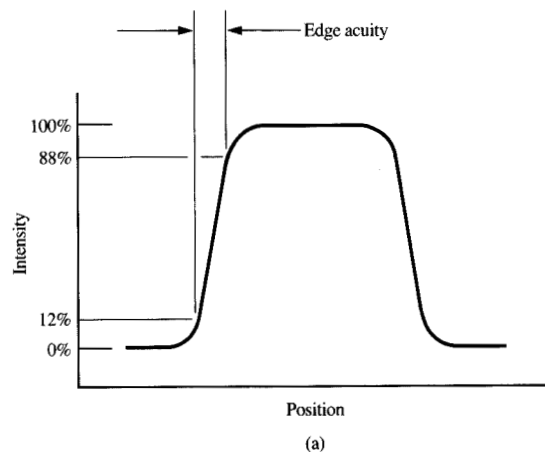


Figure 5

Intensity distribution of a shaped spot: (a) schematic, showing the definition of edge acuity; (b) measured. The edge acuity is $0.070 \mu\text{m}$ for a $1.0 \mu\text{m}^2$ spot at 50 kV, 50 A/cm².

Fabricating 0.25- μm structures

The electron-beam column is shown schematically in **Figure 4**. A single-crystal lanthanum hexaboride cathode forms the electron source. The source floods a square aperture uniformly with electrons. This aperture is imaged onto a second square aperture by means of the first condenser lens. The spot-shaping deflector allows all or part of the image of the first aperture to pass through the second aperture. The result is a rectangle of variable dimensions, which is demagnified onto the writing surface. The spot is moved over a 5-mm-square area on the writing surface by the deflection yoke.

The beam is also scanned over registration marks which have been previously written on the wafer. A signal derived

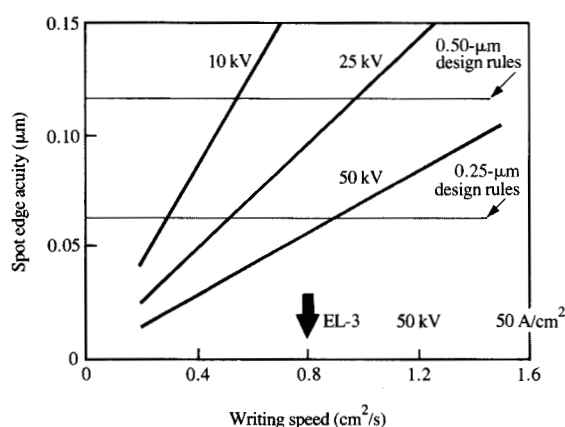


Figure 6

EL-3 edge acuity as a function of writing speed at various accelerating voltages. Also shown are the acuity limits set by the semiconductor device ground rules. (Writing speed = beam current/dose; dose at 50 kV = $2.5 \mu\text{C}/\text{cm}^2$; e-beam = $2 \mu\text{m}^2$ beam spot.)

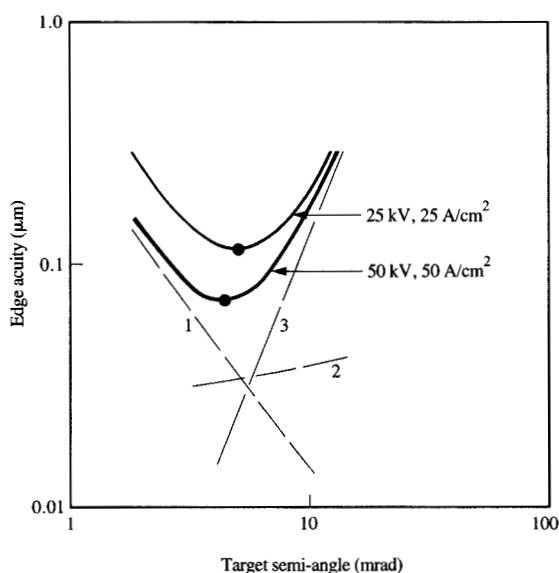


Figure 7

Edge acuity as a function of aperture. The various contributions are (1) transverse Coulomb repulsion, (2) longitudinal Coulomb energy broadening, (3) spherical aberration. The aperture is expressed as the beam cone semi-angle at the target surface. The resultant curves at 25 and 50 kV are shown. (Constant writing speed; $1.0 \mu\text{m}^2$ beam spot.)

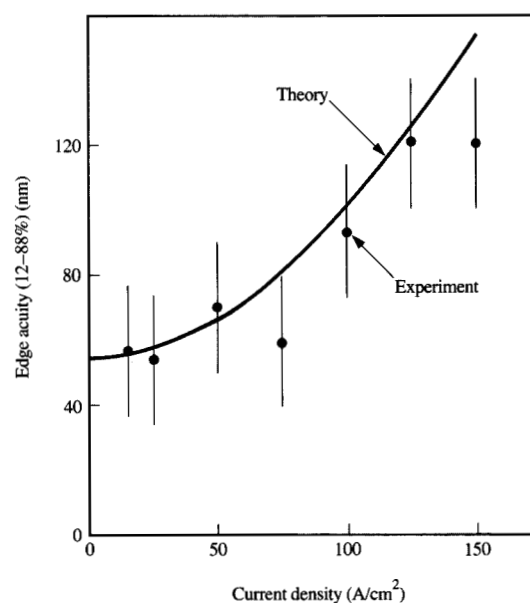


Figure 8

Edge acuity as a function of current density in the writing probe. The spot is $1.0 \mu\text{m}^2$ on axis at 50 kV. The points represent measured values, while the solid curve represents the result of a Monte Carlo simulation [16].

from the backscattered electrons allows precise positioning of the beam relative to the wafer. The backscattered electrons must have sufficient energy to penetrate and emerge from the resist, and 25 keV is a reasonable lower limit to the incident energy. However, on the basis of previous arguments concerning the suitability of higher accelerating voltages, a 50-kV system was built for writing device structures of $0.25\text{-}\mu\text{m}$ dimensions.

The wafer is clamped to an *X-Y* table which can be stepped around beneath the beam. The position (to a precision of about 10 nm) of the table is sensed continuously with a laser interferometer which also provides the metrological standard for the tool. Pattern information is downloaded to the tool from a host computer via a 128-megabyte pattern buffer. The electronic system can deflect the beam to the desired point on the wafer, select the appropriate spot shape, and unblank the beam for the proper exposure time, all of this in synchronism with the pattern data stream. The minimum exposure time is 100 ns for a single pattern feature. The performance of the system is best judged from the written patterns. In addition to obtaining good image quality in the developed resist, the images must

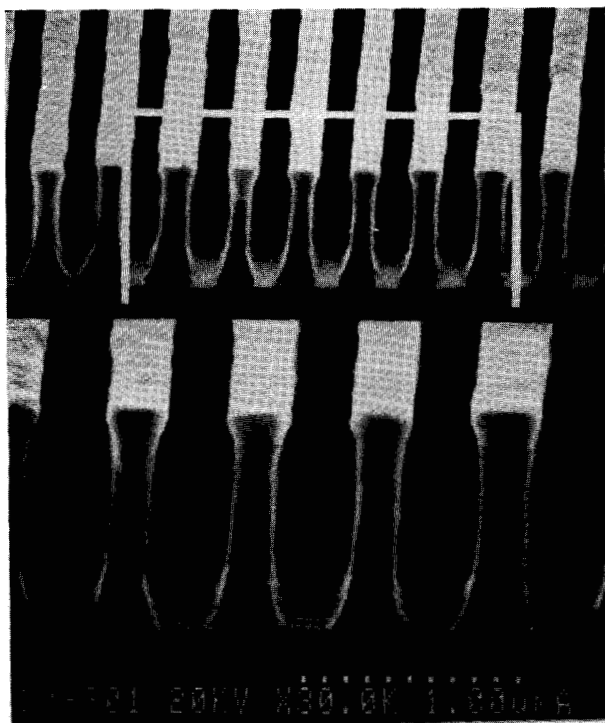


Figure 9

Profile of exposed resist. The distinct vertical walls indicate the sharpness of the writing probe. The lines are $0.15\text{ }\mu\text{m}$ wide, on $0.30\text{-}\mu\text{m}$ centers. The lower images are enlargements of the upper image. The extremities of the row of dots indicate a distance scale of $1\text{ }\mu\text{m}$ in the upper row.

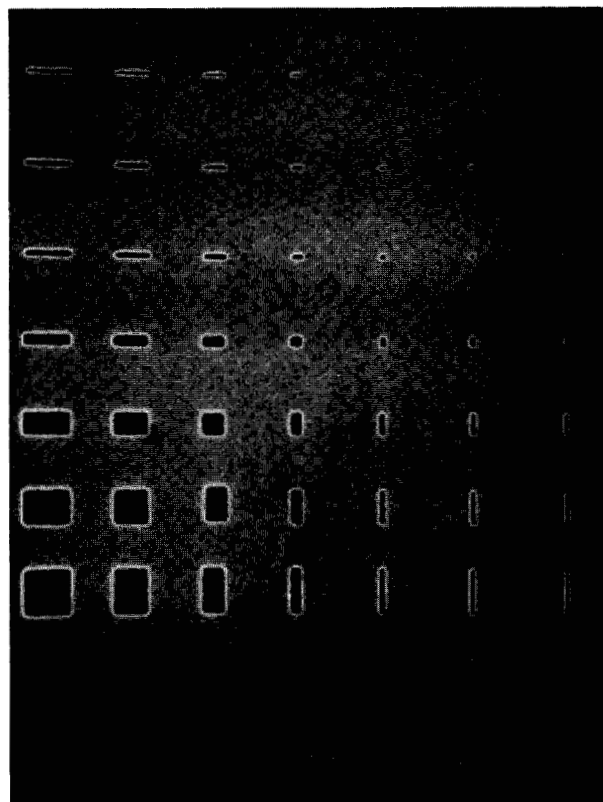


Figure 10

EL-3 test pattern. The distance scale, indicated by the extremities of the row of dots, is $10\text{ }\mu\text{m}$.

also be correctly positioned. This latter is referred to as overlay. The overlay accuracy was measured as $0.080\text{ }\mu\text{m}$ (worst case) for registered writing.

Ideally, the intensity profile of the focused spot should fall off infinitely sharply at the edges. Because of the blurring effects mentioned above, this is not possible. The intensity distribution is shown schematically in **Figure 5(a)**. We define the edge acuity as the width of the intensity distribution between the 12–88% intercepts. It is a figure of merit used to describe the quality of the electron-optical system. **Figure 5(b)** shows the actual intensity distribution measured by scanning the beam across a straight edge and detecting the current. The edge acuity for a $1.0\text{-}\mu\text{m}^2$ spot at 50 kV and 50 A/cm^2 is $0.070\text{ }\mu\text{m}$. The effect of varying the beam voltage is shown in **Figure 6**. The edge acuity always degrades as the writing speed increases. However, for a given writing speed the edge acuity improves with increasing e-beam accelerating voltages [17].

In addition to the Coulomb interaction, the spherical and the chromatic aberration of the lenses also contribute to the edge acuity. The size of these contributions depends on the choice of the system defining aperture, usually measured in

terms of the beam cone semi-angle at the writing surface. The influences of these factors for a constant e-beam spot size and beam current are shown as a function of aperture angle in **Figure 7**. The individual contributions at 50 kV are also shown in the figure. They are labeled (1) transverse Coulomb interaction, (2) longitudinal Coulomb interaction energy broadening, and (3) spherical aberration. The beam current is maintained constant. These data indicate that an optimum aperture exists for which the edge acuity is minimized, as indicated by the data points at the minima of the two curves. The minimum is chosen as the operating point for the system.

The edge acuity is shown as a function of probe-current density in **Figure 8** for a $1.0 \times 1.0\text{-}\mu\text{m}$ spot at 50 kV . The points represent measured values, while the solid curve represents values computed by a Monte Carlo simulation of the column [18]. In this simulation a random number generator was used to initialize electron trajectories in the source region. The individual particle trajectories were then computed, with the influence of the Coulomb repulsion taken into account. The effects of the lens defects were also included in the simulation.

The resolution is maintained over a 5-mm deflection area. The main deflection of the beam is done with a magnetic deflection yoke immersed in the final projection lens of the system. This arrangement, called in-lens deflection, minimizes the deleterious effect of deflection aberrations on spot edge acuity. These aberrations, primarily transverse chromatic aberration, limit the useful size of the field which can be written.

Examples of images written in positive resist are shown in Figures 9 and 10. The ability to resolve fine structures is shown here. It should be noted that this system was designed for use in a high-volume manufacturing environment. Unlike other systems capable of fabricating similar fine structures, this system overcomes much of the throughput limitation associated with earlier EL systems.

Conclusion

More than thirty EL systems are installed worldwide in IBM's semiconductor production lines. Applications range from research and early product development to full-scale manufacture of semiconductor devices. The system described here is capable of fabricating 0.25- μ m device structures.

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