

Study of contact and shallow junction characteristics in submicron CMOS with self-aligned titanium silicide

by Y. Taur
B. Davari
D. Moy
J. Y.-C. Sun
C. Y. Ting

The contact resistance between TiSi_2 and shallow n^+/p^+ source-drains in CMOS is studied for a variety of junction depths and silicide thicknesses. The contact contribution to the total device series resistance can be significant if excessive silicon and dopants are consumed during silicide formation. Low contact resistances are obtained for $0.15\text{-}\mu\text{m}$ n^+ and $0.20\text{-}\mu\text{m}$ p^+ junctions when the titanium thickness is reduced to keep a high doping concentration at the TiSi_2/Si interface. Alternatively, a nonstandard process can be employed to implant additional dopants into the titanium. A thin layer of dopants then out-diffuses into the silicon after the silicide reaction and anneal to help reduce contact resistance

and leakage currents. The latter technique is more extendable to CMOS devices which require thicker titanium films and/or shallower junctions.

1. Introduction

As CMOS technology is being scaled to submicron dimensions for higher performance and density, device series resistance becomes an important consideration. Since the MOSFET channel resistance decreases with channel length, even a small parasitic resistance would substantially offset the current-drive gain derived from scaling. The problem is further aggravated by the requirement of shallow source-drain for short-channel threshold control, since the source-drain sheet resistance tends to increase as the junction depth is scaled down. It is, therefore, necessary to employ a self-aligned silicide process [1] so that the gate and n^+/p^+ source-drain sheet resistances can be reduced by one to two orders of magnitude in submicron CMOS devices. However, self-aligned silicide formation is, in general, not a purely additive process. It consumes a layer of silicon as well as dopants in that layer in the absence of snowplow effects. For example, a silicon thickness of typically 1.5 times the deposited titanium thickness is consumed to form TiSi_2 . This may lower the

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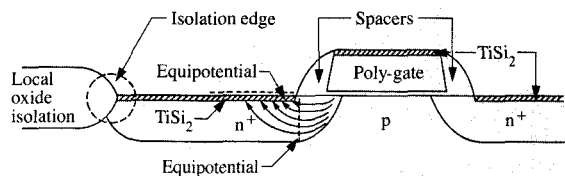


Figure 1

Schematic diagram of an n-channel MOSFET fabricated with self-aligned TiSi₂, showing the current distribution between the channel and silicide. The dashed circle indicates the junction-isolation boundary where silicide-induced leakage may occur due to field-oxide over-etch.

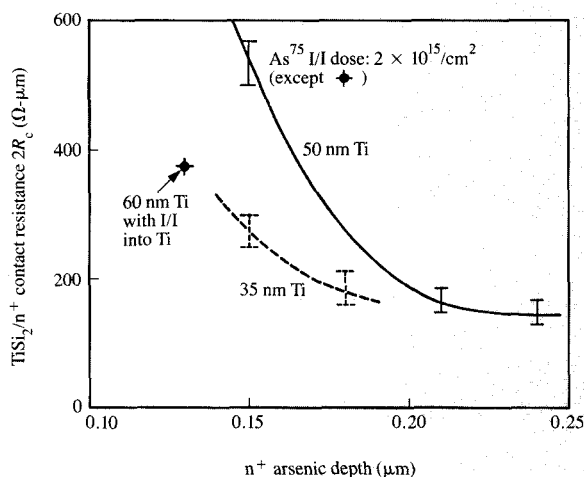


Figure 2

Measured TiSi₂/n⁺ contact resistance (including both sides of the FET) versus arsenic depth for two titanium thicknesses. The isolated point represents the contact resistance obtained with an additional arsenic implant into titanium (discussed in Section 3). Note: I/I = ion implantation.

doping concentration at the silicide/silicon interface and cause an unacceptably high contact resistance. In addition, there is a potential junction leakage concern if the silicide approaches the depletion region near the isolation edge. Both of these effects must be taken into consideration in the process design.

In this paper, the contact resistance between TiSi₂ and n⁺ or p⁺ diffusions is studied for different titanium thicknesses

and shallow source-drain profiles (0.15–0.25 μm deep). The contact resistivities are measured versus temperature to investigate the current transport at the TiSi₂/Si interface. It is shown that, in order to maintain low contact resistance and leakage currents, the titanium thickness must be kept below a certain limit. Alternatively, an unconventional process can be used to implant additional arsenic or boron into titanium prior to silicide formation [2]. This raises the doping concentration at the TiSi₂/Si interface due to the out-diffusion of a thin layer of dopants. The advantage of the implanted-titanium technique is that it allows the use of a thicker titanium film for decreased silicide sheet resistance without contact or leakage problems.

2. Contact resistance of TiSi₂ to n⁺ and p⁺ source-drains

A schematic cross section of an n-channel MOSFET fabricated with self-aligned TiSi₂ is shown in **Figure 1**; p-channel devices have a similar structure. Dielectric spacers are formed prior to silicide formation to prevent bridging between the gate and source-drain. There is a nonsilicided region under the spacer. The FET current flows out of the surface channel through the nonsilicided n⁺ region into the silicide film. The effective contact resistance (R_c) between the n⁺ region and TiSi₂ is defined by the two equipotential surfaces (a good approximation) shown in **Figure 1**. It arises from the finite contact resistivity between TiSi₂ and n⁺ or p⁺ diffusions and includes some silicon resistance underneath the TiSi₂ layer. Once the current flows completely into the silicide film, there is no further appreciable resistance, since both the TiSi₂ sheet resistance and the contact resistivity between TiSi₂ and metal are very low. In most practical situations, the effective contact resistance R_c is independent of the diffusion width in the direction of current flow (electrically long contacts) [3]. This is due to current crowding near the dielectric-spacer end of the silicided region. By definition, 2R_c represents the contact contribution to the total FET series resistance. The unit for 2R_c is Ω-μm, since the resistance is inversely proportional to the FET width perpendicular to the current flow.

In order to measure R_c directly, test structures are fabricated with TiSi₂ formed only in the contact hole areas. This enables the current to flow through the TiSi₂/Si interface so that R_c can easily be extracted from a transmission-line-type test site [4]. Another test structure used in this study is a standard Kelvin-type four-point site to measure the contact resistivity ρ_c (in Ω-cm²) with proper geometrical corrections [5]. Since the contact resistivity between TiSi₂ and the aluminum metallurgy used is negligibly low, the resistance from the four-point measurement can all be attributed to the contact between TiSi₂ and n⁺ or p⁺ diffusions.

The measured TiSi₂/n⁺ contact resistance contribution to the total device series resistance is plotted in **Figure 2**

versus the arsenic depth. The same arsenic implant dose, $2 \times 10^{15}/\text{cm}^2$, is used except for the isolated point, which is discussed later. The drive-in cycle varies from 30 to 60 minutes at 900°C to 950°C to yield different depths. The arsenic depths are measured from SIMS profiles. When 50-nm-thick titanium is used, the TiSi_2 sheet resistance is $4 \Omega/\square$ and the contact resistance is low if the junction is deeper than $0.20 \mu\text{m}$. However, for a $0.15\text{-}\mu\text{m}$ -deep junction, the contact resistance increases significantly. The impact of such a high contact resistance on the n-MOSFET linear transconductance is shown in **Figure 3**. There is a significant degradation at low drain and high gate biases when the channel resistance is low. The transconductance degradation would be even worse for submicron-channel-length devices. The high contact resistance is due to excessive silicon consumption with respect to the arsenic depth, as shown by the SIMS profile in **Figure 4**. For a 50-nm titanium thickness, the arsenic concentration at the projected TiSi_2/Si interface is only $\approx 3 \times 10^{19}/\text{cm}^3$. This is responsible for the high contact resistance. Contact resistance can be lowered if the titanium thickness is reduced to 35 nm so that the interface doping is above $1 \times 10^{20}/\text{cm}^3$ (**Figure 4**). The measured $2R_c$ values in this case are shown by the dashed curve in **Figure 2**. For an arsenic depth of $0.15 \mu\text{m}$ with a titanium thickness of 35 nm, the TiSi_2 sheet resistance is $6 \Omega/\square$ and the contact resistance contribution is less than $300 \Omega\text{-}\mu\text{m}$. This is acceptable when compared with a minimum channel resistance of $2000 \Omega\text{-}\mu\text{m}$ in the linear region of a $0.5\text{-}\mu\text{m}$ NMOS transistor [6].

The measured TiSi_2/p^+ contact resistance is shown in **Figure 5** as a function of implanted boron dose. The low-energy boron implant is made after a silicon pre-implant to amorphize the substrate in order to prevent boron channeling. The drive-in cycle after a 600°C anneal to regrow the substrate is 15 minutes at 900°C , which gives a p^+ source-drain depth of around $0.20 \mu\text{m}$. The TiSi_2 sheet resistance, $4 \Omega/\square$, is slightly lower than the n^+ case for the same 35-nm titanium thickness. **Figure 5** shows that the contact resistance decreases with increasing boron dose as expected. A $2 \times 10^{15}/\text{cm}^2$ dose is sufficient to bring $2R_c$ to an acceptable level. Higher doses will cause a deeper junction because of concentration-enhanced diffusion effects, but will not improve the contact resistance significantly. The SIMS profile in **Figure 6** shows that although there is a second boron peak coinciding with the initial amorphous/crystalline boundary, the boron concentration near the TiSi_2 interface is about $1 \times 10^{20}/\text{cm}^3$. Also noted from the SIMS profile is that the TiSi_2/p^+ contact resistance is less sensitive to the titanium thickness than the n^+ case. This is because the boron profile is not as steep as the arsenic near the silicide interface.

Both TiSi_2/n^+ and TiSi_2/p^+ contact resistivities have been measured at low temperatures to study the current transport at the interface. The results are shown in **Figure 7**. Very

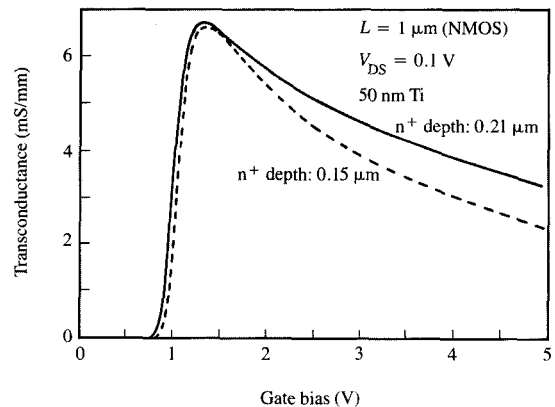


Figure 3

Low-drain linear transconductance of n-channel MOSFETs versus gate voltage for different arsenic depths with the same titanium thickness and effective channel length.

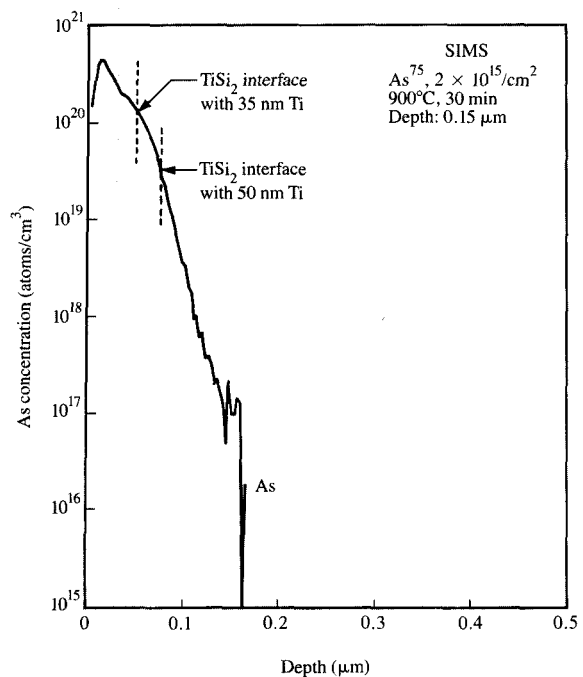


Figure 4

SIMS arsenic profile for the $0.15\text{-}\mu\text{m}$ -deep case in **Figure 2**. The dotted lines indicate the projected TiSi_2/Si interfaces for the corresponding titanium thickness.

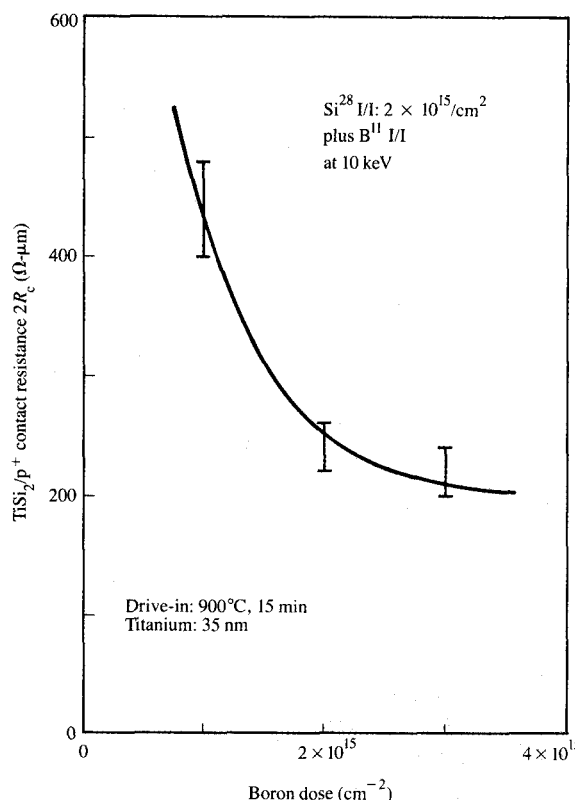


Figure 5

Measured TiSi_2/p^+ contact resistance, $2R_c$, as a function of implanted boron dose. Same titanium thickness, 35 nm, is used for all cases.

little temperature dependence is observed in both cases from 300 K to 77 K. This shows that the current transport mechanism at the TiSi_2/Si interface is dominated by tunneling injections for such high source-drain doping concentrations ($\approx 1 \times 10^{20}/\text{cm}^3$) [7]. In general, the TiSi_2/n^+ contact resistivity is about a factor of 3 lower than that of TiSi_2/p^+ . This could be due to the effective-mass difference between electrons and holes, since TiSi_2 has a near-midgap work function which exhibits the same barrier height to both n-type and p-type silicon.

3. Effects of additional implants into titanium

It was pointed out in Section 2 that there is an upper limit on the titanium thickness for a given junction depth. In some circuit applications, it may be desirable to have a lower TiSi_2 sheet resistance that requires a thicker titanium film than allowed in a standard process. Or, conversely, when the source-drain depth is further scaled down to 0.1 μm or less, the conflicting requirements of a very thin silicide and a low

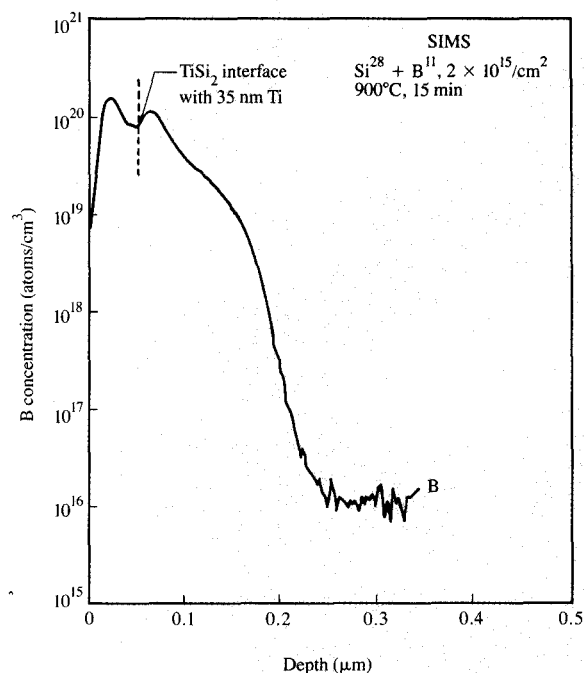


Figure 6

SIMS boron profile for the case of medium dose in Figure 5. The dotted line indicates the projected TiSi_2/Si interface.

sheet resistance at the same time may be difficult to satisfy. In order to overcome this problem, an unconventional process has been investigated in which additional dopants (arsenic or boron) are implanted into a thicker titanium film prior to silicide formation. This saturates the TiSi_2 with n- or p-type dopants so that a thin layer diffuses out during the subsequent anneal to keep the interface doping concentration high and, therefore, the contact resistance low. Furthermore, a serious concern in a conventional TiSi_2 process is the possibility of silicide-induced source-drain leakage [8] at the isolation edge shown in Figure 1. The leakage may occur as a result of over-etching the field oxide after source-drain implants and before titanium deposition. This problem is also solved by the implanted-titanium technique, since the out-diffused dopants are always conformal to the TiSi_2/Si interface to prevent silicide penetration of the junction.

The SIMS profiles of arsenic implanted into titanium are shown in Figure 8. The profile in silicon is taken after the silicide is formed, annealed, and stripped. The inset shows the as-implanted arsenic profile in the presence of titanium film. For these samples, the n^+ source-drain implant before titanium deposition has been skipped. It is clear that

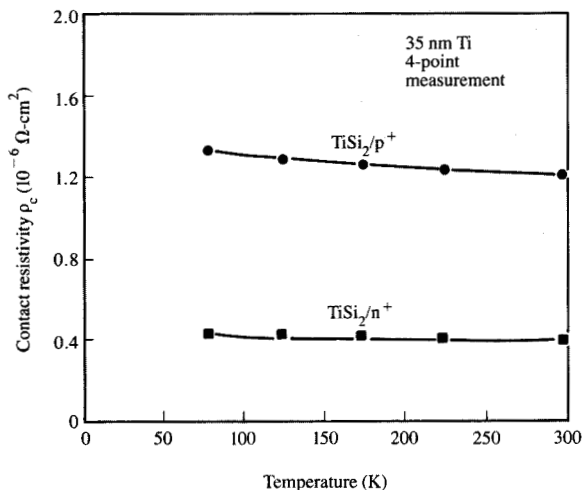


Figure 7

Measured specific contact resistivities from TiSi₂ to n⁺ and p⁺ diffusions as functions of temperature.

although the as-implanted arsenic concentration is very low at the projected TiSi₂/Si interface, a thin layer of high-concentration arsenic has diffused into silicon after silicide formation and anneal. In fact, the final arsenic concentration at the interface is probably much higher than that indicated in Figure 8, which is limited by the SIMS resolution capability.

The effect of the arsenic implant into titanium on the contact resistance is shown by the isolated point in Figure 2. In this case, an arsenic source-drain implant dose of $8 \times 10^{14}/\text{cm}^2$ is used with 60-nm-thick titanium, which would normally result in a very high contact resistance. However, with an additional arsenic implant dose of $4 \times 10^{15}/\text{cm}^2$ into titanium, the contact resistance is kept below $400 \Omega\text{-}\mu\text{m}$. Care must be exercised in the choice of arsenic dose. If too many arsenic ions ($>6 \times 10^{15}/\text{cm}^2$) are implanted into titanium, they may retard the transformation of TiSi₂ into its low-resistivity phase during the final 800°C anneal.

The reverse leakage currents of silicided n⁺/p gated diodes with and without implant into titanium are shown in Figure 9. Very high leakage current is observed without the extra implant. The current dependence on the gate bias indicates that the leakage is dominated by junction perimeters, i.e., due to TiSi₂ penetration at the isolation edge. The leakage current improves by several orders of magnitude with the additional arsenic implant into titanium. In fact, reasonably low leakage current is obtained even if the initial source-drain implant is omitted.

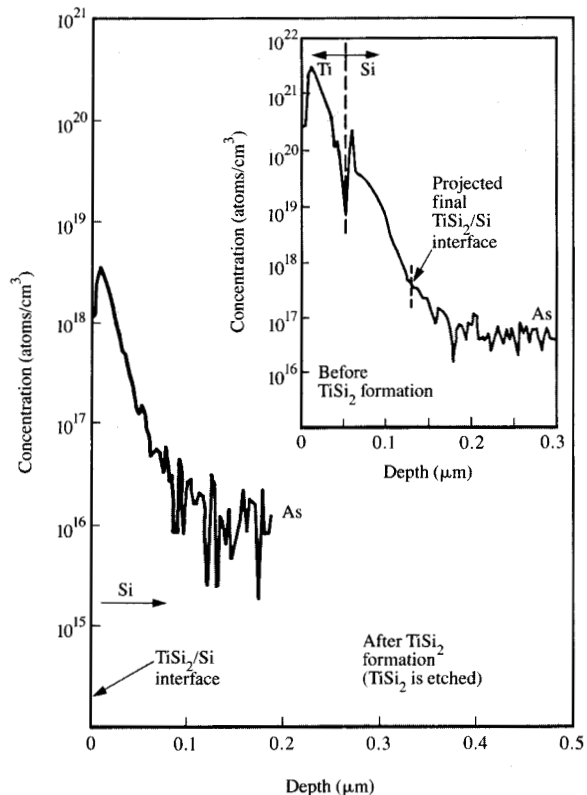


Figure 8

SIMS profiles of arsenic implanted into titanium and out-diffused into silicon after an 800°C silicide anneal. The insert shows the as-implanted arsenic profile.

Similar experiments have been carried out for p-channel devices with an additional $1 \times 10^{16}/\text{cm}^2$ boron implant into 50-nm-thick titanium. The leakage current of a p⁺/n diode with the extra implant is again much lower than without the implant, as shown in Figure 10. However, the TiSi₂/p⁺ contact resistance does not improve significantly with the second boron implant. This is because boron tends to react with titanium and only a small fraction of boron diffuses into silicon. Another factor is that the initial source-drain boron profile is relatively broad (Figure 6) so that the interface concentration remains high even for a slightly thicker titanium film. Contrary to the n⁺ case, no adverse effect on TiSi₂ sheet resistance is observed due to boron ions implanted into titanium.

4. Conclusion

In summary, the contact resistance of TiSi₂ to n⁺/p⁺ diffusions is studied for a variety of junction profiles

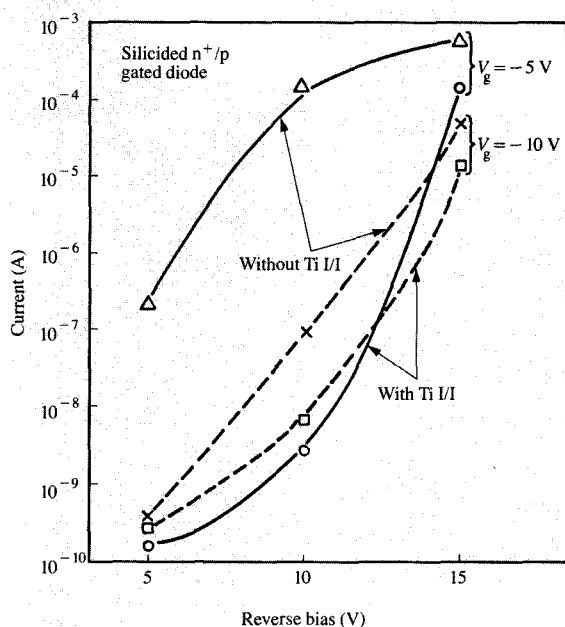


Figure 9

Gated-diode leakage current for n^+ diffusion versus reverse bias voltage with and without an additional arsenic implant into titanium. The diode perimeter region is accumulated at a more negative gate bias (-10 V).

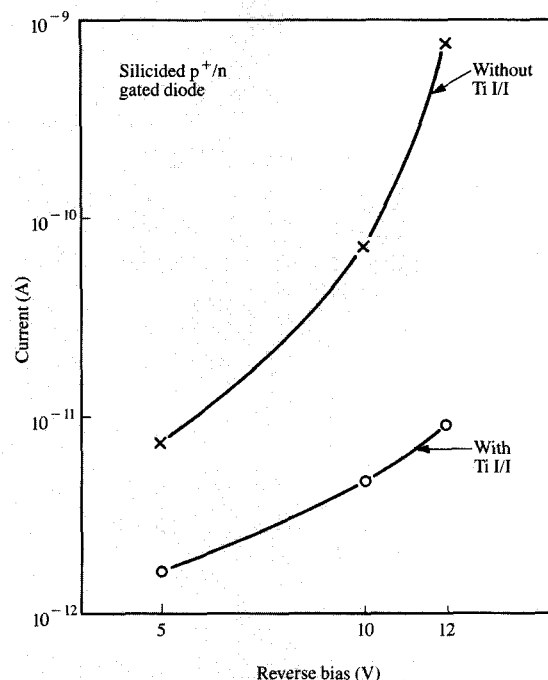


Figure 10

Gated-diode leakage current for p^+ diffusion versus reverse bias voltage with and without an additional boron implant into titanium.

applicable to submicron CMOS technology. Although very low source-drain sheet resistance is obtained with the silicide process, it is important to keep the TiSi_2/Si interface doping above $1 \times 10^{20}/\text{cm}^3$ to avoid high contact resistance. A significant degradation of FET transconductance can occur if excessive amounts of silicon and dopants are consumed in a standard TiSi_2 process. If a slightly higher sheet resistance can be accepted, the titanium thickness should be reduced as the source-drain depths are scaled down.

A thicker titanium film than normally allowed can be used to obtain a lower TiSi_2 sheet resistance if additional dopants are implanted into the titanium before silicide formation. This causes a thin layer of dopants (arsenic or boron) to diffuse into the silicon during the subsequent silicide anneal. Such a dopant layer is conformal to the TiSi_2/Si boundary so as to keep the interface concentration high. It is shown that both the contact resistance (for the arsenic case) and the leakage current at junction-isolation perimeters are reduced significantly by this method. Although extra masks are needed to implement such an implanted-titanium technique in a CMOS process, it is more extendable to sub-half-micron-range technologies with even shallower source-drain junctions and more stringent contact-resistance requirements.

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Yuan Taur IBM Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598. Dr. Taur joined IBM Yorktown as a Research staff member in the Silicon Technology Department in 1981. He received his B.S. degree in physics from National Taiwan University, Taipei, Taiwan, in 1967, and the Ph.D. degree in physics from the University of California, Berkeley, in 1974. From 1981 to 1984, Dr. Taur worked on an advanced one-micron CMOS process which demonstrated retrograde n-well, self-aligned titanium silicide, and the use of thin epi to eliminate latchup. He is currently manager of MOSFET technology, responsible for advanced CMOS process development.

Bijan Davari IBM Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598. Dr. Davari joined IBM Research in Yorktown Heights in March 1984 as a member of the MOS technology group. He is currently involved with sub-half-micron CMOS research, with particular interests in the isolation, gate, junction technology and the integrated process. He received his B.S. degree in electrical engineering in 1977 from Arya-Mehr University of Technology, Tehran, Iran, and the M.S. and Ph.D. degrees in electrical engineering in 1984 from Rensselaer Polytechnic Institute, Troy, New York. His thesis work included the introduction and development of nondestructive semiconductor characterization techniques using surface acoustic waves and the investigation of GaAs MIS structures. Dr. Davari is a member of the Electrochemical Society, the Institute of Electrical and Electronics Engineers, and Sigma Xi.

Dan Moy IBM Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598. Dr. Moy is currently a staff engineer in the Silicon Science and Technology Department at Yorktown Heights. He joined IBM in his current position in 1985, and has been engaged in the research and development of silicide films for VLSI semiconductor applications. From 1983 to 1985, he worked at Intel Corporation in San Jose, California, on the characterization of thin films principally by auger electron spectroscopy and secondary ion mass spectrometry. He received the B.S. degree in physics from the Massachusetts Institute of Technology, Cambridge, in 1978, and the M.S. and Ph.D. degrees in solid state physics from the University of Illinois, Urbana, in 1981 and 1983, respectively. Dr. Moy is a member of the American Vacuum Society and the Materials Research Society.

Jack Yuan-Chen Sun IBM Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598. Dr. Sun is currently the manager of Oxidation, Diffusion, and CVD in the Advanced Silicon Technology Department. He joined IBM Yorktown in 1983 as a Research staff member. Dr. Sun received his B.S.E.E. degree from National Taiwan University, Taipei, Taiwan, in 1975 and the M.S. and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana, in 1979 and 1983, respectively. He was a Rotary International Graduate Fellow from 1977 to 1978 and an IBM Predoctoral Fellow from 1980 to 1981. Dr. Sun is a member of the American Physical Society, the Institute of Electrical and Electronics Engineers, and Phi Kappa Phi.

Chung-Yu Ting IBM Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598. Dr. Ting received his Ph.D. from Harvard University, Cambridge, Massachusetts. He joined IBM as a staff engineer in East Fishkill in 1968, working on IC process development, and was promoted to advisory engineer in 1971, becoming a manager in 1974. In 1976, he moved to IBM Research at Yorktown Heights as a manager of a package group in the Josephson project. In 1979, he transferred to silicon technology, managing a group in thin-film metallurgy and interconnecting. In March 1986 he was promoted to his current position as a second-level manager in Manufacturing Research. Dr. Ting is currently in charge of Materials Interaction Technology as part of Process Technology in Manufacturing Research, interacting with various IBM manufacturing sites providing new materials and technologies through research projects and technology transfer. Areas of particular interest are material joining, thin-film interfaces and corrosion, and laser applications.