Electrical and microstructural investigation of polysilicon emitter contacts for high-performance bipolar VLSI

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Key electrical characteristics of polysilicon emitter contacts in bipolar transistors, such as contact resistance and recombination velocity, are extremely sensitive to the microstructure of the polysilicon/single-crystal silicon interface. In this study, we correlated the microstructural and electrical characteristics of this interface by performing cross-sectional transmission electron microscopy (XTEM) on *actual* transistors on the same chip where ring-oscillator speeds were measured. The base current and emitter resistance of the fastest devices approached values typical of single-crystal silicon emitters. Interpretation of these electrical data and of the SIMS impurity profile indicates that significant restructuring of the polysilicon/single-crystal interface had taken place. This conclusion was indeed confirmed by the XTEM results. Although the low-current performance was degraded because of higher junction capacitances, the high-current switching speed was improved because of the minimal emitter contact resistance. Since the current gain was sufficiently high and very uniform, it is concluded from this work that minimization of both junction depth and contact resistance is the most important design consideration for high-performance submicron transistors, rather than maximization of the gain enhancement of the polysilicon/single-crystal interface.

Introduction

The maximum speed (frequency) at which bipolar transistor circuits can operate is largely limited by base resistance and base-emitter diffusion capacitance ($C_d = G_m \times \tau_F$, the product of transconductance and transit time). Shorter transit time can be obtained by a thinner base and shallower emitter, without compromising controllability. Scaling in the

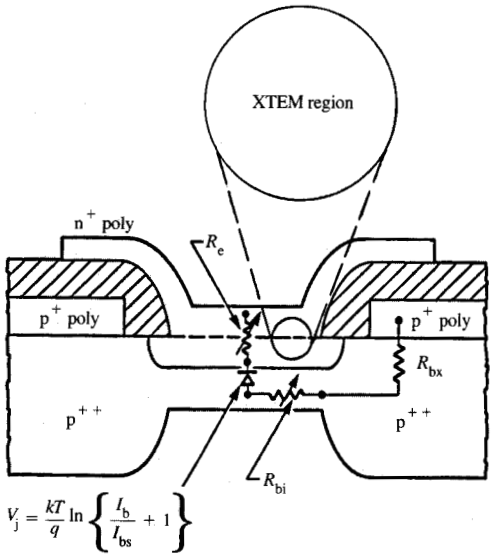

Figure 1

Schematic cross section of self-aligned double-polysilicon bipolar transistor.

Table 1 Transistor parameters.

Emitter area	$A_E \simeq 10\ \mu m^2$		
Emitter anneal	*800°C*	*900°C*	
J_{cs}	7.2×10^{-19}	8.3×10^{-19}	$A/\mu m^2$
J_{bs}	1.6×10^{-21}	6.6×10^{-21}	$A/\mu m^2$
V_{CE_0}	6.0	5.5	V
V_{BE_0}	5.3	3.5	V
ρ_{bi}	5.6 ± 1.2	6.1 ± 0.17	kΩ/□
R_{bx}	110	85	Ω
R_e (at 2 mA)	20	5	Ω
C_{be}	3.9	3.7	$fF/\mu m^2$
C_{bc}	0.48	1.1	$fF/\mu m^2$
C_{cs} (area)	0.14	0.13	$fF/\mu m^2$
C_{cs} (perimeter)	4.0	3.9	$fF/\mu m$
f_T (at 4 mA)	5	6.2	GHz

Collector saturation current density	J_{cs}
Base saturation current density	J_{bs}
Collector-emitter punchthrough voltage	V_{CE_0}
Base-emitter breakdown voltage	V_{BE_0}
Intrinsic base sheet resistance	ρ_{bi}
Extrinsic base resistance	R_{bx}
Emitter resistance (at 2 mA)	R_e
Base-emitter junction capacitance	C_{be}
Base-collector junction capacitance	C_{bc}
Collector-substrate capacitance	C_{cs} (area)
Collector-substrate capacitance	C_{cs} (perimeter)
Transit frequency	f_T (at 4 mA)

lateral dimension also requires a shallow base-emitter junction. When only the emitter *width* is reduced, the contribution of the lateral sidewall junction can degrade high-frequency performance. However, reducing the base-emitter junction *depth* in conventional metal-contacted transistors causes the base current to be unacceptably high and very sensitive to the contact properties. Polysilicon emitter contacts significantly improve bipolar device performance, because they produce a highly abrupt, shallow base-emitter profile without a reduction in current gain since the metal contact is moved away from the junction [1].

By using polysilicon both as the contact and as the diffusion source for the emitter, very shallow, highly abrupt junctions can be obtained by limiting the outdiffusion of As into the single-crystal silicon. In addition, the reduced mobility in the polysilicon [2,3] and the presence of an interfacial tunneling barrier [4] at the polysilicon-monosilicon interface result in a base current density (holes for an npn transistor) that is reduced by a factor of 3 or more. The polysilicon/monocrystalline silicon interface, however, not only acts as a barrier to hole transport (base current), but also increases the resistance for electrons (emitter current) [5,6]. Since the largest current density in the device passes through the emitter contact, the specific contact resistivity must be kept as low as possible to prevent a degradation in transconductance. Although the exact electrical properties of the polysilicon/silicon interface are still under investigation, it is known that the interface structure changes significantly as a result of high-temperature annealing, and that these changes are enhanced at high doping levels [7–11]. Specifically, the "native" interface oxide layer "balls up" and the polysilicon tends to realign to the underlying substrate, thereby extending the single-crystal emitter up into the polysilicon layer. This type of structural change has been expected to result in the following trade-off: Although a lower emitter resistance can be obtained by a higher-temperature treatment and/or higher doping level, the junction depth and base current would then be increased.

In order to determine the potential performance trade-off between base current and emitter resistance, this paper compares the structural *and* electrical aspects of advanced-technology bipolar transistors which differ only in the annealing treatment of the polysilicon emitter contact. In the following sections, the sample preparation is described, followed by the dc electrical transistor characteristics. Next, XTEM results of the polysilicon/single-crystal silicon interface are presented, showing significant restructuring of the poly-emitter interface for the devices with the lowest emitter resistance. In the final section, switching performance is addressed. Measurements on ring-oscillators show a strong correlation between speed and low emitter contact resistance. Simulation is used to analyze the increasing importance of low contact resistance for high-speed, submicron bipolar transistors.

Sample preparation

The devices used in our experiment were self-aligned double-polysilicon bipolar transistors, whose schematic cross section is shown in **Figure 1**. Relaxed geometries (2.5 μm) were used, and isolation was achieved by a combination of recessed oxide isolation and p^+ channel-stop implantation. The epitaxial layer was kept thin to prevent high-current degradation due to basewidening [12]. The base contact was *in situ*, boron-doped polysilicon with a (measured) thickness of 0.26 μm. The emitter opening was etched using a selective chemical wet etch, so as to prevent surface contamination from reactive ion etching (RIE) that might alter the condition of the emitter surface. The base contact was diffused into the silicon to provide a self-aligned connection to the intrinsic device. After formation of an oxide sidewall on the base contact polysilicon, *in situ*, arsenic-doped polysilicon was deposited at 650°C in an AM 704 reactor, using N_2 as the carrier gas. The emitter surface was given a 4-s buffered hydrofluoric acid (BHF) cleaning prior to this deposition to minimize any residual native oxide on the surface. The as-deposited grain size of the emitter polysilicon was measured by TEM to be approximately 20 nm. The arsenic content was measured by Rutherford backscattering spectroscopy (RBS) to be about 3 atomic percent, resulting in a sheet resistance after annealing of 1–3 kΩ/□. Two different emitter anneals were used: 900°C for 10 min or 800°C for 45 min. The second anneal condition was designed to result in approximately the same integrated base doping while minimizing the base-emitter junction depth, as is discussed later. Metallization consisted of a Ti/Al/Si sandwich, which was annealed in forming gas at 400°C.

Transistor dc electrical characteristics

The results of extensive dc and ac characterizations are summarized in **Table 1**. From large transistors [see **Figure 2(a)**] it was found that the base current for the devices annealed at 800°C was lower than that of the devices annealed at 900°C by about a factor of two. The collector currents were approximately the same, indicating that the integrated base charge was indeed equivalent for both types of devices. This was confirmed by the base-emitter junction capacitance measurements shown in **Figure 3**, which were in good agreement with secondary ion mass spectroscopy (SIMS) profiles taken on monitor wafers. The peak doping was slightly higher for the lower-temperature anneal, but the base thickness was estimated to be about the same. These observations were further supported by measurements of the sheet resistance of the active base of 6 and 5 kΩ/□, for the high- and low-temperature anneals, respectively (see Table 1).

The I–V curves for small devices ($A_E \leq 10\ \mu m^2$) are shown in **Figure 2(b)**. The curves indicate that the series resistance was substantially higher for the device given the 800°C anneal. In order to assess whether this was due to base or emitter resistance, the method of Ning [13] was used. In this approach, the total series voltage drop at high currents is extracted by extrapolating the ideal exponential behavior of the base current $I_b\,(V_j)$ versus the junction voltage V_j to high currents. Then, subtracting this from the base current $I_b\,(V_{BE})$ versus the emitter voltage V_{BE}, the total series voltage drop is

$$\Delta V \equiv V_{BE} - V_j = R_e(I_c + I_b) + (R_{bi} + R_{bx})I_b, \qquad (1)$$

where the extrinsic base resistance R_{bx} is constant and associated with the contact area, and the intrinsic base resistance R_{bi} is modulated by the injection level in the active

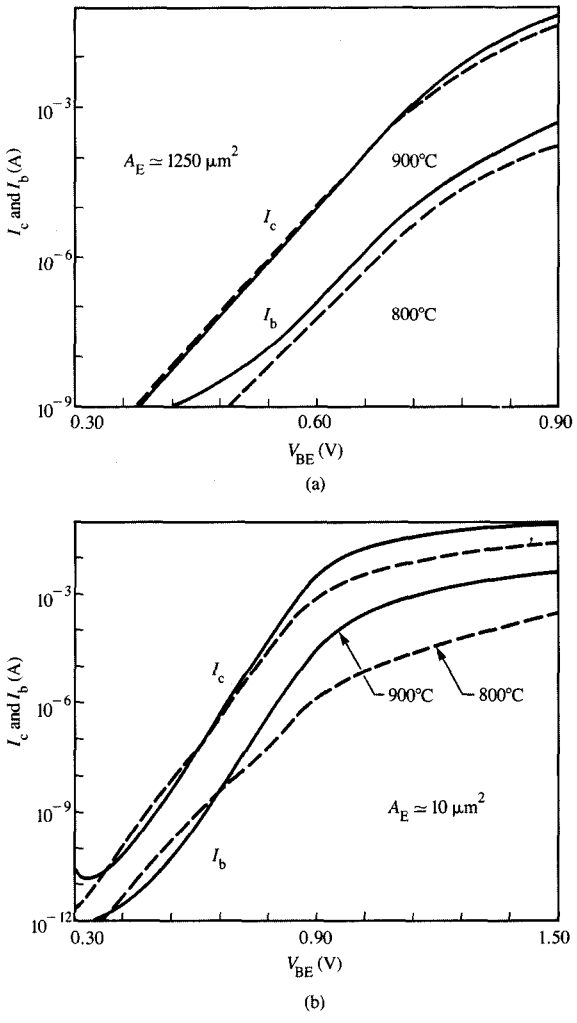

Figure 2

I_c, I_b versus V_{BE} curves for (a) large devices: $A_E \simeq 1200\ \mu m^2$; (b) small devices: $A_E \simeq 10\ \mu m^2$.

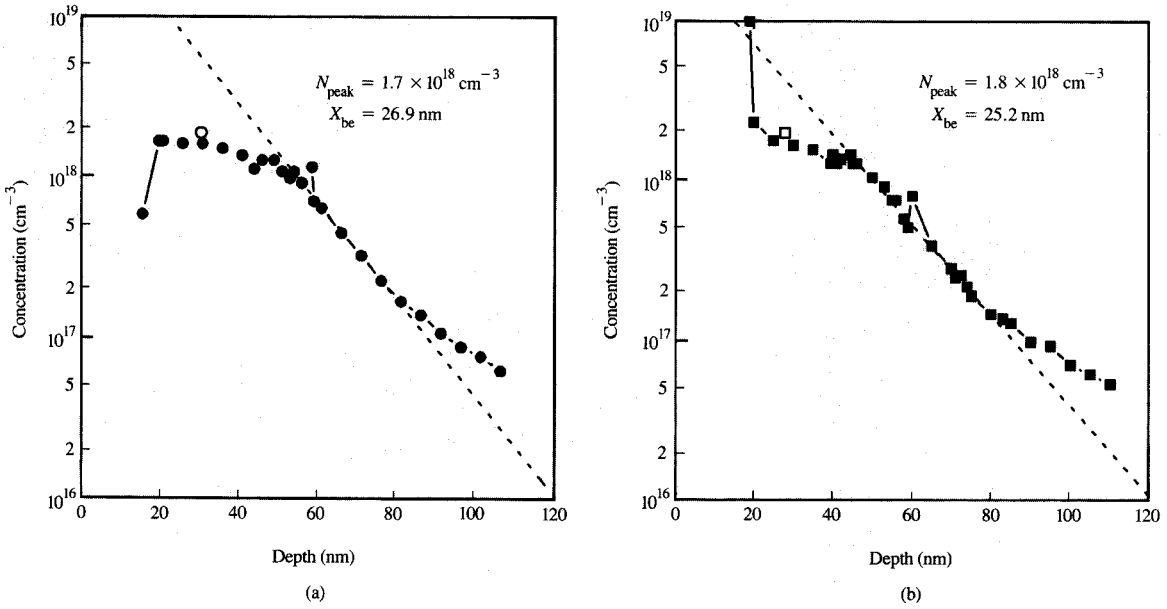

Figure 3

Base doping profile extracted from *C-V* measurement of the base-emitter junction. X_{be} is the extracted base-emitter junction width at zero bias. The base profiles are evidently nearly equal for both emitter anneals: (a) 900°C; (b) 800°C.

device. Since $I_c = \beta I_b$, the base resistances can be separated from the emitter resistance by dividing ΔV by I_c,

$$\frac{\Delta V}{I_c} = R_{tot} = R_e\left(1 + \frac{1}{\beta}\right) + (R_{bi} + R_{bx})\frac{1}{\beta}. \quad (2)$$

In order to uniquely determine R_{bx}, the assumption was made in [13] that R_{bi}/β is small and approximately constant as a function of collector current. In typical devices, however, the intrinsic base resistance produces a lateral voltage drop, which "crowds" the current injection toward the perimeter of the base-emitter junction because the largest forward bias is there. When the intrinsic base resistance is large (because of a high sheet resistivity or because of layout) this crowding reduces the effective resistance (without a degradation in current gain) so that the lateral voltage is overestimated when the low-current value of R_{bi} is used. Further complications arise from the reduction in current gain that results from high-injection effects; this had led to confusion about the interpretation of nonohmic emitter resistance [14]. An extensive treatment of the impact of current crowding on the extraction of base and emitter resistance can be found in [15].

For the devices of this study annealed at 800°C, the crowding effect of *intrinsic* base resistance is negligible, however: The lateral voltage drop never exceeds kT/q because of the high β and low base sheet resistance. The extrinsic base component from the slope in **Figure 4** having been determined, the net voltage drop across the emitter contact can then be extracted. In **Figure 5** it is shown that the emitter current depends in a sine-hyperbolic manner on the voltage across the polysilicon/single-crystal silicon interface. Such behavior is expected when transport through the contact is barrier-limited [16], as has been verified elsewhere [17]. The contribution of the metal-to-polysilicon contact resistance was estimated at 3 Ω, which gave very good agreement for the sine-hyperbolic fit. (The quoted resistance data were measured on bonded devices to minimize probe and cable parasitics.) This is also consistent with the emitter resistance measured on devices given the 900°C emitter anneal. For such 900°C devices, the extracted emitter resistance is ohmic and extremely small (≃5 Ω). Due to the low intrinsic base resistance, little crowding takes place, so that R_{bi} and β degrade at the same rate and their ratio remains constant at $R_{bi}/\beta \simeq 2$ Ω. Therefore, most of the emitter resistance can be estimated to be contact resistance between the polysilicon and the metal. Again, this is consistent with the constant component in the total resistance of the 800°C transistor. In addition to the very low resistance of the 900°C anneal, the base current density was a factor of 2 higher than that of the 800°C device and its

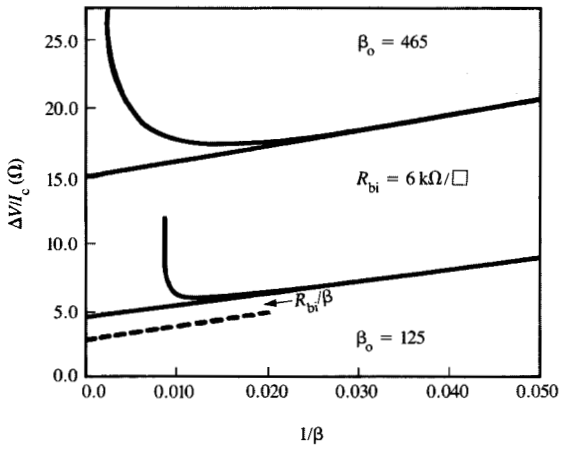

Figure 4

Total series resistance versus inverse β. The slope at low β gives R_{bx}, while R_e is extracted from the intercept. Although there is a slight difference in R_{bx}, the emitter resistance is a factor of 4 or more larger for the 800°C emitter anneal.

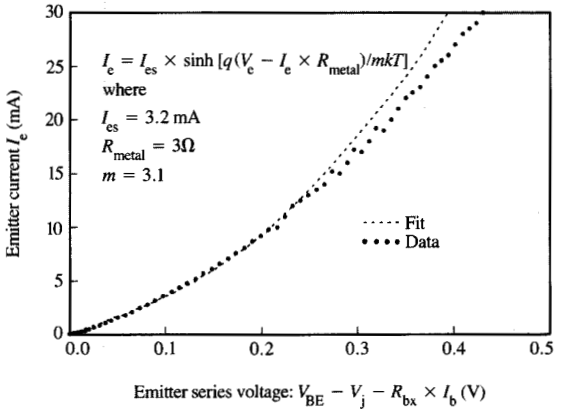

Figure 5

Sine-hyperbolic *I-V* relation of the poly-emitter contact annealed at 800°C. The 900°C transistor showed ohmic behavior.

magnitude (≃1 pA/cm^2) is comparable to values obtained with deep, single-crystal emitters [7]. Despite the higher-temperature anneal, the emitter junction depth was less than 50 nm in these devices (from SIMS). Indeed, simulation of a single-crystal silicon layer with an ideal box-like doping profile results after the same anneal in a shallower but slightly more graded junction compared to a polysilicon diffusion source. This effect has been observed before [18] and is explained by epitaxial regrowth, which moves the fast grain-boundary diffusion sites away from the substrate.

Cross-sectional TEM

The high base-current density, low emitter resistance, and relatively shallow junction depth of the 900°C device mentioned in the previous section all indicate that the effect of the polysilicon/single-crystal interface on the device characteristics is minimal. The very high *in situ* doping level (1×10^{21} cm^{-3} from SIMS), wet-etched emitter opening, and BHF cleaning before polysilicon deposition are favorable conditions for epitaxial realignment of the polysilicon. As shown in [8, 10] and [7, 9, 11], high doping levels reduce the critical temperature for realignment and result in an increase in I_b. Indeed, as shown in **Figure 6**, the base-current density of the emitter annealed at 900°C has reached a value close to what can be expected when the polysilicon is perfectly aligned to form an extended single-crystal emitter. For the other devices shown in Figure 6, which were annealed at higher temperatures or for longer times, it was shown [7]

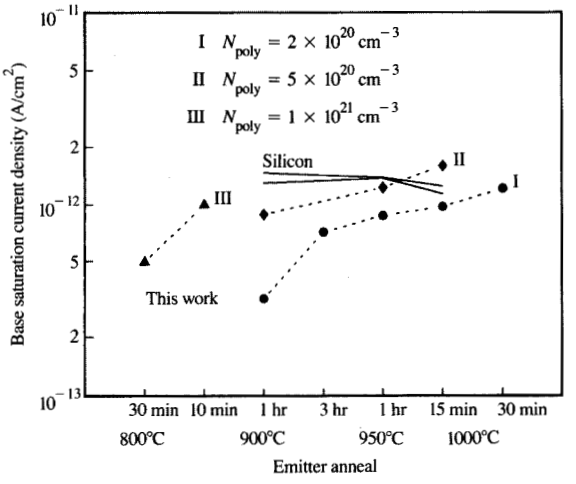

Figure 6

Base current for various emitter annealing conditions. It appears that the "saturation" value of an extended single-crystal emitter is obtained for lower and shorter annealing conditions when the effective doping of the poly (N_{poly} = doping concentration) is increased.

that a noticeable increase in base current occurs when the residual native interface *begins* to break up. Although annealed in an oxygen ambient (shown to favor realignment of boron-doped poly [19]), the low-temperature (900°C)

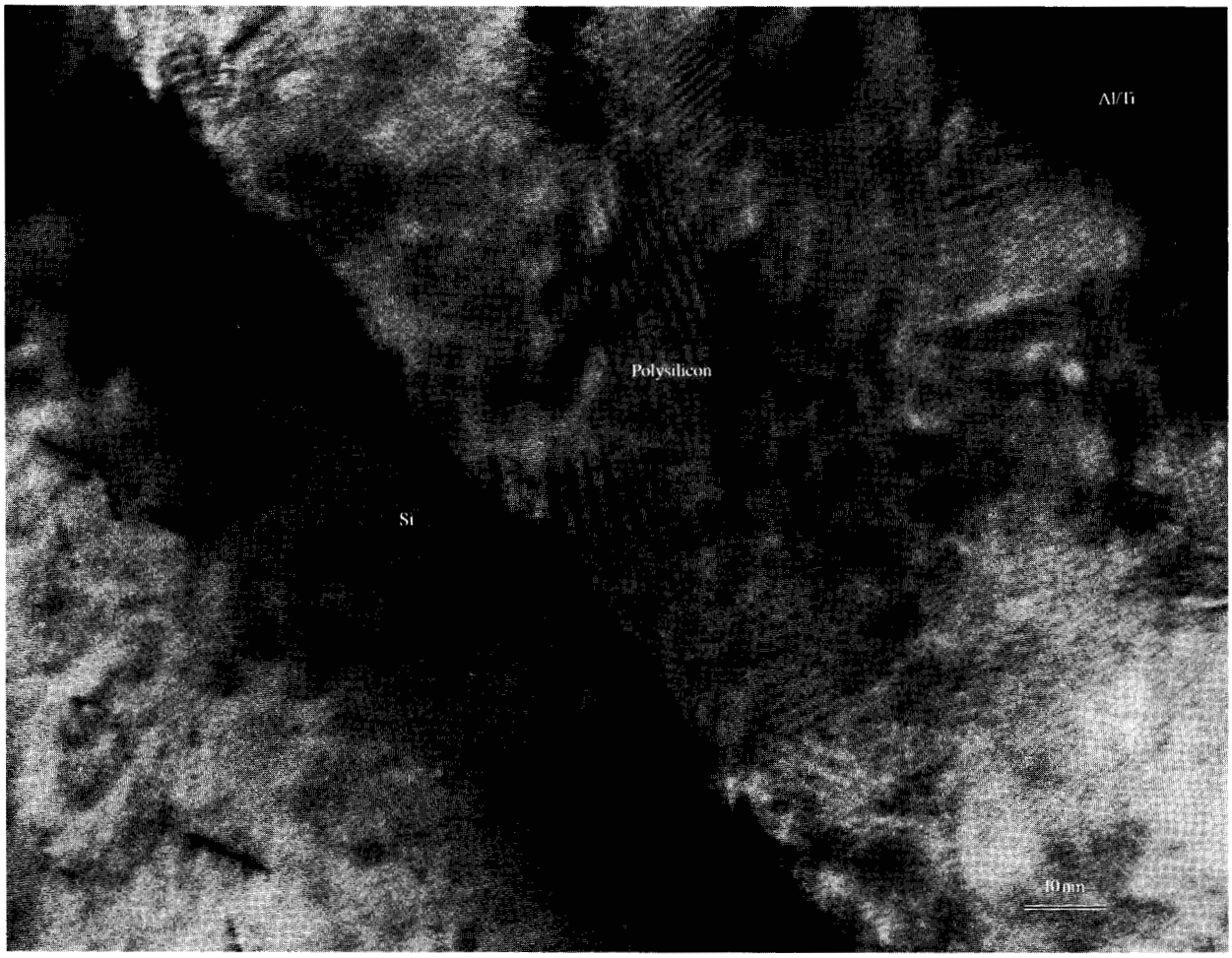

Figure 7(a)

XTEM photograph of the polysilicon/single-crystal interface: (a) Low magnification, showing global features of the polysilicon layer.

emitter anneal was short enough to cause us to question the amount of interface restructuring. To determine whether restructuring had occurred in the devices annealed at 900°C, an *actual* transistor was examined by cross-sectional TEM. The results are shown in **Figures 7(a)** and **7(b)**. The high-magnification lattice image in Figure 7(b) clearly shows realignment at the interface. No evidence is present of any remaining interfacial oxide: Because of the low annealing temperature the oxide might not have "balled" sufficiently to become visible. However, because a lattice image is visible for almost all grains, these polysilicon grains must have aligned to some degree.

Switching performance

The essential device parameters for switching performance, such as the junction capacitances and f_T, are also summarized in Table 1. The extrinsic base capacitance for the 900°C devices was substantially higher because the extrinsic base drive-in was different for the two types of devices. The intrinsic base delay, which was extracted by plotting $1/f_T$ versus $1/I_c$, was equivalent and was not affected by high injection effects at the measured power levels because of the thin epitaxial layer used. The impact on switching performance was addressed by measuring both emitter-coupled logic (ECL) and non-threshold logic (NTL) ring-oscillators. The power delay curves in **Figure 8** show the impact of the principal delay components: The smaller extrinsic base-collector capacitance (shallower junction) for the transistors annealed at 800°C allows faster operation at low power levels, but the larger emitter resistance leads to a considerable increase in delay at higher currents. This high current delay for an NTL circuit is plotted in **Figure 9** versus emitter resistance. Similar results are obtained for ECL circuits. The large spread in delay for the high-resistance data is a result of a wider spread in the dc characteristics of the high-resistance devices. The large variability in resistance is

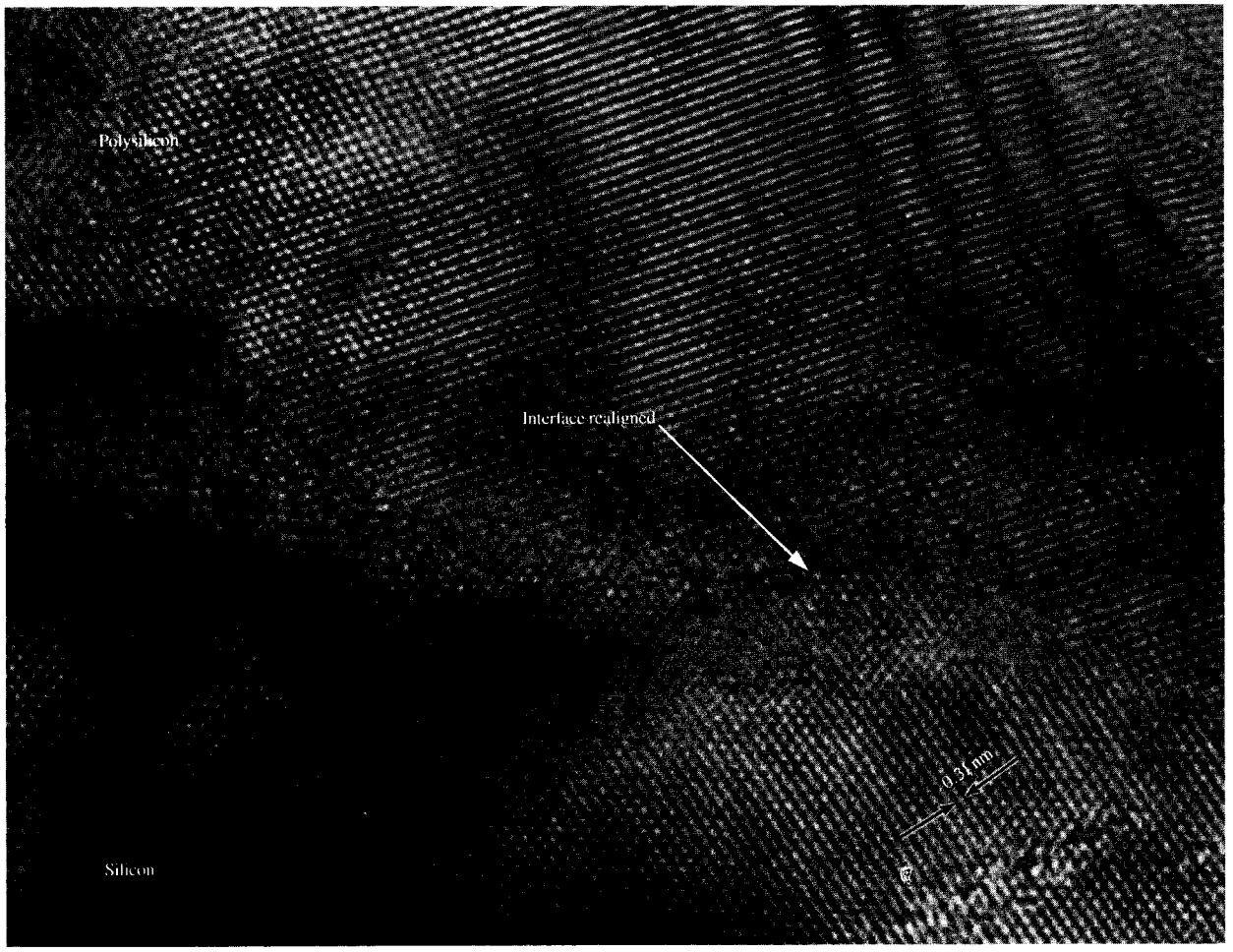

Figure 7(b)

XTEM photograph of the polysilicon/single-crystal interface: (b) Highest magnification–lattice fringes are visible and are clearly continuous through the interface at many places.

actually more of a concern, because that prevents accurate tracking and adds to the noise margin. Although it would be more appropriate to use the resistance averaged over the voltage swing, it is difficult to eliminate measurement-induced disturbances of the waveform to extract the actual voltage-versus-time behavior. Thus, only the resistance for one particular current level is given, as this is not expected to change the observed correlation between resistance and gate delay.

Implications for further scaling

As a result of the use of polysilicon emitter contacts to achieve advanced profiles, circuit performance is now more sensitive to device and contact geometry. An increase in specific emitter contact resistance reduces transconductance and precludes optimum performance at high current densities [20]. In **Figure 10**, calculation results demonstrate the effect of high contact resistance on ECL gate delay. Starting with zero contact resistance, the emitter length was adjusted to obtain maximum speed for a given minimum emitter width. As the specific contact resistivity increased, the emitter length was adjusted to keep the voltage drop across the emitter contact below one kT/q. It can be seen that enlarging the contact area results in speed degradation: Even though the length-to-width aspect ratio of the emitter reduces the base resistance, all capacitances increase such that narrow emitters become the slowest. These results indicate that a specific contact resistivity of less than 150–200 Ω-μm^2 is required to take advantage of the high-current-speed potential of emitter widths less than 1.0 μm. Even lower values will be needed for 0.5-μm technologies. Even if the effect of the polysilicon/single-crystal interface were negligible, a contact resistivity below 100 Ω-μm^2 would be difficult to obtain. For example, this would require an

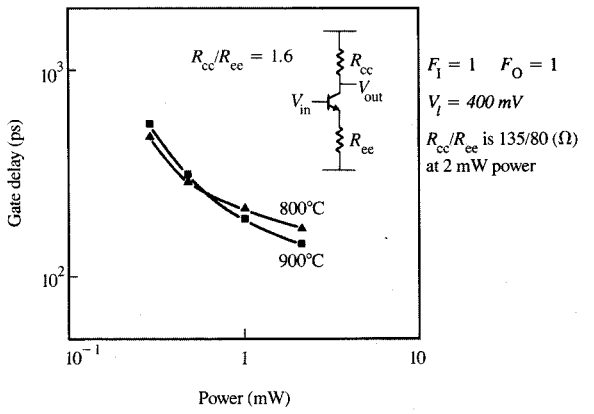

Figure 8

Measured power-delay curves for NTL circuits. (F_I and F_O are the fan-in and fan-out for the circuit, respectively.)

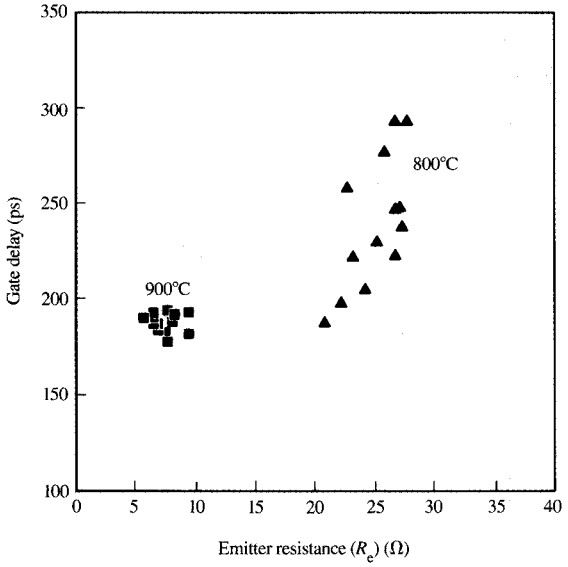

Figure 9

NTL delay versus emitter resistance. Delay was measured at constant current (logic swing varied from 0.35–0.43 V). Total power was approximately 1.1 mW per gate.

active doping concentration of 4×10^{20} cm^{-3} for an n^+–Si–Al contact potential. Because of the clustering of As atoms at lower processing temperatures (and segregation to the grain boundaries in the case of polysilicon), either *in situ*

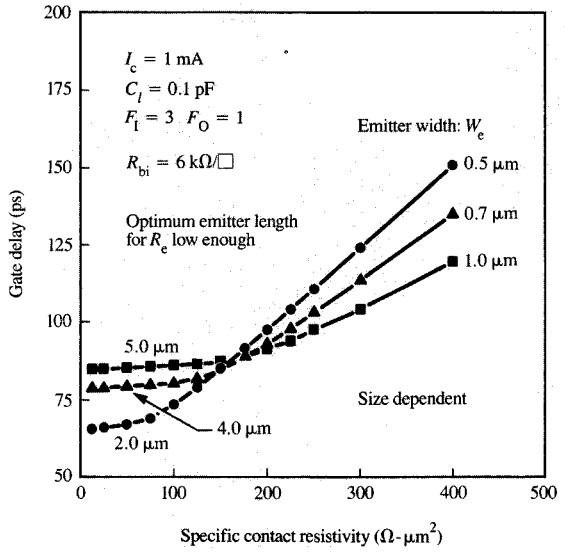

Figure 10

Impact of emitter resistance on delay for scaled devices. The specific contact resistance of the 800°C emitter anneal would be unusable for submicron devices.

doping or 1000°C rapid thermal anneals are required to obtain such low contact resistivities. Moreover, the data of Figure 10 clearly indicate that the specific contact resistance of 200 Ω-μm^2 (see Table 1) attained by annealing at 800°C precludes the use of this annealing temperature for the fabrication of submicron devices. In any case, very tight control is needed to prevent emitter resistance variations from determining the minimum usable emitter area in circuit design.

Conclusions

From both dc and ac electrical characteristics, as well as XTEM analysis, we conclude that the microstructure of highly As-doped (1×10^{21} cm^{-3}) polysilicon, annealed at temperatures as low as 900°C, results in emitter electrical characteristics resembling those of extended single-crystal silicon. The base current in these recrystallized polysilicon emitters was higher in comparison with a more-or-less continuous polysilicon/single-crystal interface, but appears tolerable for circuit design, in particular because of the smaller spread in device characteristics. The better reproducibility of the emitter as a diffusion source with lower and more tightly controlled contact resistance leads to greater reliability and superior speed performance in high-current switching applications. Simulation shows that increasingly lower specific contact resistivity is demanded at design rules for smaller circuits. Any residual effects of the

native oxide between the polysilicon/single-crystal silicon interface are expected to be intolerable for submicron, high-performance digital devices. In order to obtain the very highly doped, abrupt emitter profiles of the future, other alternatives for emitter doping and dopant activation have to be explored.

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