Contact metallurgy development for VLSI logic

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The criteria involved with the choice of an ohmic contact material for VLSI logic are discussed. The problems of aluminum penetration encountered with Al metallization and solid-phase epitaxy associated with Al–Si metallization make these interconnect materials incompatible with VLSI technology. The contact resistance characteristics of palladium and platinum silicides were compared to the contact resistance obtained using a titanium contact layer. The contact resistance of palladium silicide increased with extended annealing at 400°C, while the PtSi and Ti contact materials exhibited stable contact resistance under these conditions. A Ti/Al–Cu/Si process which is compatible with a lift-off patterning technique and partial coverage of contacts is described. Rutherford backscattering results indicate that copper and silicon additions to the aluminum metallization retard the Ti–Al reaction. SIMS data show that silicon in Ti/Al–Cu/Si films redistributes during heat treatment, accumulating at the Ti/Al–Cu interface.

Introduction

Successful implementation of an ohmic contact material within a manufacturing environment requires that a number of very diverse criteria be met. The choice of materials for a contact layer usually begins with an assessment of the requirements for a family of products. There are usually a large number of contact materials which possess suitably low contact resistivities to be considered potential ohmic contact candidates. The selection and development process then consists of understanding the process, tooling, and manufacturing constraints associated with each material. Process-related questions such as junction penetration effects and materials interactions with the interconnect must be answered. In addition, the annealing requirements and limitations of each contact and interconnect system must be determined.

Tooling issues such as availability, cost, throughput, and defect density are an important and often neglected part of the selection process. Finally and most importantly, various manufacturability issues must be weighed by the development team. Process simplicity is of paramount importance in a manufacturing environment; therefore, schemes which can combine or eliminate process steps are worth pursuing. For example, the question of whether the interconnect itself is a suitable contact material should certainly be asked. The other necessary ingredient for manufacturability is selection of materials and processes which are relatively immune from defects and easy to control in a manufacturing environment.

Process and design interactions

Junction penetration must certainly be considered in evaluating the suitability of any interconnect and contact metallurgy system. Most VLSI logic technologies utilize junctions which are less than 500 nm in depth and are therefore not compatible with an Al or Al–Cu metallization. Silicon diffusion from the contact into the adjacent Al interconnect occurs during post-deposition heat treatments

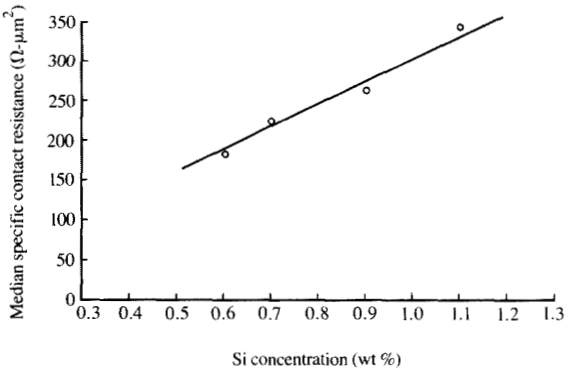

Figure 1

Specific contact resistance as a function of silicon content for Al–Si interconnect metallurgies.

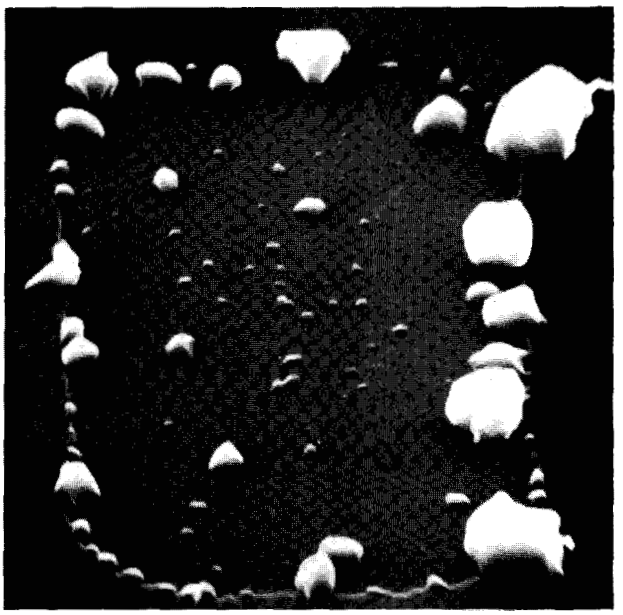

Figure 2

Scanning electron micrograph of contact with Si epitaxial growth.

to satisfy Si solubility requirements in Al. The resultant Al penetration of the contact region causes either high leakage or shorting between the diffusion and substrate.

The conventional solution to this problem is the addition of Si to the Al metallurgy. Indeed, an Al–Si metallurgy has become the industry standard in the past several years. However, Al–Si is also not without its problems. In order to guarantee that junction penetration does not occur, an amount of Si in excess of the solubility limit is added to the Al. Typical concentrations in use by the semiconductor industry are 1.0–1.5 weight percent, even though the Al–Si phase diagram indicates that only 0.5 weight percent is needed for post-metallization processing temperatures of 450°C.

This excess Si diffuses to the Al–substrate silicon interface, where a solid-phase epitaxial Si growth occurs on the contacts [1]. The presence of this epitaxial Si film can have a profound effect on contact electrical behavior. Since the layer is growing from an Al solid solution, it becomes doped p-type with Al. For ohmic contacts, resistance problems are exclusively associated with n-type contacts. This observation is consistent with the presence of a p-type epitaxial layer [2].

The volume of Si available for epitaxial growth is determined by the excess Si in the interconnect line within a diffusion distance of the contact. A large volume of Si can be grown, since the diffusion length of Si in Al is approximately 40 μm for a 400°C, one-hour heat treatment [3]. Electrical measurements indicate that some minimal thickness of epitaxial layer covers most of the contact. **Figure 1** plots the median contact resistance for an n-type diffusion versus weight percent Si in the Al interconnect. As expected, the lower the amount of excess Si in the Al film, the thinner the epitaxial layer and the lower the contact resistance.

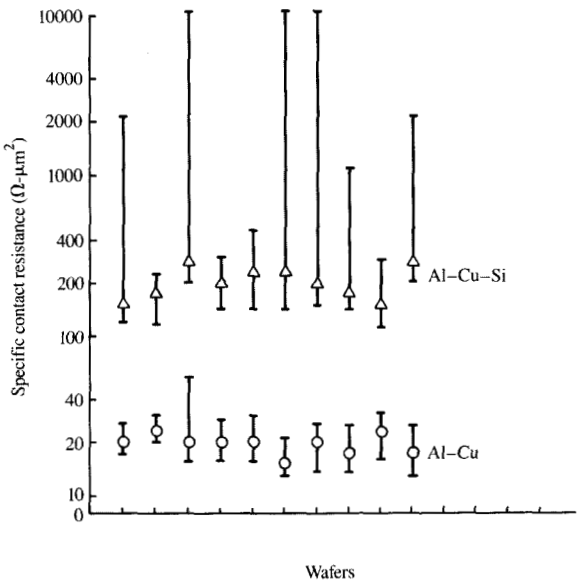

Figure 3

Median and range of specific contact resistance (to n^+ diffusions) for lots split between Al–Cu–Si and Al–Cu metallizations.

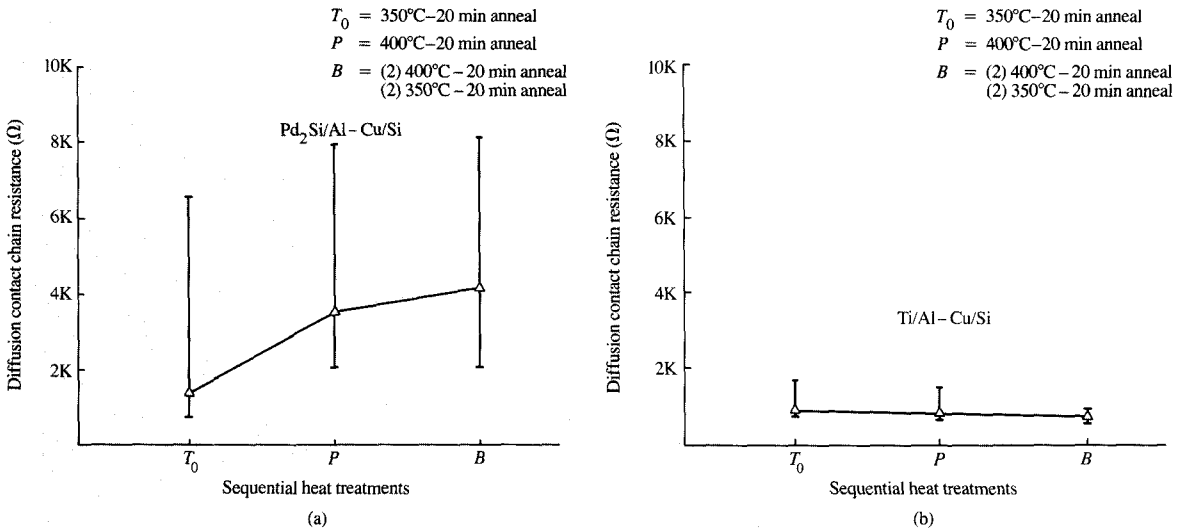

Figure 4

Diffusion contact chain resistance as a function of heat treatment for (a) Pd_2Si and (b) Ti contact layers with Al–Cu/Si metallization.

Only the very thickest layers of the epitaxial film can be observed visually, and they normally accumulate in thick layers or mounds around the edge of the contact window because of closer proximity to the Al diffusion source. This normal pattern of Si epitaxial growth is illustrated in the scanning electron micrograph (SEM) in **Figure 2**. The Si growth pattern could lead us to postulate that reduction of Si contact area through either design or process contaminants would result in very thick epitaxial layers and therefore high contact resistance. In fact, this is exactly what is observed. **Figure 3** illustrates the median contact resistance and range of individual wafers in an experiment in which three lots were split between Al–Cu and Al–Cu–Si metallurgies. The diffusions in this study were n-type, doped with As to a concentration of approximately 1×10^{20} atoms/cm^3. The contact resistance measurements were taken on single-contact sites with a four-point probe technique.

It is clear that the Al–Cu–Si metallurgy exhibits high and erratic contact resistance. Failure analysis of the high-resistance contacts showed the presence of process contamination in the contacts. It is interesting that these same resist or oxide contaminants did not cause resistance excursions with the Al–Cu film. The evidence clearly suggests that a Si-doped Al metallurgy is not as forgiving in a manufacturing environment.

The design implications of the contact metallurgy choice primarily revolve around the issue of metal contact area. VLSI trends are causing dramatic decreases in contact size. For example, there has been a fourfold decrease in contact area as photolithography ground rules have gone from 2 μm to 1 μm. In addition, significant improvements in wiring density for logic devices can be achieved if ground rules allowing partial metal coverage of contacts are used. The use of this design leverage causes significantly decreased nominal and worst-case metal contact area. These reduced areas would lead to severe manufacturability problems with a Si-doped Al metallurgy because of the solid-phase epitaxy phenomenon. Clearly, Al-based or Al–Si-based interconnection metallurgies are not compatible with all of the design and manufacturability requirements imposed by a VLSI logic technology.

Contact metallurgy development

The first requirement of a contact material must be resolution of both the Al penetration and solid-phase epitaxy problems associated with Al-based and Al–Si-based interconnection metallurgies, respectively. There is an extensive list of silicides, for example Pd_2Si and PtSi [4], that have been investigated for use as ohmic contacts. Some of these materials are reported to be Si diffusion barriers [5] and therefore should prevent Si solid-phase epitaxy when used with an Al–Si-based metallization. In addition, there are also various transition metals, for example Ti and V, which have been extensively studied and reported to have excellent Si diffusion barrier properties [6, 7].

Discussions of Si diffusion barrier properties are incomplete unless post-metallization processing temperatures and interactions with the interconnect metallurgy are considered. This point is critical because in most cases these

contact materials cease to be Si diffusion barriers when they react with the Al-based interconnect to form various intermetallic compounds [7, 8]. Therefore, a contact material which might be an acceptable Si diffusion barrier when subjected to one hour of 350°C processing might be totally inadequate for a technology which required processing for one hour at 400°C. In fact, this is exactly what is observed with a Pd_2Si contact metallurgy when it is used with an Al–Si-based interconnect.

Another important consideration for any contact material is the underlying metal semiconductor conduction properties. The correct choice for a contact material for low-resistance ohmic contacts depends in large part on the doping level and conductivity type of the semiconductor. For lightly doped semiconductors it is quite important to choose a material with the lowest possible barrier height on that semiconductor [9]. Naturally, it is not possible to choose one material which would result in low-resistance ohmic contacts on both low-doped n- and p-type semiconductors. This has obvious implications for process complexity. Fortunately the doping levels of the diffusions in most logic technologies are quite high. The operative metal-contact conduction mechanism is generally tunneling through the barrier rather than excitation over it, and the effect of metal barrier height is not as predominant [9]. For example, a 0.25-volt difference in barrier height at a doping level of 1×10^{18} atoms/cm^3 has been shown to cause a difference of four orders of magnitude in specific contact resistance. That same barrier height differential causes a difference of only one order of magnitude in specific contact resistance at doping levels of 1×10^{20} atoms/cm^3 [10]. In general, when low-resistance ohmic contacts in both n- and p-type diffusions are required, a barrier height near the center of the band gap (0.55 eV) is desirable.

Silicides have shown greater applicability as discrete contact materials than metal contact barriers. The primary reason for this is process simplicity. An additional photomasking level would be needed to align and etch a metal layer over a contact, while silicides generally are self-aligned to the contact. Metal barriers have a process simplicity advantage only if they can be deposited as part of the interconnection metallurgy, since this would result in the elimination of the entire contact metallization sector. This latter course was the one chosen for this development project.

Titanium was chosen as the contact metal. It is particularly well suited for inclusion in an interconnect. Its barrier height is 0.55 eV [9], making it suitable for contacting both n- and p-type moderate to highly doped junctions. Ti also exhibits excellent adhesion to SiO_2 and Si [11], which is an absolute prerequisite for an interconnect underlayer. The interconnect metallurgy in this study was Ti/Al–Cu/Si. Copper was included in the Al interconnection metallurgy to provide increased electromigration resistance and also to suppress hillock growth. Inclusion of the Si was necessary to suppress Al penetration in partially covered contact regions.

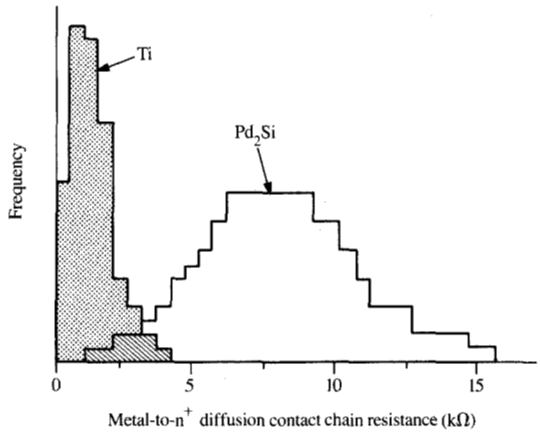

Figure 5

Metal-to-n^+ diffusion contact chain resistance distributions for Pd_2Si and Ti contact layers with Al–Cu/Si metallization.

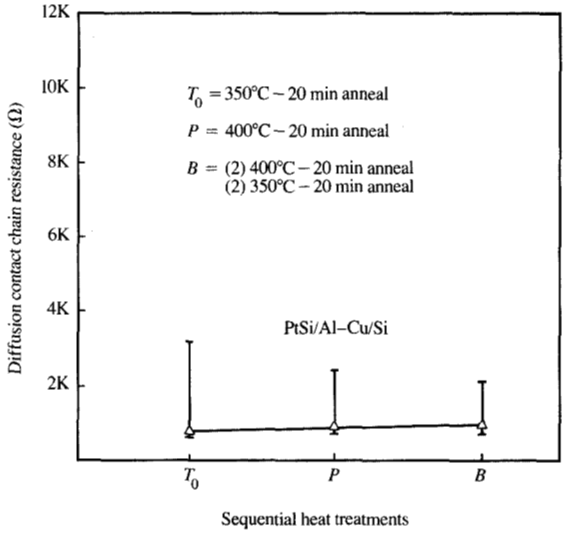

Figure 6

Diffusion contact chain resistance as a function of heat treatment for PtSi contact layers with Al–Cu/Si metallization.

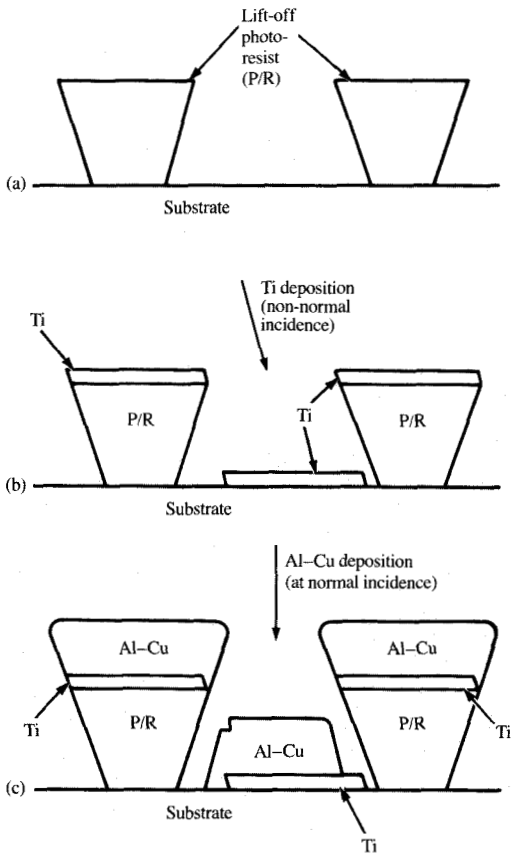

Figure 7

Metallization patterning sequence: (a) after photoresist pattern definition, (b) after Ti evaporation, (c) after Al–Cu evaporation, and (d) Ti/Al–Cu/Si after photoresist lift-off (Si evaporation not shown).

Process description

Lift-off was chosen as the metallization patterning technique for these studies. Although the lift-off technique offers several advantages [12], it restricts the choice of titanium deposition method to evaporation. Titanium thin films have been prepared by resistive evaporation using low-alkali tungsten filaments as support materials. Resistive evaporation is used to avoid potential radiation damage to FETs. Titanium evaporation under a shutter prior to deposition may also be used to getter the vacuum system. The Ti film is deposited at a rate of from 1 to 3 nm/s until a thickness of 100 nm is achieved. This is followed by the Al–Cu interconnect deposition. After Al–Cu deposition and without breaking vacuum, silicon is deposited on the Al–Cu surface in order to prevent Al penetration problems that might result with subsequent heat treatments. The Ti/Al–Cu/Si stack structure is annealed at 400°C for 20 minutes in hydrogen or nitrogen/hydrogen mixtures. The anneal causes the silicon to diffuse into the Al–Cu layer and allows the titanium layer to contact diffusions and polysilicon.

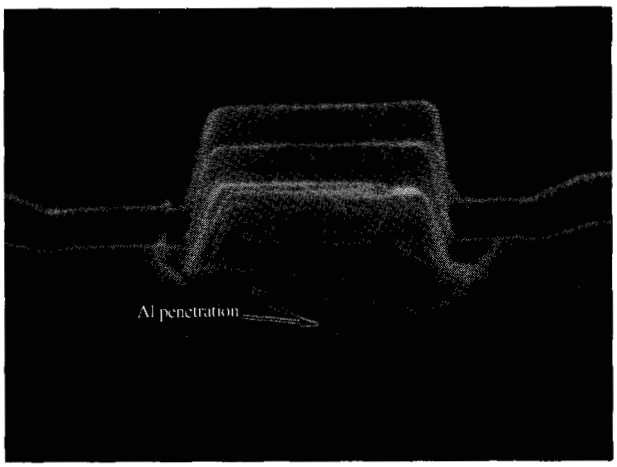

Figure 8

Scanning electron micrograph of Al penetration in a partially covered contact region.

Contact resistance

The advantages offered by a titanium contact layer in a metallization include potential increases in electromigration mean-time-to-fail [13] and resistance to hillock formation [14], as well as reproducible, stable contact resistance (R_c). Our studies have concentrated on the contact resistance obtained using titanium. The reduction of thin interfacial SiO_2 by titanium metal [11] allows the contact resistance obtained with titanium to be insensitive to small run-to-run process variations.

Unlike many materials, contact resistance using a titanium contact layer has been observed to be stable with typical post-metallization heat treatments. For instance, **Figures 4(a)** and **4(b)** show n^+ diffusion contact chain resistance as a function of heat treatment for Pd_2Si [in 4(a)] and Ti [in 4(b)] contact layers. The contact resistance of the Pd_2Si sample increases as temperature is increased from

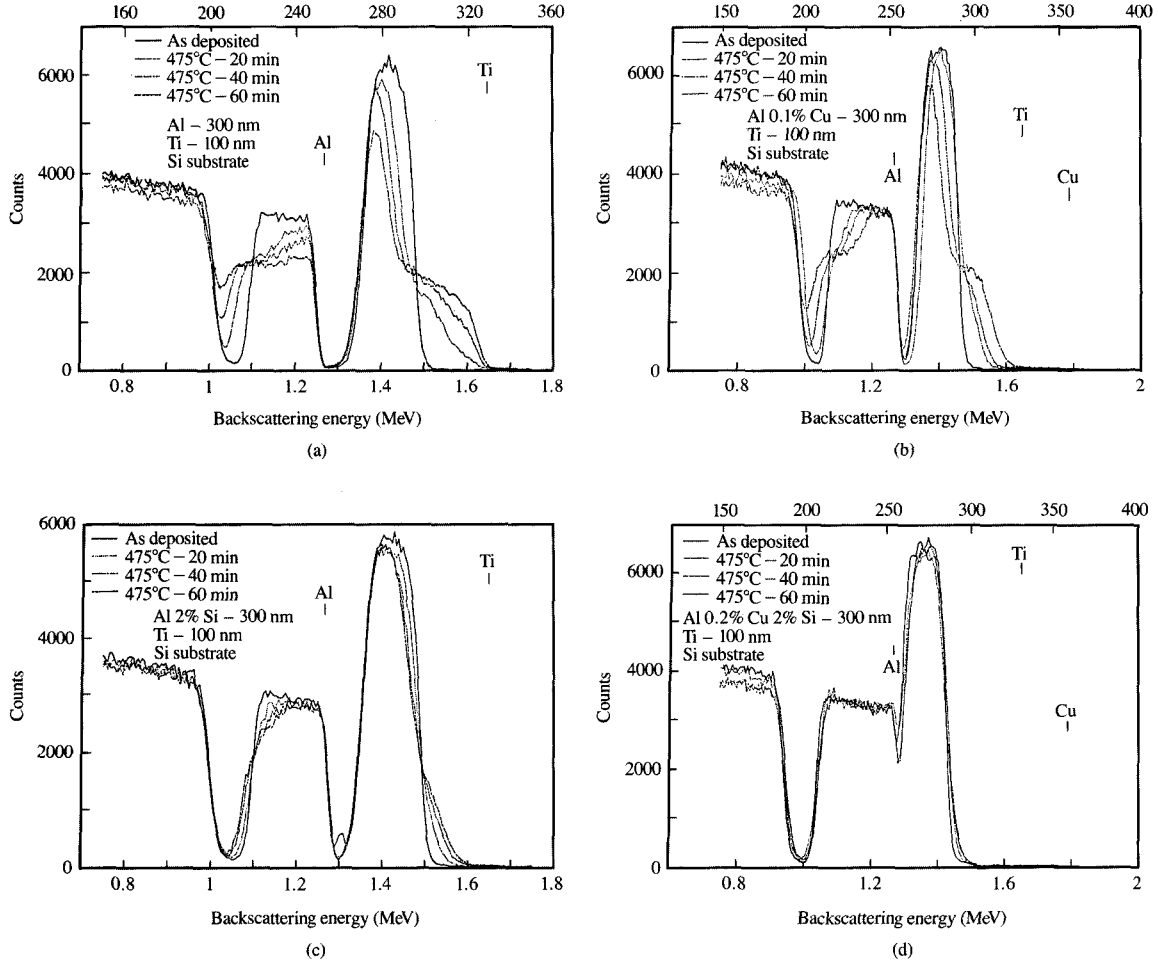

Figure 9

RBS spectra of (a) Ti/Al, (b) Ti/Al–Cu, (c) Ti/Al–Si, and (d) Ti/Al–Cu/Si thin films as deposited and after 475°C anneals of 20, 40, and 60 minutes in a 10% hydrogen and 90% nitrogen ambient. The Al layer in Figure 9(a) has been completely consumed after one hour at 475°C. The presence of either Cu [9(b)] or Si [9(c)] retards the Ti–Al reaction. The presence of both Cu and Si [9(d)] almost halts the reaction.

350°C to 400°C and increases with time at 400°C. This increase in R_c is caused by the formation of an Al–Pd–Si ternary compound and the concurrent loss of properties as a barrier to Si epitaxial growth [8]. Although a ternary has been observed in the Al–Ti–Si system [7], no corresponding increase in R_c has been observed at temperatures up to 400°C. The kinetics of the Ti–Al reaction are such that only a small amount of the titanium is consumed (at 400°C) and therefore its Si barrier properties are retained. This difference between Ti and Pd_2Si contact layers is particularly noticeable when contact resistance distributions are examined. **Figure 5** shows chain contact resistance distributions for Ti and Pd_2Si. The R_c in the titanium case is much lower and more tightly distributed than for Pd_2Si.

PtSi shows contact resistance characteristics similar to those of titanium when it is subjected to comparable heat treatments, as shown in **Figure 6**. However, cost considerations and process simplicity favor the use of a titanium contact barrier. Not only does the platinum source material cost more than titanium, but PtSi formation requires a separate electron gun evaporation or sputtering step plus annealing and etching steps to form it. Ti is more

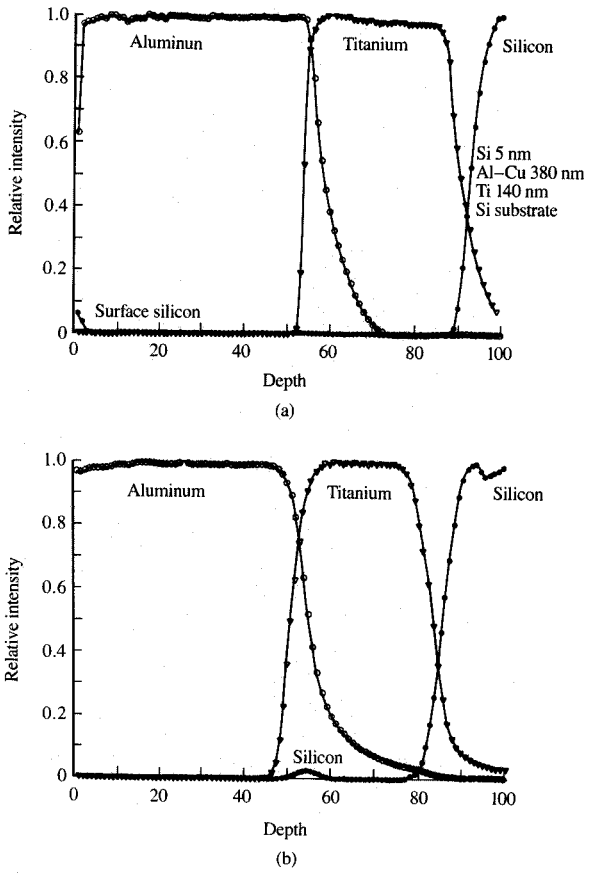

Figure 10

SIMS depth profiles of Ti/Al–Cu/Si films: (a) as deposited and (b) after one hour at 400°C in a 10% hydrogen and 90% nitrogen ambient. Note that during the anneal the silicon has moved from the film surface to the Ti/Al–Cu interface.

cost-effective, since it can be evaporated along with the metallization layer and requires no additional processing.

Defects

Two types of defects arising from this process have been observed. Titanium source material and tungsten filaments may sometimes be contaminated with sodium or other elements that are mobile in silicon dioxide. Great care is taken to obtain high-purity titanium (99.9%) and low-alkali tungsten filaments to avoid this potential problem. The second type of defect from this process is due to the use of the lift-off patterning technique.

Figures 7(a)–(d) display the metallization patterning sequence. Note in Figures 7(b) and 7(c) that the titanium and aluminum are deposited at different angles of incidence. The evaporation sources are positioned such that evaporant from the Al–Cu source is normally incident on the center of each wafer position in the evaporator dome (substrate holder). Since only one source can occupy the position that delivers evaporant at normal incidence, the titanium and silicon are evaporated at non-normal incidence. The silicon source is usually at the same height as the Al–Cu source and approximately 100 mm from the center position. The titanium source is usually positioned above the Al–Cu source on a swing arm (as close as possible to the Al–Cu source to minimize the difference in angle of incidence). After titanium evaporation is complete, the swing arm moves the titanium source out of the way to allow unimpeded evaporation of the Al–Cu. This difference in source positioning causes the titanium layer to be misaligned with the Al–Cu layer.

The source misalignment can produce areas where the Al–Cu layer may be in direct contact with the substrate. This becomes important in partially covered contact regions where the Al–Cu layer directly contacts diffused silicon. Annealing above 400°C may produce aluminum penetration into the contact if an inadequate amount of Si is added to the metallization. **Figure 8** shows a scanning electron micrograph of an aluminum penetration in a partially covered contact region. The Al penetration occurred in the misaligned region where the Al alloy layer was in direct contact with the silicon substrate. To more clearly show the Al penetration, the diffused region of the silicon substrate has been etched away. It is clear that due to the layer misalignment associated with lift-off, titanium is not a barrier to Al penetration and must therefore be used with an Al–Si-based interconnect metallurgy. It has been demonstrated that utilization of an Al–Cu interconnect film with an excess amount of Si is sufficient to eliminate this problem. Moreover, since the Ti does provide an effective barrier to Si solid-phase epitaxy over the majority of the contact, this excess Si does not have any deleterious effects on contact resistance.

Ti–Al interactions and silicon redistribution

Bower [7] has reported that titanium and aluminum react at or above 350°C to form $TiAl_3$ with an activation energy of 1.85 eV. In this study, Rutherford backscattering spectrometry (RBS) has been used to study the effect on the Ti–Al reaction of alloying additions of copper and silicon to aluminum. **Figures 9(a)–(d)** show RBS spectra of Ti/Al, Ti/Al–Cu, Ti/Al–Si, and Ti/Al–Cu/Si thin-film couples as deposited and after heat treatment at 475°C for 20, 40, and 60 minutes. Figure 9(a) shows that the Ti–Al reaction has completely consumed the available Al after one hour at 475°C. The addition of only 0.1 weight percent copper retards the Ti–Al reaction [Figure 9(b)]. This is in agreement with the observations of Krafcsik et al. [15], who found that

the addition of Cu retarded the growth rate of $TiAl_3$ by an order of magnitude and increased the activation energy for $TiAl_3$ formation from 1.8 to 2.4 eV. When silicon is added, the reaction is even slower [Figure 9(c)]. Surprisingly, the addition of both Cu and Si to the Al interconnect almost halts the reaction, even at 475°C for one hour [Figure 9(d)].

The redistribution of silicon in aluminum films in contact with titanium layers has been studied by secondary ion mass spectrometry (SIMS). Silicon diffuses rapidly through both aluminum and aluminum alloys [3]. SIMS characterization of evaporated Ti/Al–Cu/Si films in this study indicates that Si diffuses rapidly from the top of the interconnect and collects on the titanium layer. **Figure 10(a)** shows the SIMS profile of a Ti/Al–Cu/Si stack structure prior to heat treatment. **Figure 10(b)** shows the SIMS profile of this structure after a 400°C one-hour anneal in nitrogen/hydrogen. The silicon has redistributed during the anneal, accumulating at the Ti/Al–Cu interface. This phenomenon may be a result of the silicide formation reactions described by Bower [7] and Hinode et al. [16].

Summary

The various criteria associated with the choice of an ohmic contact material for VLSI logic have been discussed. The silicon solid-phase epitaxy phenomenon has been shown to increase contact resistance and decrease the manufacturing process window. Results have been presented which show that the contact resistance of Pd_2Si increases with extended annealing at 400°C, while PtSi and Ti contact materials exhibit stable contact resistance under the same conditions. A Ti/Al–Cu/Si process which is compatible with a lift-off patterning technique and partial coverage of contacts has been described. RBS measurements have been used to observe the Ti–Al reaction. Copper and silicon alloy additions have been shown to significantly retard this reaction. SIMS data illustrate substantial redistribution of Si during post-metallization heat treatments.

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