# Analysis of the holding current in CMOS latch-up

by Haruhiro Matino

**The holding current in CMOS latch-up with or without well and/or substrate bias has been examined. Measurements indicate that the holding current increases significantly with reverse bias and low shunting base resistance. It is shown that a previous equation for the holding current is inaccurate, and a new equation for holding current with bias is presented.**

## 1. Introduction

One of the major problems encountered in implementing the use of CMOS integrated circuits has been the occurrence of latch-up. Various methods to reduce or eliminate latch-up have been discussed [1, 2], but not completely resolved. Estreich [2] has discussed the condition for triggering latch-up in some detail, and in [1, 2] an equation for the holding current is given in terms of the *forward* base-emitter voltage $V_{BE}$ as

$$I_H = \frac{1}{\beta_{npn}\beta_{pnp} - 1} \times \left[\frac{\beta_{npn}(1 + \beta_{pnp})V_{BEn}}{R_w} + \frac{\beta_{pnp}(1 + \beta_{npn})V_{BEp}}{R_s}\right], \quad (1)$$

where $V_{BEn}$ and $V_{BEp}$ are the external forward voltages necessary for latch-up to occur for the npn and pnp transistors, respectively. This is incorrect physically. The holding current is related to the total reverse base-emitter voltage, including the built-in junction potential, as discussed in Section 3.

In addition, the base current direction in the triggering of latch-up and in the sustaining of latch-up has not been made clear in the literature [1–5]. Most authors have considered the triggering condition when the base-emitter is forward-biased by noise, or have confused the triggering and the sustained latch-up condition. However, the sustained latch-up condition after elimination of the noise which triggers latch-up is more important, because holding current is defined only for the sustained latch-up condition after elimination of the triggering signal.

The effects of the substrate or well bias on the holding current and transient triggering conditions have been studied recently [3, 5, 6]. A typical current-voltage latch-up characteristic is shown in **Figure 1**. The holding current $I_H$ is defined as the current at the sustaining voltage $V_S$. In this study, holding current has been measured as a function of the bias voltage for the following: discrete transistor pairs, simulating the case of high current gains for both npn and pnp devices, and integrated n-well CMOS structures in which the npn and pnp devices have relatively low current gain. A physical model and a holding current equation applicable both with and without bias are also presented.

## 2. Experimental results

The circuit for measuring the holding current $I_H$ is shown in **Figure 2**. Pulse generator 2 is used for triggering into the *on* state; the dc *off* set bias is provided as indicated. The external base-emitter shunting resistance $R_b$ can be varied. A sawtooth wave is applied across the structure in order to obtain precise $I_H$ values. After application of the anode voltage by means of pulse generator 1, a triggering pulse sufficient to cause latch-up is applied to the base by means of

pulse generator 2. After the trigger pulse, the base-emitter junction voltage of the device connected to pulse generator 2 returns to the original dc bias voltage. When the anode voltage, which is decreasing gradually, as shown in Fig. 2, drops below the sustaining voltage $V_S$ of the pnpn device, the anode current decreases suddenly to the leakage current of that device. The holding current is measured through $R_L$ as the minimum value in the *on* state.

**Figure 3** shows measured values of $I_H$ as a function of the bias voltage for a discrete transistor pair. The common-base current gains of the pair are 0.974 for the npn transistor and 0.995 for the pnp transistor. Note that the holding current approaches zero at forward bias conditions when $R_{bp}$ or $R_{bn}$ is open.

**Figure 4** shows measured values of $I_H$ vs. bias voltage for the n-well CMOS devices [7]; current gains were 0.5 for the npn structures and 0.83 for the pnp structures. Again, there is a significant linear increase of the holding current with reverse bias. Estimated intrinsic base resistances obtained from Fig. 4 are 750 ohms for the npn portion and 3.96 kilohms for the pnp portion.

In both cases, the holding current at the forward bias conditions approaches zero or very small values.

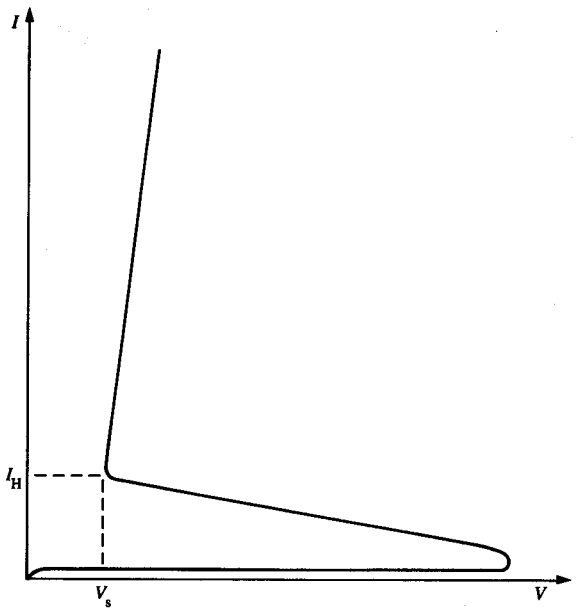


**Figure 1**

Typical current-voltage latch-up characteristic.

## 3. Discussion and conclusions

Equation (1), given previously [1, 2] in terms of $\beta$, has been applied to the triggering of latch-up. Equation (1) also shows that the higher forward bias $V_{BE}$ gives the higher $I_H$ values, and that $I_H = 0$ at $V_{BE} = 0$.

The experimental results given above indicate that contrary to Eq. (1), the holding current in CMOS latch-up should be proportional to the reverse bias voltage instead of the forward bias voltage, and the holding current is not zero at zero bias; it reaches zero in the forward bias state.

In the triggering condition of **Figure 5(a)**, an external noise source, such as a constant current source, drives the base-emitter junction in the forward direction. The pnpn device is easily triggered into the *on* state because the holding current at the forward-biased condition is very small, as shown in the experimental results. After the noise source is removed, the base-emitter junctions become reverse-biased by $V_{Rp}$ and $V_{Rn}$. The reverse current through $R_b$ results from the minority-carrier-storage effect and is given by

$$I_R = \frac{\phi_B + V_R}{R_b}, \tag{2}$$

where $\phi_B$ is the built-in potential of the junction, $V_R$ is the bias voltage in the reverse direction, and $R_b$ is the total series resistance of the circuit. The reverse-direction minority-carrier-storage current is observed during the *on* state, as shown in **Figure 6**.

Previously, several authors have discussed the gate turn-off of pnpn devices (GTO or gate turn-off thyristor) [8–11]. The *off* condition for the pnpn device shown in **Figure 7** is

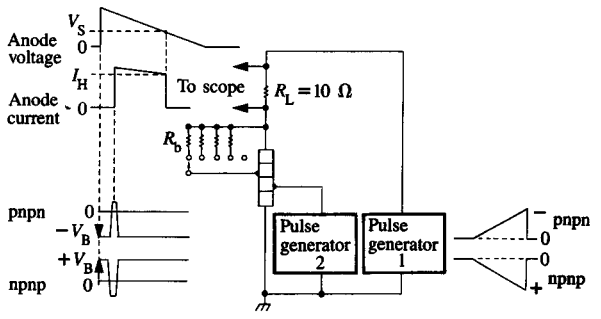


**Figure 2**

Circuit configuration for measurement of holding current.

$$I_c < \frac{\alpha_p I_{bp} + (1 - \alpha_p) I_{bn}}{\alpha_n + \alpha_p - 1} \tag{3a}$$

or

$$I_e < \frac{\alpha_n I_{bn} + (1 - \alpha_n) I_{bp}}{\alpha_n + \alpha_p - 1}, \tag{3b}$$

where $I_{bn}$, $I_{bp}$, $I_c$, $I_e$, $\alpha_n$, and $\alpha_p$ are defined as shown in Fig. 7.

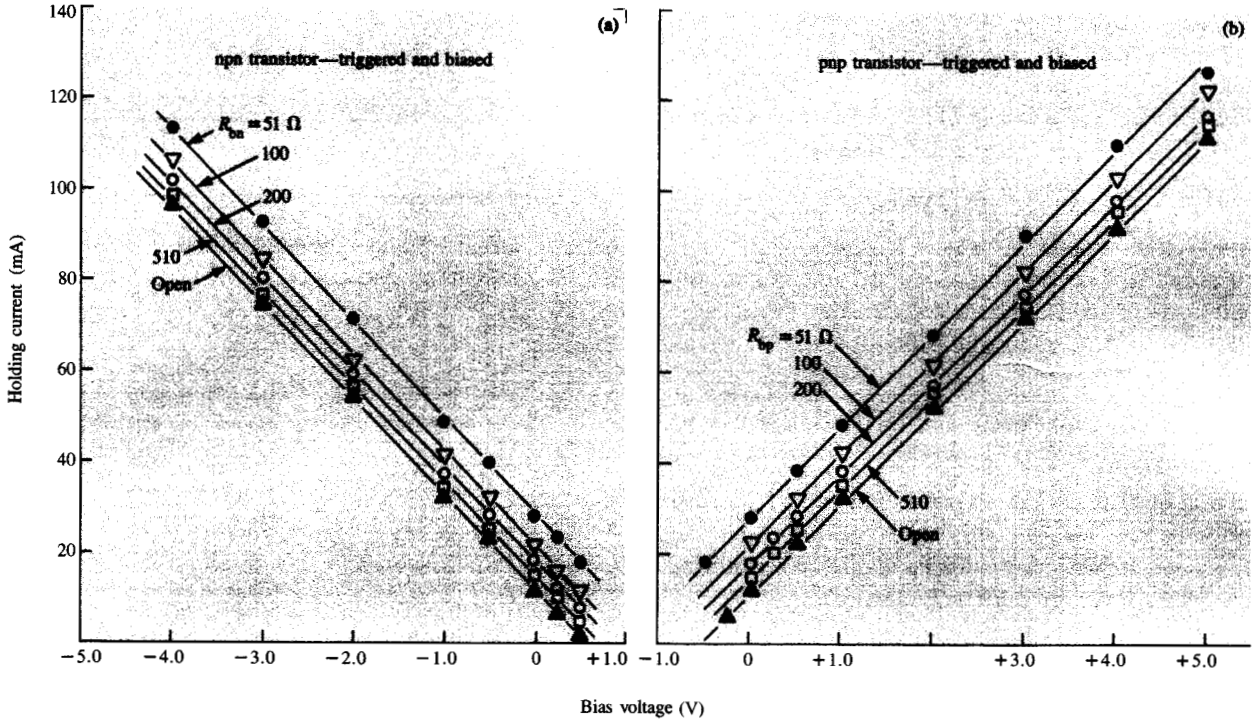


**Figure 3**

Holding current vs. bias voltage for a discrete npn (a) and pnp (b) transistor pair.

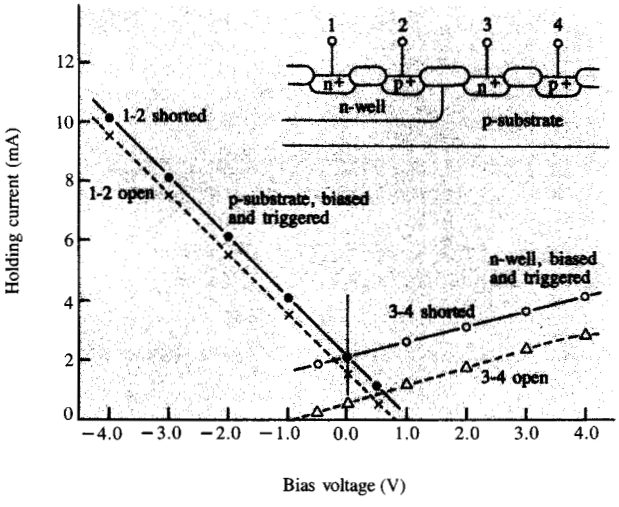


**Figure 4**

Holding current vs. bias voltage for n-well CMOS devices.

The holding current $I_H$ is given by the summation of $I_c$ and $I_{bn}$, or $I_e$ and $I_{bp}$, so that

$$I_H = \frac{\alpha_p I_{bp} + \alpha_n I_{bn}}{\alpha_n + \alpha_p - 1}. \quad (4)$$

This equation shows that the larger the magnitude of $I_{bp}$ or $I_{bn}$, the larger the holding current. These are external base currents and their direction is opposite to that in the forward bias condition. Of course, $I_H$ is infinite when $\alpha_n + \alpha_p$ is equal to unity, which is a condition completely free from latch-up. These equations are valid only in the sustained latch-up mode after triggering, when the pnpn device is *on*. Minority carriers are continuously being injected and recombining in this mode. In the absence of latch-up, $I_{bn}$ or $I_{bp}$ is zero before triggering.

By using Eq. (2), Eq. (4) can be written as

$$I_H = \frac{1}{\alpha_n + \alpha_p - 1}\left[\frac{\alpha_n(\phi_{Bn} + V_{Rn})}{R_{bn}} + \frac{\alpha_p(\phi_{Bp} + V_{Rp})}{R_{bp}}\right], \quad (5)$$

where $\alpha_p$, $\phi_{Bp}$, $V_{Rp}$, and $R_{bp}$ are the current gain, built-in potential, reverse bias voltage, and base-emitter resistance, respectively, for the npn transistor, and $\alpha_n$, $\phi_{Bn}$, $V_{Rn}$, and $R_{bn}$ are the equivalent quantities for the pnp transistor. Equation (1) is similar in form to Eq. (5) but incorrectly includes the *forward* base-emitter voltage $V_{BE}$ instead of the total *reverse* potential $\phi_B + V_R$, which includes the built-in potential.

Equation (5) gives a steady-state holding current, because minority carriers are being injected and recombining in the base regions continuously in the *on* state. Note that $I_H$ becomes larger when the pnp or the npn transistor is reverse-

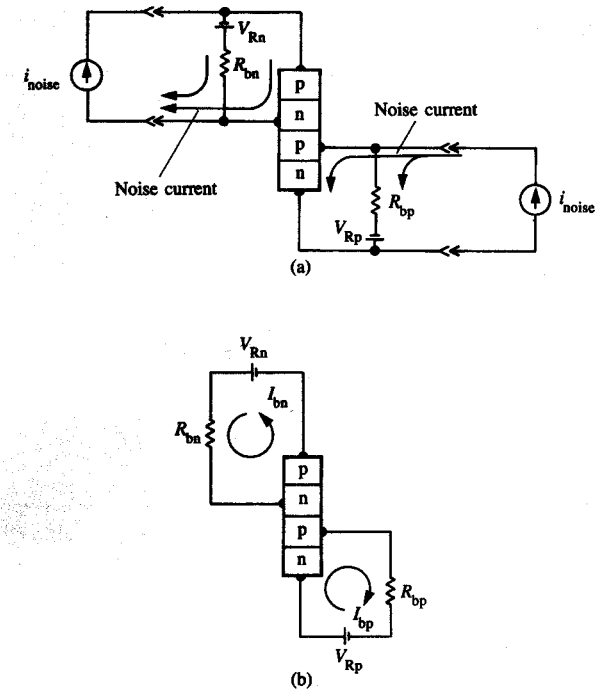


**Figure 5**

Equivalent circuit for triggering latch-up in (a), and for sustained latch-up after triggering in (b).

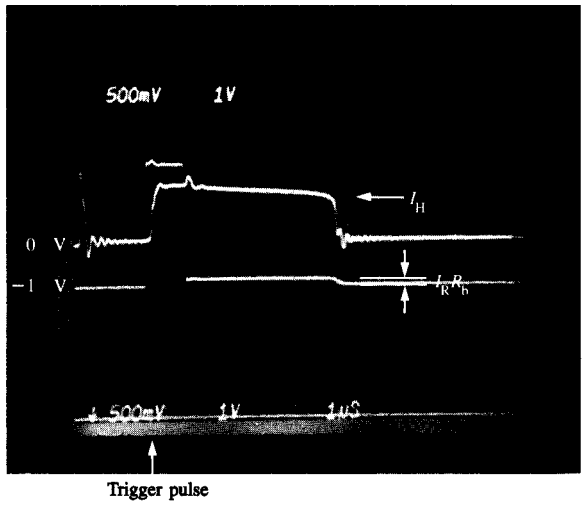


**Figure 6**

Typical experimental waveforms of the anode current (upper curve, 10 mA/division) and of the base voltage (lower curve, 1 V/division). The reverse-direction minority-carrier-storage current is observed as $I_R R_b$ during the *on* state. The holding current $I_H$ is the minimum value of the anode current in the *on* state.

biased and becomes very small under forward bias. Equation (5) also predicts that the holding current reaches zero if (1) $R_{bn}$ and $R_{bp}$ are infinite, or (2) $V_{Rn} = -\phi_{Bn}$ and $V_{Rp} = -\phi_{Bp}$, i.e., when the transistors are forward-biased.

The physical models representing the states before and after triggering are quite different. The equivalent circuits for the sustained latch-up mode after triggering and for triggering latch-up are shown in Fig. 5. Equation (5) gives the holding current for the sustained latch-up model after triggering, in which $I_H$ is determined by reverse-direction currents in the base junctions of the transistors required to sustain carrier injections from the emitters, as shown in **Figure 5(b)**.

In the triggering condition of Fig. 5(a), the direction of $I_{bp}$ or $I_{bn}$ is opposite to that in the sustaining condition, and thus they are not inversely proportional to $R_{bp}$ or $R_{bn}$. External noise sources, such as constant current sources, drive both the base-emitter junctions (in the forward direction) and their associated resistors. Of course, small values of those resistors lead to a small voltage drop and hence to a suppression of triggering. For the same reason, shunting the base-emitter junction with a Schottky-barrier diode, or a tunnel or backward diode in parallel, is very effective in improving the immunity to latch-up. After triggering caused by noise, the holding current increases to the value defined by Eq. (5). Clearly, reverse bias is very effective in increasing the holding current and, hence, in substantially increasing the immunity to latch-up.

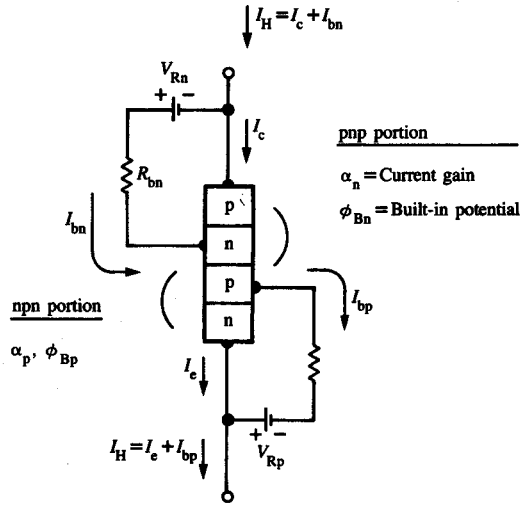


**Figure 7**

Simplified equivalent circuit of a pnpn device.

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