Jitter accommodation in token-passing ring LANs

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In a token-passing ring Local Area Network (LAN) each message accumulates phase jitter as it travels around the ring. Unlike typical digital transmission systems, which tend to have random data traffic, ring systems carrying computer-generated traffic may have long strings of repetitive-pattern data. This traffic produces a jitter amplitude which is a function of the message statistics and the transmission characteristics of the physical layer. For the system to be stable, this jitter must be controlled. This paper describes the repetitive-pattern jitter generation and accumulation process and gives a methodology for designing the physical layer components to accommodate it.

1. Introduction

The IEEE 802.5 Local Area Network Standard [1] describes a token-passing media access technique for LANs. In this scheme all messages make one complete transit around the ring from their "source" station, through each station on the ring, including the "destination," and back to the "source," as shown in **Figure 1**.

As they pass through each station, the message data are equalized, regenerated, and retimed by the physical layer. **Figure 2** shows the various physical layer subsystems in each station that perform these functions.

Inevitably, because of nonideal circuit implementation, each retiming operation adds jitter to the data, so that in a large ring the accumulated jitter can become the principal transmission impairment. For the system to be stable, there must be one station in the ring, called the monitor, which provides a reference clock and accommodates the accumulated jitter in an elastic buffer. The input data are written into the buffer using the recovered clock and read out using the reference clock, as illustrated in **Figure 3**.

The next section begins with a review of the relevant literature on jitter generation and accumulation for general digital transmission systems. We observe that the data characteristics in LAN are different from those in general systems, so that the jitter accumulates more rapidly than would normally be expected. The next subsection describes computed and measured results of the jitter buildup in a ring of LAN stations using phase-lock loop (PLL) timing recovery circuits. This is followed by a review of the role of equalization in minimizing the jitter generation in a ring environment. In Section 3 we give a methodology for designing the components in the physical layer to accommodate the more rapid jitter accumulation process.

2. Jitter generation and accumulation

• *Literature survey*

Jitter generation and accumulation in digital transmission systems have been studied extensively. Recently Del Pistoia et al. [2] extended some of the theoretical analyses, and their paper includes a good summary of earlier work.

Briefly, sources of jitter in a digital repeater can be divided into those which are signal-dependent and those which are not. The former are said to produce systematic jitter, and the latter, nonsystematic. Examples of each type are intersymbol interference and thermal noise, respectively. In a long chain

of repeaters, systematic jitter accumulates more rapidly than nonsystematic, since the former is by definition correlated.

Byrne et al. [3] in their classic paper described the Chapman model for calculating the systematic jitter accumulation due to random signals in a chain of N repeaters having bandpass filter (LC) timing recovery circuits. This model showed that random-signal systematic jitter accumulates in proportion to $\sqrt{N}$, and, by inference, nonsystematic in proportion to $\sqrt[4]{N}$; the latter result was also shown by Rowe [4] and DeLange [5]. Later Shimamura and Eguchi [6] showed that the Chapman model is a good approximation for random signals and second-order PLL timing recovery circuits, so long as their damping factor is large. However, for small damping factors, both types of jitter accumulate exponentially.

In the same paper Byrne et al. also analyzed the systematic jitter accumulation that occurs due to signals containing long periods of repetitive patterns, e.g., all ones. They demonstrated that the worst possible jitter amplitudes occur when a repetitive pattern which causes an extreme phase lead is followed by a pattern that causes an extreme phase lag, or vice versa. In this case, for bandpass filter timing recovery circuits, the repetitive-pattern jitter accumulates in proportion to N and, hence, more rapidly than random-signal systematic jitter.

However, the literature subsequently appears to have largely ignored the growth phenomena of repetitive-pattern jitter, concentrating instead on the properties of random-signal jitter. This may be explained by the fact that most digital transmission systems carry signals multiplexed from many sources, so that they tend to be random. The effect of line coding will correlate the line statistics, but this has been shown, e.g., Reference 7, to affect only marginally the $\sqrt{N}$ accumulation rate. (Matsushita et al. [8] found that significant amplitudes of repetitive-pattern jitter could be produced by simple PCM-coded video signals, but showed that it could be eliminated by scrambling the data before transmission. Thus the issue of repetitive-pattern jitter accumulation was essentially avoided.)

The next sections illustrate that repetitive patterns can easily arise in messages transmitted in LAN. Furthermore, with PLL timing recovery circuits, the resulting repetitive-pattern jitter can accumulate exponentially with the number of stations.

• *Message statistics in LANs*

In Reference 1 source signals are encoded using Differential Manchester code to condition them for transmission around the ring; **Figure 4** illustrates the encoding rules. A one bit is encoded with a transition at the mid-bit time, while a zero is encoded with transitions at both the beginning and mid-bit times. When there are no messages circulating around the ring, an "idles" signal is generated, consisting of all zeros; through encoding, this becomes a 4-MHz-square wave.

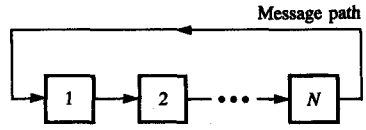

Figure 1

N-station ring.

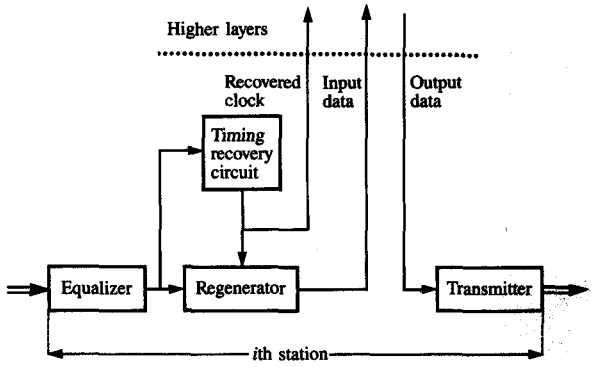

Figure 2

Physical layer subsystems in each station.

Figure 3

Elastic buffer in monitor station.

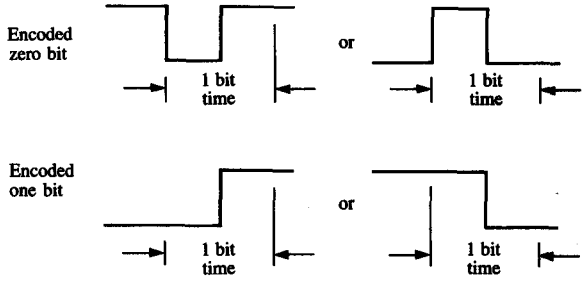

Figure 4

Differential Manchester encoding.

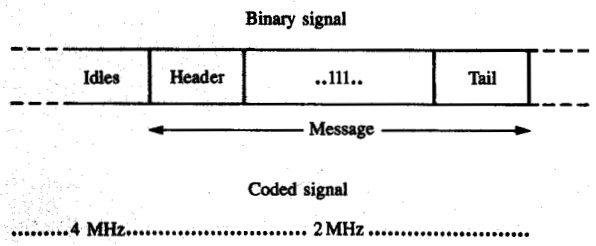

Figure 5

Possible message causing repetitive-pattern jitter.

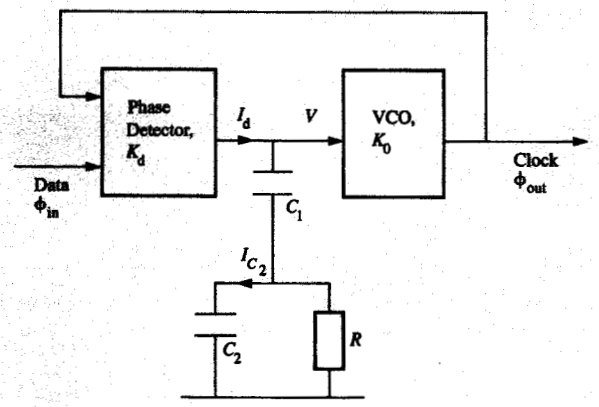

Figure 6

PLL timing recovery circuit.

In LANs, a message containing a string of identical bytes, e.g., transferring the contents of a large block of memory previously all initialized to the same value, is not uncommon. **Figure 5** shows an example of a message where the repetitive pattern within the message is all ones; encoded, this becomes a 2-MHz-square wave. We thus have the conditions for repetitive-pattern jitter accumulation.

• *PLL timing recovery circuits*

Figure 2 shows the subsystems of the physical layer within each station. The incoming signal is first equalized and then fed to a regenerator and timing recovery circuit. The latter recovers the clock and latches the recovered data. Both the recovered clock and input data are fed to the higher layers of the system. The timing recovery circuit is based on a phase-lock loop (PLL) instead of a bandpass (LC) filter because of the former's generally superior performance.

Figure 6 shows details of the PLL timing recovery circuit. A "zero-crossing"-type phase detector [9] produces a phase error signal on the rising edges of the data. This signal is fed, via a charge pump within the detector, through the loop filter (R, C_1, C_2) to the voltage-controlled oscillator (VCO). The VCO output is fed back to the phase detector input to complete the loop.

In theory, the behavior of this PLL circuit can be studied analytically. However, it rapidly becomes intractable if we want the model to include various practical circuit imperfections (e.g., VCO leakage current, phase detector nonlinearities) and then look at the behavior of a long chain of these stations. For this reason a computer simulation has been used as an analytical tool, solving the difference equations at successive discrete intervals in time.

Each repetitive pattern produces a periodic waveform with the phase of its rising edge crossing through zero at a particular instant, with respect to some reference. If the repetitive pattern is changed, the zero-crossing phase alters to a new value: That is, the pattern change produces a phase step at each PLL input. If the intersymbol interference extends only over the adjacent trailing time slot, then the position of all adjacent baud transitions will be perturbed; the position of rising edges preceded by two like bauds will not be temporally altered. Thus the biggest phase steps will occur when switching between Differential-Manchester-coded all-ones and all-zeros binary data and vice versa.

From Reference 9, the gain of a zero-crossing-type phase detector is proportional to the number of zero crossings and hence, by implication, the line signal baud probabilities p. For Differential-Manchester-coded data, the gain will be maximum and minimum for all zeros and ones, respectively. Thus the PLL phase step response to the all-zeros/ones pattern change will differ from that due to the all-ones/zeros change because of the effective difference in loop gain for the two situations.

Using standard circuit analysis, the difference equations for the PLL (Fig. 6) at the nth time instant can be written as

$$I_d(n) = K_d(p)[\phi_{in}(n) - \phi_{out}(n)], \quad (1)$$

$$V(n) = [(1/C_2)\Sigma I_{C_2}(i) + (1/C_1)\Sigma I_d(i)]\Delta T, \quad (2)$$

$$I_{C_2}(n) = \frac{RI_d(n) - (1/C_2)\Sigma I_{C_2}(i)\Delta T}{R + (1/C_2)\Delta T}, \quad (3)$$

$$\phi_{out}(n+1) = K_0 \Sigma V(i)\Delta T, \quad (4)$$

where

ΔT = time interval between successive evaluations,
ϕ_{in} = input phase,
ϕ_{out} = output phase,
$K_d(p)$ = phase detector gain for bit probability p,
K_0 = VCO gain,
V = VCO input voltage,
I_{C_2} = current through C_2,
C_1, C_2, and R = loop filter capacitors and resistor.

When the repetitive pattern changes, each PLL in a chain of stations initially sees a step change both in its input phase and in its phase detector gain. Subsequently the effects of these changes appear at each PLL output and eventually propagate along the whole chain. The response of the system can be usefully characterized by the PLL damping factor ζ [10]. With the circuit implementation of Fig. 6 it becomes

$$\zeta = (R/2)\sqrt{C_1 K_0 K_d(\bar{p})}, \tag{5}$$

where $\bar{p}$ is the average bit probability.

Solving Eqs. (1–4), we find that if ζ and $C_1 \div C_2$ are large, then each PLL behaves as a second-order loop. The same behavior has been observed in [11] for random-signal jitter. Furthermore, the repetitive-pattern jitter response and accumulation are similar to those derived by Byrne et al. for bandpass filter timing recovery circuits. (The PLL as illustrated is strictly a third-order loop, although Gardner [12] has shown that, for $C_2 \ll C_1$, this is well approximated by a second-order design.) For small damping factors, the effect of jitter peaking becomes significant, as it did in the analysis of random-signal jitter by Shimamura and Eguchi.

Figure 7 shows an example of the computed time domain repetitive-pattern jitter response at the output of a chain of 1, 2, 4, 8, 16, and 32 stations to the effect of changing between all-zeros and all-ones binary data and back again. These results are for $\zeta = 2.0$ and $C_1 \div C_2 = 300$. The jitter amplitudes are normalized to their asymptotic values: That is, in the steady-state condition, after the transients have died down, the phase change at the output of the Nth station is equal to N times the phase step at the input to each station due to the intersymbol interference change.

It may be observed that the slope of the transition curves between the repetitive pattern is approximately inversely proportional to the loop bandwidth B, with the approximation improving as the damping factor is increased; this result agrees with that of Byrne et al. Hence the slope of the all-zeros/ones change is twice that for the all-ones/zeros change due to the change in phase detector gain. Extending the result obtained by Byrne et al., the duration of the transition τ is given by

$$\tau = N/B(K_d) \tag{6}$$

$$= \frac{N}{RK_0K_d(p)}. \tag{7}$$

From the results of many simulations, we have found that the rate of peak-to-peak repetitive-pattern jitter accumulation with virtual second-order PLL clock recovery circuits can be expressed as

$$\phi_N/\phi_1|_{p-p} = N + (N/2\zeta)^2 + \epsilon, \tag{8}$$

where

$$|\epsilon| < 0.1dB \quad \text{for} \quad \zeta > 5.5, \tag{9}$$

and $N < 500$.

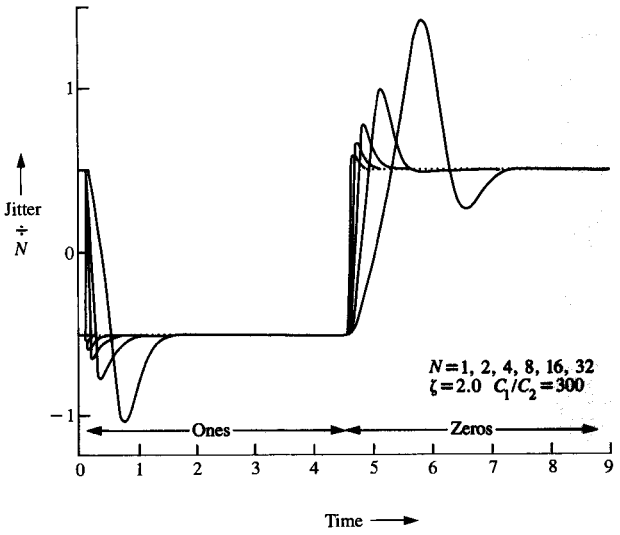

Figure 7

Computed repetitive-pattern jitter response.

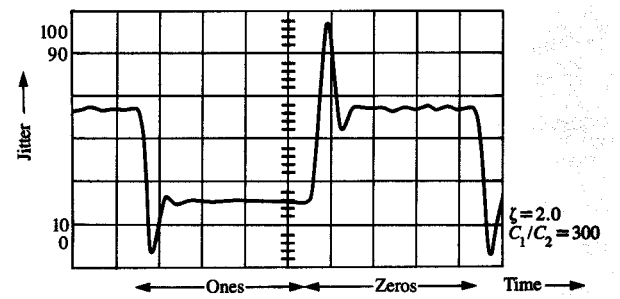

Figure 8

Measured repetitive-pattern jitter response for $N = 32$.

Figure 8 illustrates a measured repetitive-pattern jitter response at the output of a chain of 32 stations, with $\zeta = 2.0$ and $C_1 \div C_2 = 300$. The shape of the response and its peak-peak value are in good agreement with the computed results (Fig. 7).

Finally, as mentioned earlier, one of the advantages of a simulation is that it can incorporate the effects of practical circuit imperfections. For example, the effect of leakage current into the VCO, due to its finite input impedance, can be included by setting up the initial conditions

$$\phi_{out} = \phi_{in} - \frac{i_L}{K_d(p)}, \tag{10}$$

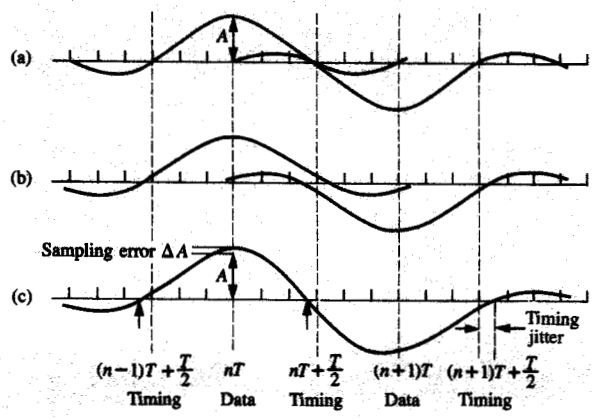

Figure 9

Timing jitter originating with intersymbol interference.

where i_L = leakage current, and extending Eqs. (1–4). In general, the addition of a small VCO leakage current does not change the shape of the repetitive-pattern jitter response but scales its amplitude so that its asymptotic values, after the transitions, are different. In theory the effect of the leakage current can completely cancel out the effect of the intersymbol interference.

• *Effects of equalization*

While the PLL characteristics such as loop gain, loop bandwidth, and damping factor determine how quickly jitter accumulates, equalization affects the amount of jitter contributed to the accumulation by each repeater. Initially, proper equalization seems a somewhat trivial task. The frequency responses of all the elements between repeaters are known, including the distortion characteristics of twisted-pair transmission cables. However, the ring differs from typical point-to-point twisted-pair digital transmission systems in that its interstation channel characteristics vary significantly with changing ring topology as users enter and leave the ring. Each repeater is subject to frequency-dependent and -independent variations in its received signal owing to the fact that its upstream neighbor can change, thereby changing the transmission distance to that neighbor. The ability of the equalizer to adapt to these variations will determine the amount of uncompensated distortion which appears as intersymbol interference and leads to jitter.

Timing errors from intersymbol interference

In an ideally equalized channel, **Figure 9(a)**, the tails of all previous pulses cross zero at each instant of time we wish to

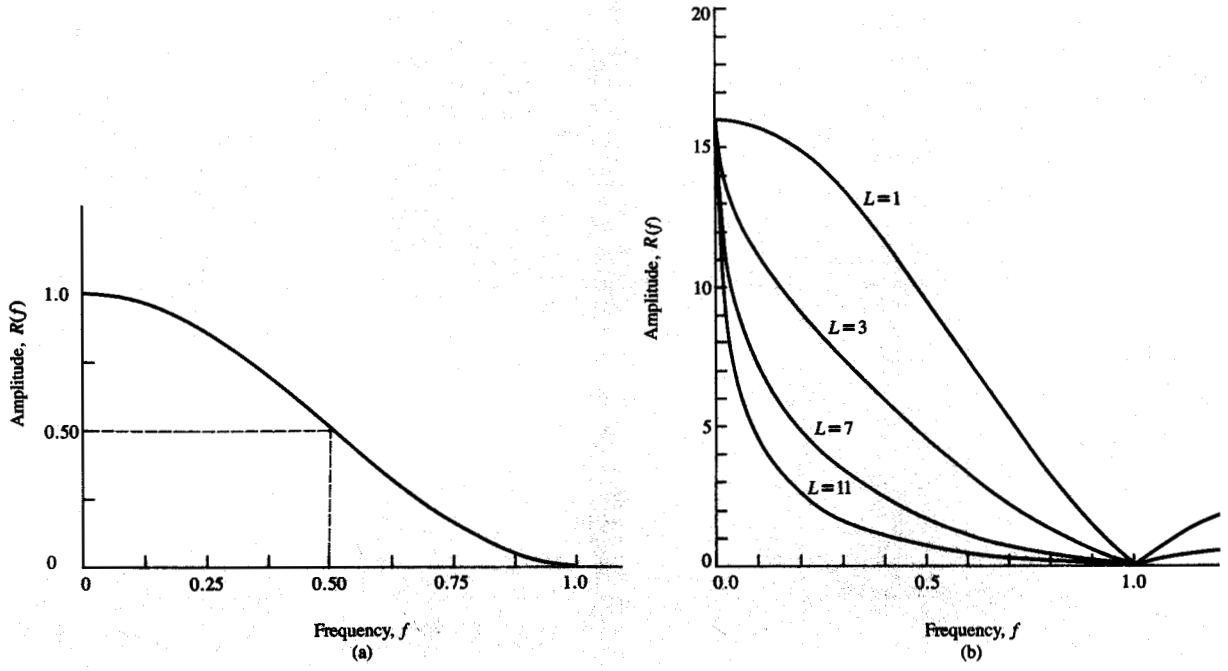

Figure 10

Ideal and actual channel frequency responses: (a) 100% raised cosine Nyquist channel; (b) channel variation with cable length.

either sample our present pulse ($t = nT$) or trigger the timing recovery mechanism ($t = nT + T/2$). Under nonideal conditions, as shown in **Figures 9(b)** and **9(c)**, the tails are nonzero and the leftover positive and negative contributions at these critical instants distort the amplitude of the present pulse. This distortion leads to variations in both the eye height and the zero-crossing times. Because it is the zero-crossings which trigger the timing recovery circuits, this variation results in jitter to the recovered clock.

The jitter just described, stemming from the random mixture of positive and negative signals, is normal systematic jitter. However, a worse situation can be expected to obtain in token-ring operation due to repetitive-pattern data. In this case, the contributions from unequalized tails are no longer subject to the random positive and negative cancellations. Thus the timing error tends toward a specific offset. When the pattern then changes, a new offset occurs which generates a timing phase step. The step produced by changing from an all-ones or all-zeros pattern to the reverse is the largest that can occur and is much larger than that produced by random data. As shown in the following discussion on Nyquist's criteria, equalization can adjust the characteristics of the channel to minimize intersymbol interference and the resulting timing jitter.

Nyquist's criteria

Nyquist's first criterion characterizes the type of channel frequency response shaping necessary to eliminate intersymbol interference at the nT sampling instants. In general this criterion can be stated as

$$R(f_1 - f) + R(f_1 + f) = 1, \tag{11}$$

where $R(f)$ is the channel frequency response and f_1 is equal to half the signaling rate ($1/2T$). Under linear phase conditions and bandlimiting to $|f| < 1/T$, this exhibits a form of symmetry about the point ($R = 1/2, f = 1/2T$) [13].

Further imposition of Nyquist's second criterion ensures that the intersymbol interference will be zero at the $T/2$ timing recovery instants as well. While the number of functions which can meet these criteria is infinite, the most commonly used shape is the 100% raised cosine shown in **Figure 10(a)**. The difficulty of actually achieving these two conditions is markedly apparent in **Figure 10(b)**. This figure presents a sample of channels to which the repeater is subject as the ring topology changes and the transmission distance from its upstream neighbor varies.

Clearly this wide variation in channel response demands either an extremely sophisticated equalizer or a system design which is tolerant of the jitter remaining after less rigorous equalization. Common sense suggests a less sophisticated equalizer and sufficient buffering to compensate for the resulting jitter.

The wide variation in channel response with transmission distance is primarily a result of skin effect. This effect produces a high-frequency loss approximately proportional to $\sqrt{f}$. Consequently, the desired equalization should include high-pass compensation. **Figure 11** illustrates typical repetitive-pattern jitter behaviors for three variations of less-sophisticated high-pass-type equalization. Not surprisingly, with nonideal equalization, the jitter increases for longer transmission distances because the signal is subject to more $\sqrt{f}$ distortion.

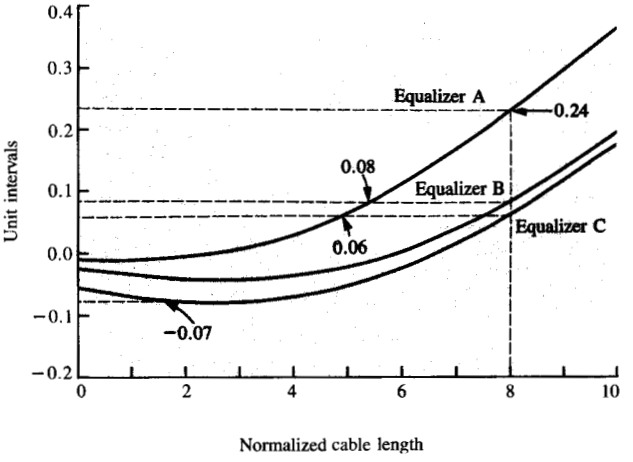

Figure 11

Pattern jitter vs normalized cable length.

3. System design impact

Jitter-tolerant system design must accommodate both jitter generation and accumulation phenomena in the token-ring LAN environment. The system designer must determine, within the applicable performance and cost constraints, a reasonable combination of equalization, elastic buffering, and PLL response to meet the range of ring topology needs.

As a quantitative illustration of the factors involved, consider a LAN ring of 32 stations ($N = 32$). Suppose that the damping factor of the second-order PLL timing recovery system has been set at 6.0 based on phase and frequency acquisition time requirements [10, 11]. The system designer is now left with a trade-off between equalization and elastic buffer size.

Equation (8) gives the jitter gain, or peaking, of repetitive-pattern systematic jitter. As a first-order approximation, we can assume that the nonsystematic jitter generated by each station is equal in peak-to-peak amplitude to the repetitive-pattern systematic jitter. (The error introduced by this approximation in the elastic buffer size calculation decreases with the size of the ring. In large rings the nonsystematic jitter contribution becomes relatively insignificant, so that its exact value is not too critical.) From References 4 and 5, nonsystematic jitter accumulates in proportion to $\sqrt[4]{N}$. Summing the amplitudes of the systematic and nonsystematic jitter, the size of elastic buffer needed can be

calculated as

$$E \geq \phi_{tot} = [\sqrt[4]{N} + N + (N/2\zeta)^2]\phi_1 , \quad (12)$$

where

E = total elastic buffer capacity required (see note),
ϕ_{tot} = total accumulated jitter of the ring,
N = number of stations in the ring (32),
ζ = PLL damping factor (6.0),
ϕ_1 = systematic jitter from a single station.

Note: The values of E, ϕ_{tot}, and ϕ_1 are normally expressed in terms of unit intervals where one unit interval equals the inverse of the system baud rate.

By using the values chosen for N and ζ, the jitter peaking quantity inside the brackets can now be computed so that $E \geq 41.5\phi_1$. Further, suppose that equalizer circuit design constraints and implementation limitations result in the three possible single-station repetitive-pattern jitter behaviors of Fig. 11. By determining what range of transmission distances can occur on the ring, a choice can now be made between equalizer performance and elastic buffer size.

Assume that an analysis of all possible ring topologies for this application indicates that the longest possible transmission distance for any station is 8 (normalized units of length). By referring to Fig. 11, the system designer would check each of the three curves for the largest positive or negative jitter ϕ_1 for lengths less than or equal to 8. Fig. 11 and Eq. (12) considered together indicate that equalizer A yields 0.24 unit intervals for a single station and would require 10 unit intervals of elastic buffering. Similarly, equalizer B allows 0.08 unit intervals per station and needs 3.3 unit intervals of elastic buffering, while equalizer C allows −0.07 unit intervals and needs 2.9 unit intervals of elastic buffering. Thus, for a known maximum transmission distance, equalizer C allows the least jitter and keeps the size of the elastic buffer to a minimum.

4. Conclusions

Repetitive-pattern jitter can easily arise in LAN due to the nature of the transmitted signals. The amplitude of repetitive-pattern jitter exceeds that of random-signal systematic jitter and hence is the dominant source of jitter in a ring LAN. In general, with PLL clock recovery circuits, repetitive-pattern jitter accumulates at an exponential rate in a chain of stations, although with large damping factors it can be limited to a linear growth. A design example has been given to illustrate the system impact of typical parameters arising from the PLL design, equalizer design, and system topology constraints. In the example, it has been shown how trade-offs may be made to accommodate the worst-case repetitive-pattern jitter.

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