

VLSI wiring capacitance

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Accurate prediction of device current and the capacitance to be driven by that current is key to the design of integrated logic and memory circuits. A finite-element algorithm is described which simulates the capacitance of structures with general shape in two or three dimensions. Efficient solution of the linear equations is provided by the incomplete Cholesky conjugate gradient method. The model is used to simulate the wiring capacitance of a 1.25-micrometer VLSI technology. The predicted capacitances of closely spaced first-metal polycide-gate and second-metal conductors used in this technology agree with measured results. The simulated three-dimensional capacitance of a second-metal line crossing a first-metal line is twice that found when estimated by two-dimensional models. The effect of line-to-line capacitance on the noise margin of logic circuits and on the signal in a dynamic RAM is examined. This capacitance presents a limit to wiring density for logic circuits and is a significant signal detractor in dynamic RAMs with closely spaced metal or diffused bit lines.

Introduction

Although scaling theory [1,2] predicts that reducing circuit dimensions reduces proportionately the capacitance that a circuit must drive, several factors force capacitance to higher values. Increasing chip size and number of circuits per chip [3] increases the ratio of average interconnection length to minimum feature size. This implies the beneficial result of

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increased logic or memory function per chip, but only with a detrimental increase in the capacitance that each circuit must drive.

The linear increase in circuit speed and quadratic reduction in power per circuit predicted by scaling theory may only be obtained if the capacitance per unit conductor length does not change. This occurs only when the insulator thicknesses and conductor width and height scale at the same rate. In this case, reduced metal thickness causes an unacceptable increase in the resistance of signal lines and power buses. Also, it is difficult to adequately cover the step heights found in present multilevel conductor technologies with very thin metal layers. Indeed, the goals of reduced line resistance and capacitance seem mutually exclusive without a significant change in technology. For these reasons, conducting film thickness has not decreased as fast as width and space. The result is that an increased portion of conductor capacitance is composed of two- and three-dimensional effects, such as fringe capacitance between the edges of the conductor and the underlying ground plane, and coupling between adjacent lines. Recently, increased attention has been given to accurate simulation of these capacitances [4-6].

In this paper we present a new two- and three-dimensional algorithm for capacitance simulation. It employs the finite-element method and will model structures of general shape. The first section describes the numerical methods used in the model. Next, verifying experimental data are presented for a 1.25-micrometer technology with three levels of conductors. Also, we describe the results of simulation of the capacitance between two crossing conductors. Finally, the model is used to examine the effects of adjacent line coupling on logic and RAM circuits. Figures of merit for design of logic signal lines and memory bit lines are evaluated.

Numerical model

Accurate determination of the wiring capacitance of narrow and closely spaced conductors requires a model which

closely represents the true structure of the conductors and surrounding insulating layers. Many techniques exist which can quickly analyze simple structures but will not model the complex geometries of real devices. For example, Green's function methods restrict the geometric configuration of the insulators and conductors [7, 8]. To overcome these deficiencies, the Finite and Infinite Element Resistance and Capacitance Estimator (FIERCE) was developed [9].

The finite-element method is used to solve the Poisson problem from which capacitive components can be determined. The relationship between charge Q and potential V for a system of m conductors is given by

$$\vec{Q} = C\vec{V}, \quad (1)$$

where C is an m by m matrix. The columns of this matrix are determined by setting the potential on the i th conductor to unity with all other conductors set to zero. The charge on each of the conductors, Q_j , yields capacitance terms from the expression

$$C_{i,j} = Q_j/V_i. \quad (2)$$

To find the capacitance, m separate Poisson problems are solved with

$$V_i = 1, V_j = 0, \quad j = 1, \dots, m \quad \text{and} \quad i \neq j. \quad (3)$$

For each problem, the potential distribution is found. Then the charge on each conductor is determined. Although more involved than specialized techniques, the finite-element method is a much more flexible method. The key to reducing the computational effort is to implement an efficient procedure for solving the Poisson problems.

Here the Poisson equation

$$\nabla^2 V = -\rho/\epsilon \quad (4)$$

is solved approximately over the domain of interest. The domain is divided into a large but finite number of elements. By using suitable variational calculus techniques and assuming the form of the potential over a single generic element, an elemental matrix expression can be obtained [10]:

$$A\vec{V} = \vec{Q}, \quad (5)$$

where the nodal potentials are $\vec{V}$ and the charges at the nodes are represented by $\vec{Q}$. The matrix $|A|$ represents the geometry and permittivity of the element. Unlike the Green's function technique, it is possible for each element to represent a different material and for there to be no restriction on the number or configuration of insulating materials. For first-order elements, the nodes are at the vertices, while with higher-order forms nodes are at vertices, on element sides, and in the interior of the elements. Currently, first- through sixth-order triangular elements are employed for two-dimensional problems and first-order right-prismatic elements for three-dimensional problems.

The individual element equations are all calculated in succession and added into the total or global matrix, which is identical in form to (5) except that $\vec{V}$ and $\vec{Q}$ are of order n , where n is the total number of nodes of the model and A is an n by n matrix.

The vector, $\vec{V}$, represents the voltage at nodes which are fixed at a potential of 1 (i th conductor nodes), 0 (other conductor nodes), or are allowed to reach their equilibrium values. The global form of Eq. (5) may then be rewritten as

$$\begin{bmatrix} A_{1,1} & A_{1,2} \\ A_{2,1} & A_{2,2} \end{bmatrix} \begin{Bmatrix} \vec{V}_{\text{free}} \\ \vec{V}_{\text{fixed}} \end{Bmatrix} = \begin{Bmatrix} \vec{Q}_{\text{free}} \\ \vec{Q}_{\text{fixed}} \end{Bmatrix}. \quad (6)$$

Since the charge on the free conductors is zero, Eq. (6) can be rewritten as

$$A_{1,1}\vec{V}_{\text{free}} = -A_{1,2}\vec{V}_{\text{fixed}}, \quad (7)$$

$$A_{2,1}\vec{V}_{\text{free}} + A_{2,2}\vec{V}_{\text{fixed}} = \vec{Q}_{\text{fixed}}. \quad (8)$$

Equation (7) is solved to determine the value of the free potentials when V for the i th conductor is set to 1. Equation (8) is then evaluated to determine the charge on each conductor node. Capacitive values are then easily determined. The main computational problem is in the solution of Eq. (7), since the order of matrix $A_{1,1}$ may be in the tens of thousands.

The technique to solve Eq. (7) must be selected to minimize the number of operations without compromising accuracy. It is well known that $A_{1,1}$ is quite sparse due to the fact that most nodes of a finite-element mesh interact with very few other nodes. Extensive research has been conducted on the solution of systems of linear equations to reduce both memory requirements and operation count [11, 12]. Iterative or direct techniques are used depending on the specific problem and the available computational resources. For example, the Green's function method requires a direct solution method since the resulting matrices are dense and poorly conditioned [7]. The operation count for a direct solver is $O(n^6)$ and uses storage of $O(n^3)$, where n is the number of segments. Thus, only 100-conductor segments were a practical limit as recently as 1979. These restrictions are unacceptable for problems with complicated structures.

Both direct and iterative techniques were evaluated for the sparse equations generated by the FIERCE program. The direct solution technique was identical to that used in FIELDAY [13, 14]. This technique was selected for FIELDAY because it was numerically stable for large, sparse, ill-conditioned systems of equations. This matrix solver always obtains a solution within a predictable amount of computation time. For the linear equations generated by FIELDAY, iterative solvers were found to be less reliable and in some cases required very long times to obtain a solution.

In the FIERCE program this method performed well for two-dimensional problems. However, when large (greater

than 10,000 nodes) problems were tried, memory requirements exceeded memory resources. As an alternative, the Incomplete Choleski-Conjugate Gradient (ICCG) technique [15] was implemented. This technique is appropriate for the symmetric positive definite systems of equations resulting from solving the Poisson problem. The method is a combination of the conjugate gradient method (an iterative technique) and Choleski factorization (found in direct techniques). By itself, the conjugate gradient may be used to solve these equations, but when the original global coefficient matrix is conditioned with its approximate factorization, the result is a more rapid solution. A complete factorization is equivalent to direct solution, and the key to ICCG is to compute an efficient but effective partial factorization. Our choice was to pick approximate factors that were in the same row and column location as the nonzero terms of the original matrix. This choice is straightforward to implement, since the same indexing schemes could be used for the original and partial factor matrices. The storage requirement for the ICCG method is $O(n)$ and the operation count is $O(n^2)$ where n is the number of nodes. This is superior to the direct solvers.

To compare the performance of the ICCG technique with the direct matrix solver, a simple problem was devised. A two-dimensional mesh of 404 nodes and 600 elements was replicated in the third dimension to yield models of 3000, 6000, and 7800 elements and 2424, 4444, and 5656 nodes, respectively. Two nodes on the first face were fixed so that 2422, 4442, and 5654 free-node problems were solved. The solving techniques use the same row and column representation for the nonzero terms of the global coefficient matrix.

The direct solver does a symbolic factorization prior to numeric factorization, while the ICCG computes partial factors prior to the iterative calculation. **Figure 1** shows the comparison of solution time for the two techniques. For problems with 2400 or fewer free nodes, the direct technique is faster. However, for larger problems the ICCG is much faster, with the difference growing rapidly with problem size. **Figure 2** shows the total region required for the two approaches. The difference in region size grows rapidly with an increased number of nodes.

Similar models were used to determine ICCG performance for problems of much larger size. Comparisons with the direct solver version were not conducted, since some program changes would have been required to handle these large problems. Two models were used. They consisted of the same two-dimensional mesh replicated in the third dimension 5, 20, 50, 80, 120, 200, and 350 times. The first model had the entire top and bottom layers of nodes held at a fixed potential. For this model there were approximately equal numbers of free and fixed nodes. The second model had only two nodes on the first plane fixed. These models were contrived to provide a comparison between a

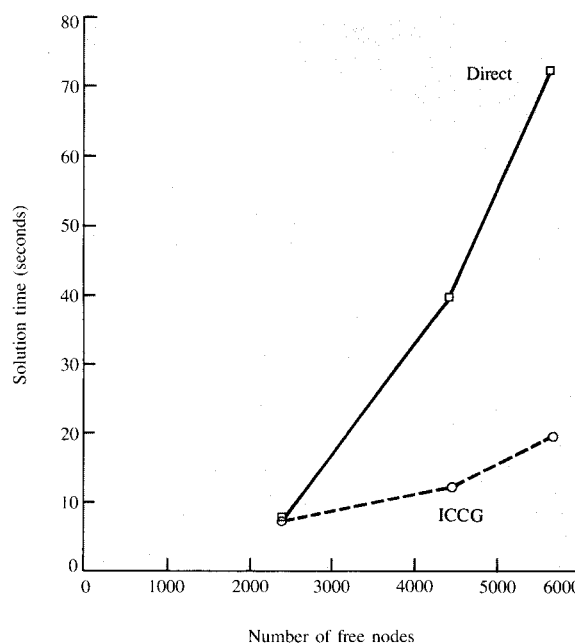


Figure 1

Solution time versus number of free nodes for direct and ICCG methods.

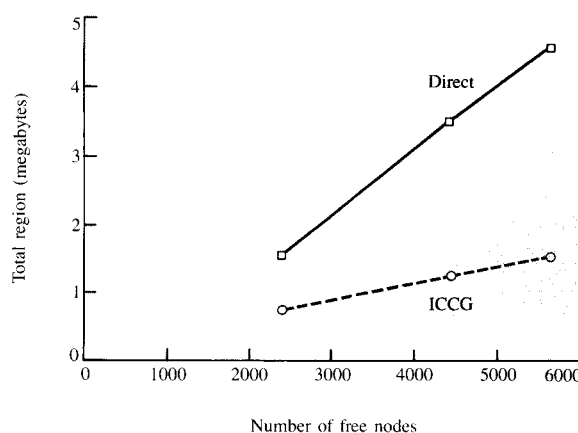


Figure 2

Storage region versus number of free nodes for direct and ICCG methods.

boundary-intensive model and a model with very few boundary nodes. **Figure 3** shows that the region size varies linearly with problem size. **Figure 4** shows the solution time for both models. With an equal number of free nodes, analysis takes much more time with a boundary-intensive problem. This is to be expected, since boundary condition

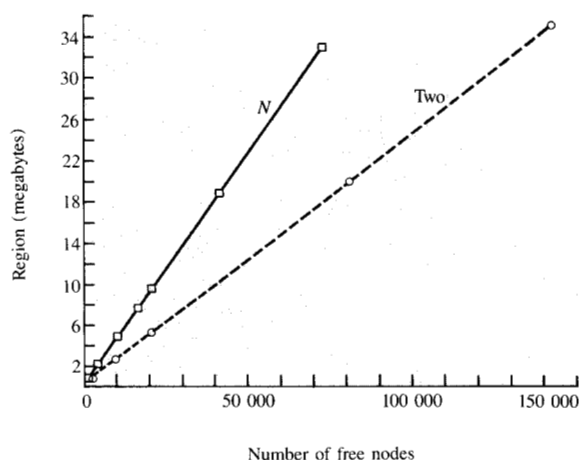


Figure 3

Storage region versus number of free nodes for a problem with two and N fixed nodes using the ICCG technique.

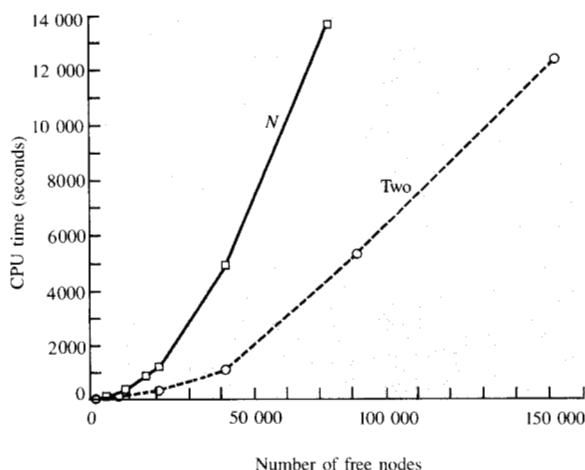


Figure 4

Total computation time versus number of free nodes for a problem with two and N fixed nodes using the ICCG technique.

information must be processed to modify the right-hand side of Eq. (7). However, when the total number of nodes is the same, the total computational time is about the same. In any case, the time for solution grows approximately linearly with problem size, rather than quadratically as with a direct solver.

Finite-element mesh generation can be an extremely time-consuming task. To reduce the time to generate the complicated meshes required for accurate simulation of VLSI wiring structures, a two-dimensional mesh generation algorithm was used [14]. An additional program was

Table 1 Nominal dimensions of serpentine and comb test structures.

Level	Pitch (μm)	Width (μm)	Length (μm)	Height (μm)
Silicide	2.1	1.5	32,000	0.34
First-metal A	2.7	1.7	100,000	1.20
First-metal B	3.3	1.7	100,000	1.20
Second metal	4.2	2.2	42,500	1.70

developed that modified a two-dimensional mesh to produce a three-dimensional mesh. In this case, a two-dimensional mesh is generated that describes a cross section of the structure of interest. This mesh is then replicated in the third dimension. The resulting mesh is modified so that three-dimensional features may be simulated. For example, the dielectric permittivity in any number of regions may be modified by specifying the eight corners of a region and the new property of the region. Also, a three-dimensional structure may be assigned to conductor regions by specifying points, lines, or planes. The mesh may then be plotted a layer at a time to verify the model input. Although not nearly as easy to use as an automatic mesh generation scheme, this program can be used to generate meshes describing complex structures.

To allow the user to obtain the large regions cited in the test problems, FIERCE has been written in VS FORTRAN using double-precision (16-byte) word length and is executed on an IBM System 3084 with the Extended Architecture (XA) capability. This enables the user to access regions of up to two gigabytes of main memory by the use of 31-bit addressing. Since the ICCG solver accesses storage addresses in a sequential fashion, this is an efficient use of the virtual storage provided by the XA architecture. This is not the case for a direct solver with optimal ordering.

Experimental verification

Verification is important both for testing the algorithm and for checking assumptions about physical structure and parameters. The model was verified by application to the three low-resistance conductors in an n -channel FET technology with a 1.25-micrometer minimum feature size. The conductors are tungsten silicide, first aluminum, and second aluminum. In this technology, tungsten silicide serves both as a gate for the active devices and as a local wiring level. The silicide was deposited via chemical vapor deposition [16] and patterned with step-and-repeat lithography and dry etching. A high-temperature oxidation surrounds this conductor with an insulating layer. The patterned and oxidized silicide was subsequently coated with a phosphoro-silicate glass. The aluminum levels were defined via a lift-off technique [17] and passivated with silicon nitride and polyimide. After first aluminum was defined, it was coated with a layer of plasma-deposited silicon nitride

and a layer of polyimide. These layers serve to isolate the first-metal level from the second and to passivate the active devices. The second-level aluminum definition was followed by another layer of polyimide.

The large serpentine and comb structures described in Table 1 were designed with minimum pitch (one line width plus one space) so that line-to-line and fringe-to-substrate capacitance could be measured with a low-frequency bridge.

The raw data were analyzed to separate the line-to-line capacitance per micrometer of edge C_L and the fringe-to-ground capacitance per micrometer of edge C_F from the total line capacitance per micrometer C_T . To find C_L , the measured total capacitance between two adjacent lines was adjusted for the capacitance between wafer probes and normalized by the total length of the adjacent edges. C_F was calculated by subtracting the parasitic capacitance of the probe pads and the area component of capacitance per unit length of line C_A . Figure 5 shows the components of capacitance of a line. Thus, the capacitance per unit length of each line is composed of an area term, which is the line width times planar capacitance per unit of area; a fringe term for each edge, which is the capacitance between the line and the substrate not accounted for by the area term; and a line-to-line term for each edge, which is the total capacitance between the line and the line adjacent to the edge. The capacitance per unit area was found by measuring the capacitance of a large area structure. The width of the narrow lines was found by direct measurement of the metal lines with a scanning electron microscope. For silicide lines the width was inferred from electrically measured channel length of active devices.

The nominal structures of the three conductors are shown in Figures 6-8.

The microscopic data were also used to measure the thickness and shape of all deposited films. The finite-element

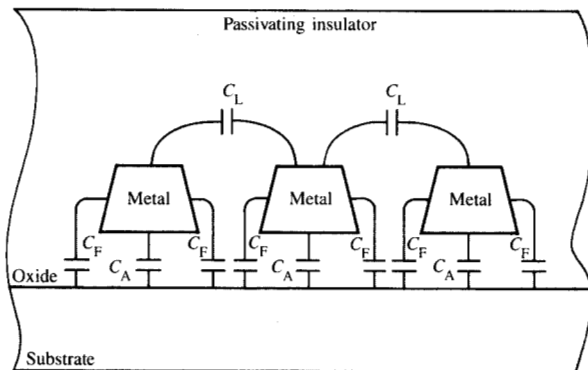


Figure 5

Capacitive components of a line with two adjacent neighbors.

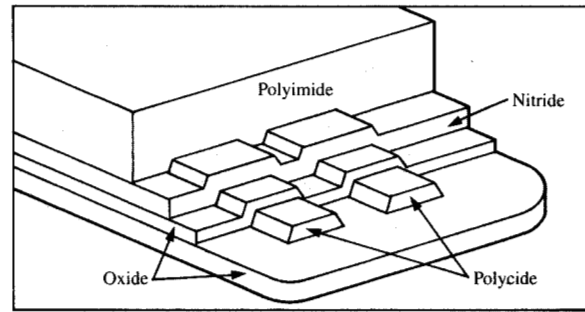


Figure 6

Polycide structure. Polycide thickness: 0.34 μm ; polycide slope: 70 degrees; overcoat oxide thickness: 0.24 μm ; nitride thickness: 0.4 μm ; underlying oxide thickness: 0.38 μm .

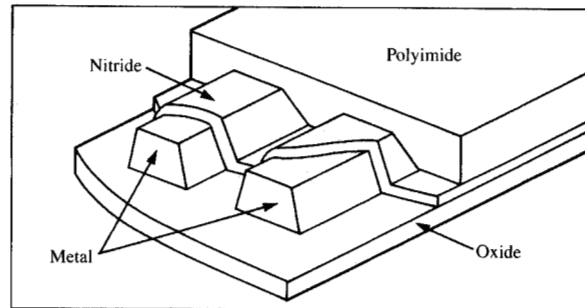


Figure 7

First-metal structure. Dimensions are shown in Fig. 9.

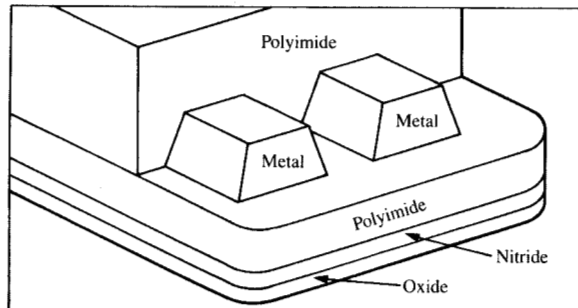


Figure 8

Second-metal structure. Dimension thickness: 1.7 μm ; metal slope: 70 degrees; nitride thickness: 0.4 μm ; underlying oxide thickness: 0.38 μm ; underlying polyimide thickness: 1.1 μm .

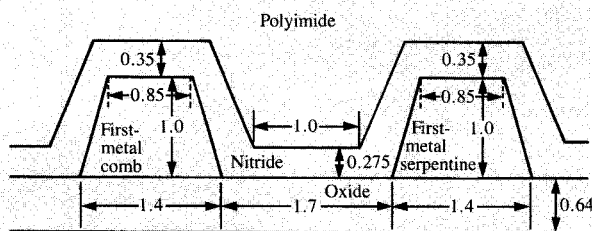
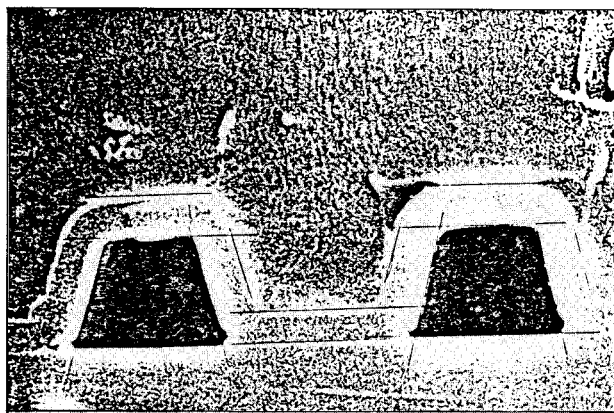


Figure 9

Scanning electron micrograph and derived cross section of first metal. All dimensions are in micrometers.

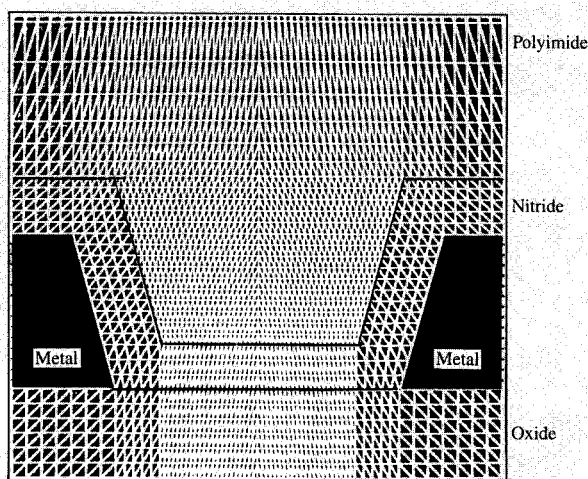


Figure 10

Typical finite-element mesh used to simulate first-metal capacitance.

models used to verify the algorithm were tailored to match the structure of each device that was characterized

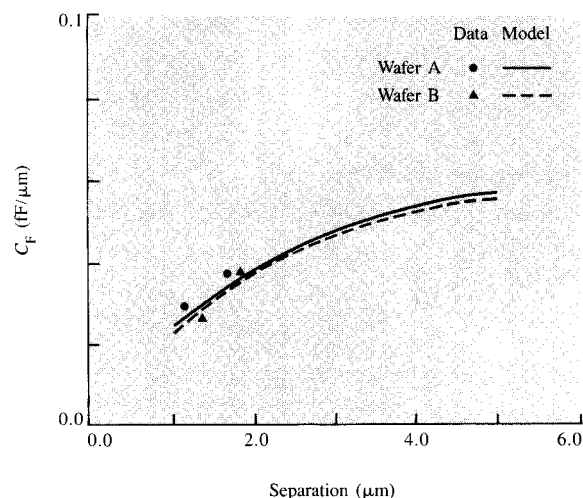


Figure 11

Measured and modeled first-metal fringe capacitances. Each of the four points represents the average of many measurements across a wafer. The uniformity of the data within a wafer was excellent. The structure is shown in Figs. 7 and 9.

electrically. **Figure 9** shows a first-metal cross section obtained in this fashion, and **Figure 10** shows the finite-element mesh used to model this structure. The silicon surface was treated as a ground plane for all of the models.

The results of this verification effort all show excellent agreement between measured and simulated capacitances. First, we examine the results found for first metal. **Figure 11** shows the measured and modeled fringe capacitances for first metal. The fringe capacitance decreases with decreasing separation between lines because the adjacent lines shield the substrate from the field at the edges of the metal. At wide spacings between lines the fringe capacitance is 50% of the total. There is excellent agreement between the model and the data. The capacitance between adjacent first-metal lines C_L is shown in **Figure 12** as a function of separation between lines at the bottom of the metal. This coupling capacitance increases with decreasing separation. Of the 0.3-fF/ μm total capacitance of a line with nearest neighbors 1.0 micrometer away, 46% is line-to-line capacitance and 16% is fringe capacitance. The rapid increase in line-to-line capacitance with decreasing separation is caused by the increasing ratio of metal height to separation between adjacent lines and the relatively high permittivity of the nitride filling the region between closely spaced adjacent lines. The separation and height are equal at 1.0 micrometer.

The second-metal structure is similar to the first, except that the metal is deposited over a much thicker insulating layer and there is no nitride overcoat. This increases the relative size of the line-to-line capacitance and decreases the fringe and area components. For this structure with a 1.0-

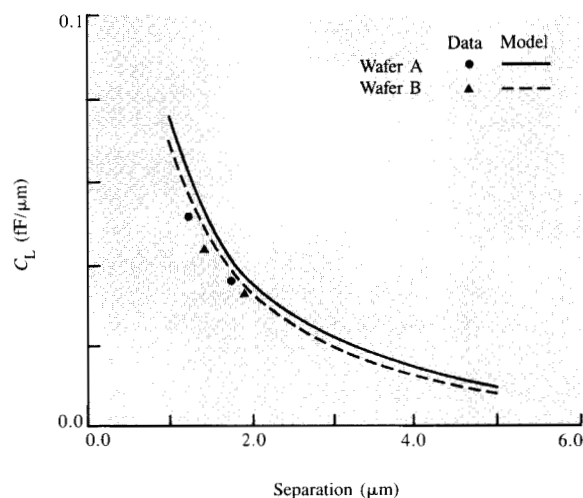


Figure 12

Measured and modeled first-metal line-to-line capacitances. The structure is shown in Figs. 7 and 9.

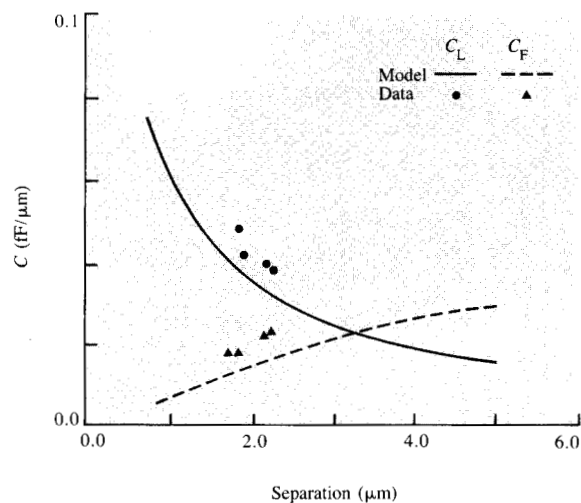


Figure 13

Measured and modeled second-metal line-to-line and fringe-to-substrate capacitances. The structure is shown in Fig. 8.

micrometer separation between lines, 58% of the total is line-to-line and 7% is fringe capacitance. C_F and C_L are shown for second metal in **Figure 13**.

The polycide structure includes three different passivating layers. Its line-to-line component is much smaller than the fringe component, as it is three times thinner than the metal layer. As shown in **Figure 14**, there is again good agreement between the model and measured capacitances.

These data not only show that the model is correct, but also illustrate the differences in capacitance among the three wiring conductors. As the underlying insulator increases in thickness, the line-to-line capacitance component dominates the total capacitance. Thinning the conductor decreases the ratio of line-to-line capacitance to total capacitance. These differences show that capacitance can play a role in optimal matching of fabrication technology to circuit application.

Three-dimensional modeling

The three-dimensional capability of the FIERCE model was used to simulate the capacitance of a second-metal line crossing a first-metal line, as shown in **Figure 15**. The results are shown in **Table 2**. The modeled capacitance, C_{model} , between the crossing lines is five times the capacitance, C_{area} , calculated from the capacitance per unit area and the overlap area. It is also more than twice that found when the capacitance is estimated by summing two-dimensional components. The two-dimensional components were obtained by considering the three-dimensional problem as the sum of separate two-dimensional cross sections. This result emphasizes the need for a three-dimensional capacitance model.

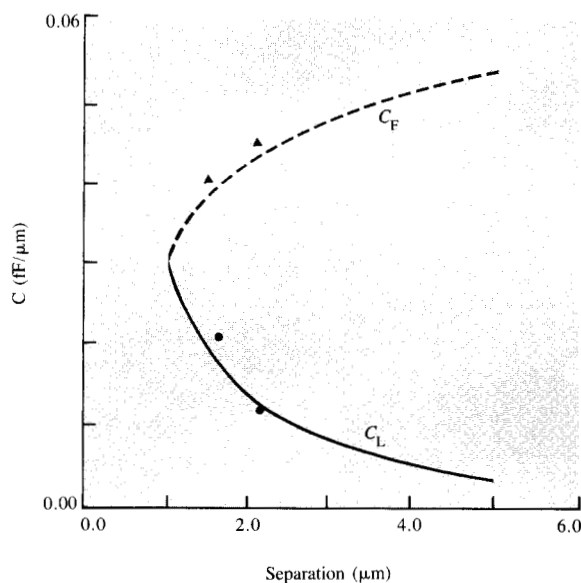


Figure 14

Measured and modeled polycide line-to-line and fringe-to-substrate capacitances. The structure is shown in Fig. 6.

Increasing the separation between conductors decreases the coupling capacitance but increases the error in estimating that capacitance with two-dimensional models. A 73% increase in separation only decreases the coupling capacitance by 30% because of the dominance of the fringe components.

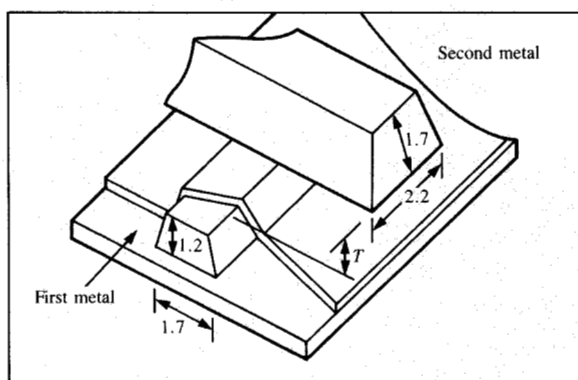


Figure 15

Schematic of second-metal line crossing first-metal line. Dimensions are in micrometers.

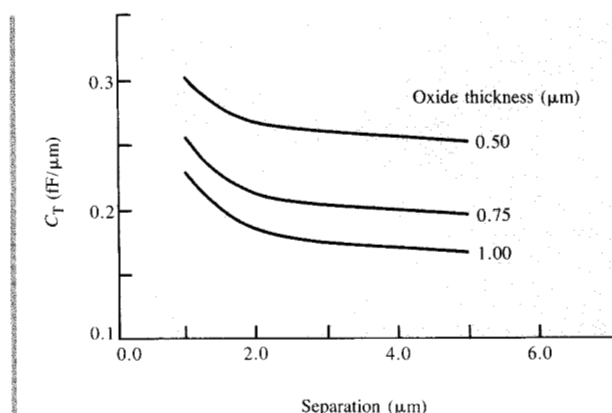


Figure 16

Total capacitance of 1.7-μm-wide, 1.2-μm-thick metal lines versus separation between lines with oxide equivalent insulator thicknesses of 0.5, 0.75, and 1.0 μm.

Table 2 Capacitance of a second-metal line crossing a first-metal line.

T (μm)	C_{model} (fF)	C_{area} (fF)	$C_{\text{model}}/C_{\text{area}}$
1.30	0.52	0.10	5.2
0.75	0.67	0.17	3.9

Unfortunately, additional development effort is required before three-dimensional models can be used easily and routinely. Recent work [18] in the modeling of three-dimensional structures found in VLSI technologies and the

advent of automatic mesh generation [19] will allow easier application of the powerful solution algorithms found in the FIERCE program.

Circuit implications

Some circuit implications of capacitance in VLSI circuits are power, performance, noise immunity, and for dynamic memory cells, the signal at the sense amplifier. In **Figure 16** the total capacitance of a 1.7-μm-wide first-metal line is displayed as a function of the separation between lines for three insulator thicknesses. For widely spaced lines, doubling the insulator thickness only reduces the total capacitance by one third. This is because of the dominance of fringe capacitance between the line and the substrate. At 1.0-micrometer spacing between the lines, doubling the thickness of the insulator provides less than a 25% reduction in capacitance because the presence of the adjacent lines now adds to the total edge capacitance. The rate of increase of total capacitance with decreased separation is greater for thicker insulators because a larger fraction of the capacitance is due to the coupling between adjacent lines. Since wiring capacitance may dominate circuit performance in critical logical paths, it is well worth the effort to examine the technology and layout changes necessary to reduce it.

In addition to adding capacitive loading to a circuit, the proximity of adjacent signal lines may also add noise via capacitive coupling. The coupling factor F is defined as the ratio of the capacitance between a given signal line and its neighbors to its total capacitance. Assuming that the signal line is driven by a relatively high impedance and that two adjacent lines switch simultaneously, the maximum coupling factor is

$$F = 2 \cdot C_I / C_T. \quad (9)$$

F is then the maximum logical voltage swing that may be coupled into a circuit from adjacent signal lines. **Figure 17** shows the coupling factor versus line separation for the same three insulator thicknesses and conductor used in Fig. 16. By assuming that 50% of the capacitance that a circuit must drive is wiring capacitance and 50% is gate capacitance, a maximum allowable coupling factor of 0.4 is found, if no more than 20% of the logical voltage swing is tolerable as a noise signal. This limits the minimum pitch (line plus space combination) to 3.7 micrometers for a 1.0-micrometer insulator thickness and 2.9 micrometers for a 0.5-micrometer insulator. As can be seen in Fig. 17, a tight pitch with an acceptable noise coupling implies that total capacitance must be increased. This increased capacitance will result in reduced performance and/or increased power. This trend will not occur if conductor thicknesses are scaled with insulator thicknesses. While this may be possible for signal lines, reduced conductor thickness is not an option for power buses or clock lines. One implication is that in future technologies there will be separation of power distribution

and signal distribution functions between two different levels of wiring. This trend may already be observed to some extent in present double-level metal technologies.

One possible method of reducing the capacitance between adjacent lines is to reduce the permittivity of the embedding dielectric layers. **Figure 18** shows the effect of thinning and eliminating the passivating nitride layer. Since this material has roughly twice the permittivity of SiO_2 or polyimide, this results in a significant decrease in the line-to-line capacitance.

Since this simplistic analysis does not consider either the noise coupling through or the current sinking capability of the active devices, the coupling factor may be over- or under-estimated. In spite of this, it can be seen that noise coupling may be a more stringent limit to metal pitch than the capability to fabricate dense wiring. Thus, capacitance, resistance, and density all play important and interactive roles in the design of new VLSI logic technologies.

Line-to-line capacitance may also have a significant effect on the signal of a dynamic memory. The signal presented to the sense amplifier in a dynamic memory is proportional to the storage node capacitance and inversely proportional to the total capacitance of the bit line and the storage node. The signal will be reduced because of the capacitive coupling to the adjacent lines.

$$\text{Signal} \propto \frac{1}{C_T + C_B} \left(1 - \frac{KC_L}{C_T + C_B} \right),$$

where C_L is the coupling capacitance to an adjacent bit line, C_T is the total capacitance of the bit line conductor, C_B is the capacitance connected to the bit line due to factors other than the bit line conductor, and K depends on the layout of the array and the signal polarity on adjacent bit lines. For a folded bit line array, the maximum value of K is 2, and for an open bit line array, the maximum value is 4. To estimate the importance of this effect, C_B is assumed equal to C_T for widely spaced first-metal bit lines (0.26 fF per micrometer) and K is set to 2.

As illustrated in **Figure 19**, the effect of coupling is increased as the bit pitch decreases because of increasing C_L . For an 8.0-micrometer bit pitch, the 1.0-micrometer insulator offers 18% more signal than the 0.5-micrometer insulator. This benefit is reduced to 15% at a 5.0-micrometer pitch and to less than 8% at 3.0 micrometers. Thus the advantage of thicker insulators is reduced as the bit pitch is decreased due to the increasing influence of adjacent line coupling.

Even diffused bit lines are not immune to this problem. The Silicon and Aluminum Metal Oxide Semiconductor (SAMOS) technology has a polysilicon field shield over thin oxide between adjacent diffusions [20]. The field shield is tied to the substrate bias to ensure that this device is always "off." Although the structure shown in **Figure 20** has lower coupling between adjacent lines than that found with thick

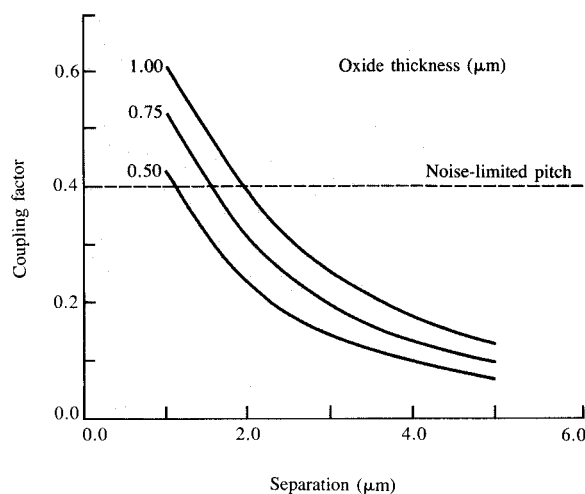


Figure 17

Coupling factor F for 1.7- μm -wide, 1.2- μm -thick metal lines versus separation between lines with oxide equivalent insulator thicknesses of 0.5, 0.75, and 1.0 μm .

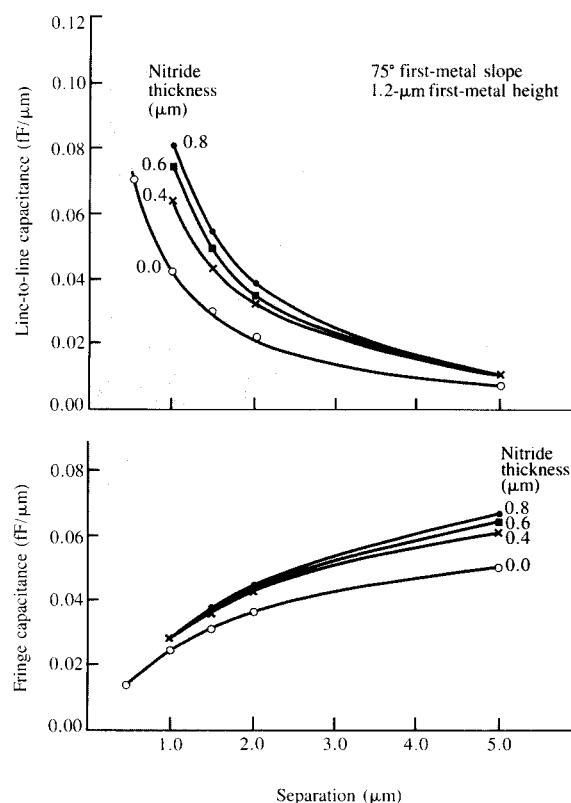


Figure 18

Simulated line-to-line and fringe-to-substrate capacitances for 1.7- μm -wide, 1.2- μm -thick metal lines versus separation between lines with four nitride thicknesses.

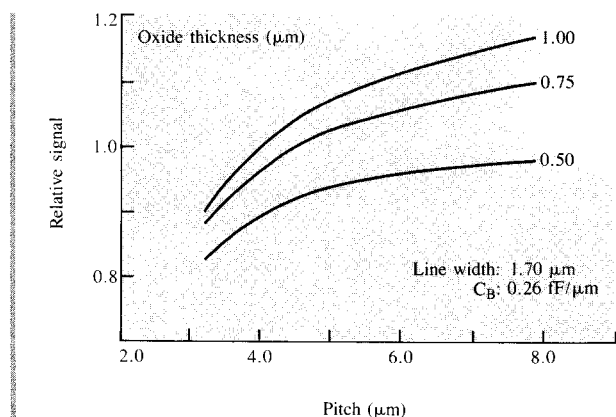


Figure 19

Relative signal for a dynamic memory array with metal bit lines versus bit line pitch for three oxide thicknesses.

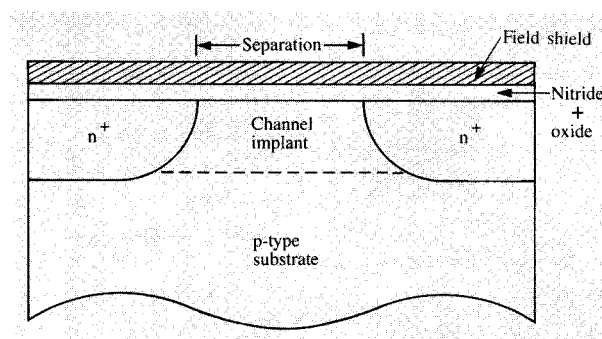


Figure 20

The field-shield structure for the SAMOS technology.

oxide isolated structures, the coupling can still affect the signal for a diffused bit line dynamic memory array. **Figure 21** shows the line-to-line coupling between two adjacent diffusions for this technology as modeled with the FIELDAY [14] program. The results show that a 2.4-micrometer separation between diffusions is equivalent to a 1.0-micrometer separation between first-metal lines. The capacitance increases rapidly for diffusion separations of less than 2.5 micrometers. At this separation the depletion regions surrounding the diffusions overlap and mobile holes no longer screen the diffusions from each other. Also, the dielectric permittivity of silicon is three times greater than that for SiO_2 . The importance of mobile carrier screening is illustrated in **Figure 22**, which shows the depletion region edges for two different line separations. Adjacent bit lines in close proximity were avoided in the design of SAMOS dynamic memory products. These all have bit lines

separated by transfer gate and storage node structures, and thus adjacent line coupling does not significantly degrade the signal.

Summary and conclusions

We have demonstrated a flexible and powerful two- and three-dimensional modeling tool for VLSI wiring capacitance. The FIERCE program will simulate large structures of general shape. The finite-element method allows simulation of complex combinations of different dielectric and conducting materials. Computational efficiency in solving large systems of linear equations is provided by the incomplete Cholesky-conjugate gradient method.

The program was verified by comparison of simulated and measured capacitance of the polycide, first-metal, and second-metal conductors in a 1.25-micrometer VLSI technology. There was good agreement between measured and simulated line-to-line and fringe-to-substrate capacitances for all three wiring structures.

The three-dimensional capability of FIERCE was demonstrated by simulation of the capacitance of crossing metal lines. Results show that the capacitance is twice that predicted by composite two-dimensional models.

The effect of the capacitance between adjacent lines on logic and memory circuits was investigated. As metal pitch is reduced, increased noise coupling and reduced bit line signal are expected. Although we have demonstrated the capability to fabricate aluminum lines on a 2.4-micrometer pitch, noise coupling may limit the useful pitch to 3.0 to 4.0 micrometers in VLSI logic applications. Coupling capacitance may also reduce the signal on a metal or diffused bit line. With a metal bit line over a 1.0-micrometer insulator, a 17% reduction in signal is expected at a 4.0-micrometer pitch. This is caused by increased total capacitance and the capacitive coupling of opposite polarity signals from adjacent bit lines. These limitations point out the strong need for careful consideration of capacitive effects when designing VLSI circuits and technology.

Clearly, the capabilities of this and similar models are inadequate for many applications. For example, although the present algorithm will simulate a very large and complicated structure, the mesh generation for such a problem requires a Herculean effort. Ultimately, we can see the need for this type of model to examine, in three dimensions, the bit line capacitance of a DRAM. At present the mesh generation capability can realistically tackle only a very simplified version of the actual structure. In addition, it would be desirable to model the semiconductor, insulators, and conductors at once. Although the FIELDAY program will do this, it is not capable of modeling large three-dimensional structures in a cost-effective fashion. Thus development effort needs to be spent on integrating software that will describe the structure to be modeled to the computer and

will automatically generate the required finite-element mesh. Furthermore, the ability to handle large problems must be extended from the capacitor model to a model that will simulate an active device. This will require new equation-solving algorithms.

In spite of these limitations, the presently available capability is more than adequate to examine trade-offs involved in designing new technologies for VLSI circuits. The challenge is to use this capability to best match technology and circuit application.

Acknowledgments

The authors are indebted to K. Salsburg and C. McMullen for their initial work on the FIERCE program. We thank D. Fitzgerald for his efforts in generating finite-element models and M. Schwartz for her careful measurement of wiring capacitance.

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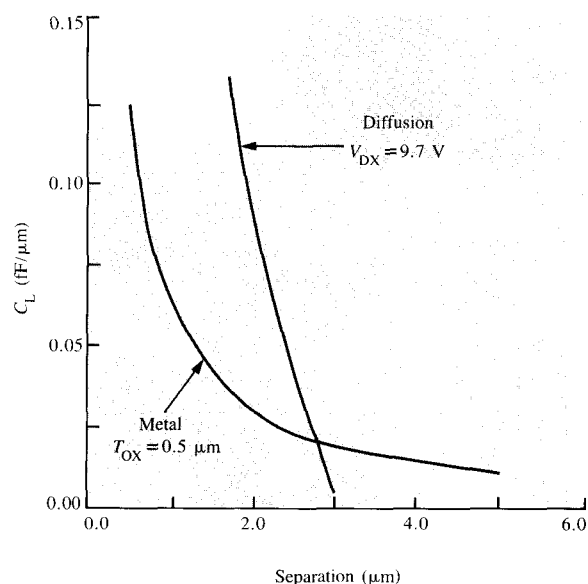


Figure 21

Coupling capacitance for adjacent diffusions in the SAMOS technology versus diffusion separation. The capacitance for first-metal lines is also shown.

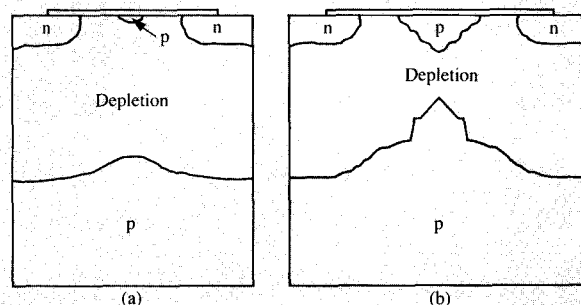


Figure 22

Depletion region shapes for SAMOS diffusions with separations of (a) 1.8 and (b) 3.0 μm.

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