Advanced bipolar transistor modeling: Process and device simulation tools for today's technology

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A series of programs have been developed and linked together for doing advanced transistor modeling. The strategy begins with a process modeling program, SAFEPRO, for predicting two-dimensional impurity profiles. These are input to a two-dimensional device physics modeling program, 2DP, for generating device electrical characteristics. A three-dimensional distributed device model is then assembled by a model generator program (MGP) which, in turn, is used to derive a lumped equivalent-circuit model for numerical circuit analysis. The tools make it possible to do process sensitivity studies, perform process and device optimization, and provide early feedback on technology performance. The approach has recently been used to examine and compare various technologies at IBM.

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Introduction

In recent years bipolar integrated circuit technology has been evolving in the direction of shallow-junction devices with minimum horizontal active region dimensions. This trend has been the result of continual improvements in lithographic capability such that additional horizontal shrinkage has necessitated a reduction in vertical dimensions as well. Also, the recent development of a polysilicon base contact [1–5] has allowed the further reduction of the extrinsic (nonactive) portion of the bipolar device, thus causing circuit performance to be more closely tied to intrinsic (active region) device performance. These reductions in transistor size, both horizontally and vertically, have all but eliminated the usefulness of simple one-dimensional transistor models. The need is clearly evident for two- and three-dimensional modeling capability in order to develop accurate equivalent-circuit device models for circuit simulation.

In addition to the need for two- and three-dimensional modeling, there has been an increasing desire to do predictive modeling. That is, one would like to know the effect of changes in process and device technology upon circuit performance without having to first produce prototype hardware. A predictive model capability must provide accurate modeling of process physics in order to

determine resultant impurity profiles, semiconductor device physics so as to predict device current and voltage relationships, and circuit behavior in order to allow simulations of circuit power and performance for the particular technology under consideration. Predictive modeling is understandably difficult. Usually not all physics is well understood. Consequently, there is often the need for a certain amount of learning with early test structures in order to obtain certain fundamental modeling parameters. However, the payoff is considerable. The value of being able to optimize a new process, study the process tolerances of a new technology, or obtain rapid feedback on a proposed process change is tremendous.

Standard bipolar modeling practice has been to obtain measured data on a reasonable cross section of good-quality transistors, resistors, and diodes before accurate equivalent-circuit models could be developed for circuit simulation. This practice works well as long as the technology is well known and reasonably fixed. Today, however, the technology is evolving at an ever-increasing pace. Consequently, the requirement for fast turnaround time is becoming increasingly severe.

This paper, along with the three following papers, describes a bipolar modeling methodology that has been developed at IBM's GTD East Fishkill facility over the past several years [6]. The technique involves a series of programs that have been developed and linked together for performing the various pieces of the modeling job. The modeling operation begins with a process modeling program, SAFEPRO (Semiconductor Applications of Finite Elements for PROcess modeling), for predicting two-dimensional impurity profiles. These are inputted to a two-dimensional device physics modeling program called 2DP for generating device electrical characteristics for a two-dimensional transistor. The output of 2DP is used to load a device model generation program, MGP, which assembles a fully three-dimensional distributed transistor model built with the 2DP-generated device characteristics. MGP then derives a lumped, equivalent-circuit model having the same terminal characteristics as the fully distributed model. The output of the MGP program is then used to perform numerical circuit analysis to determine circuit behavior using a circuit analysis program such as IBM's ASTAP program [7].

This paper gives a general description of the transistor modeling methodology. Each of the three modeling programs for performing process modeling, device physics modeling, and equivalent-circuit model generation is briefly described along with the software links for automating the interfacing of the programs. An example of the application of the modeling approach is also given to illustrate the value of these tools to the development of advanced bipolar technology. The following three papers in this issue [8–10] describe in detail the three programs SAFEPRO, 2DP, and MGP. The modeling methodology and tools described here have been developed at IBM for use in modeling advanced three-dimensional bipolar devices. Various other approaches for modeling FET and bipolar structures in one, two, and three dimensions are described in the literature (e.g., [11–16]).

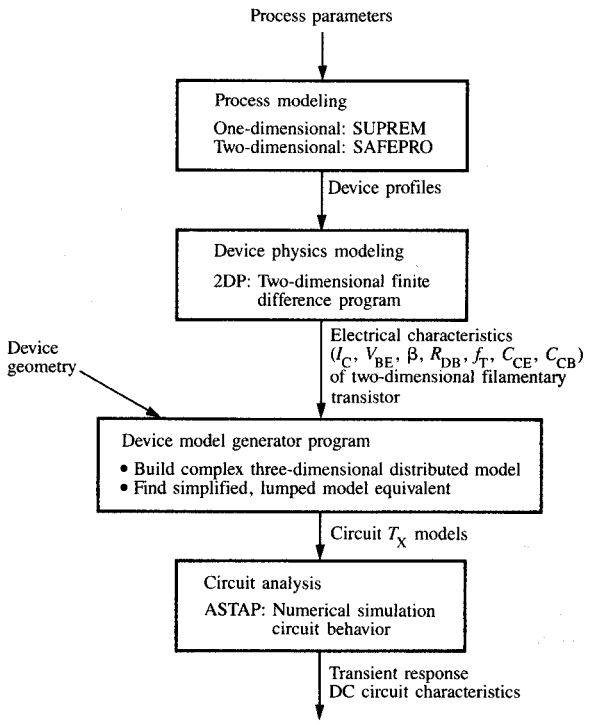

Figure 1

Advanced bipolar modeling strategy flowchart.

General description of the modeling approach

The objective of this work can be stated very simply as follows: the ability to relate process technology and profile changes to device and circuit behavior by way of program models. The achievement of this objective allows one to obtain rapid turnaround time in performing process sensitivity studies, process optimization, statistical device modeling, and early feedback on technology performance.

Figure 1 shows a flowchart describing the strategy for modeling advanced bipolar transistors within IBM. The process modeling program SAFEPRO receives as input a description of the process in terms of hot process steps, i.e., diffusion times and temperatures, implant dose, impurity types, etc. The output of the SAFEPRO program is a set of two-dimensional profiles of arsenic and boron (or other dopant types) for the device emitter, intrinsic base, and extrinsic base regions. The device physics simulation

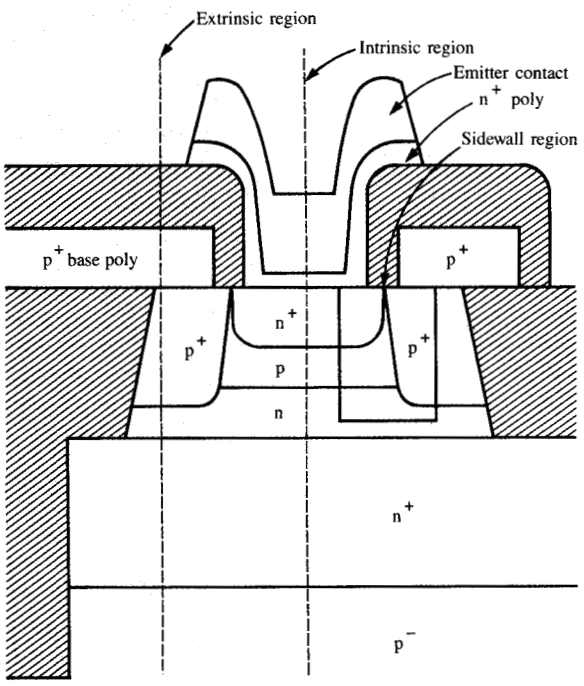

Figure 2

Advanced bipolar transistor cross section.

program 2DP receives as input the SAFEPRO 2D profiles and calculates a set of electrical characteristics for a two-dimensional transistor at each bias point (as indicated in Fig. 1). These output files are fed into the MGP program along with the transistor geometry and are used to generate an equivalent-circuit transistor model, as shown. The transistor model is then used to build a fully integrated circuit model for simulating via the ASTAP program to obtain the circuit's transient response and dc characteristics.

• *Modeling the process*

In general, there is an interest in accurately modeling all the processing steps in today's submicrometer technology with two-dimensional resolution. This is a formidable task involving the understanding of the physics/chemistry of diffusion, ion implantation, oxidation, epitaxial growth, etching, deposition of various types, pattern definition, etc. In this effort we have concentrated on first modeling diffusion and ion implantation. More recently effort is being directed toward modeling two-dimensional oxidation, epitaxial growth, etc. However, with the capability to perform two-dimensional modeling of diffusion and implantation alone, many of today's advanced bipolar structures can be adequately modeled in regard to predicting end-of-process impurity profiles.

The SAFEPRO program is a two-dimensional, finite-element, process-modeling program which, at the time this work was done, simulated the processes of diffusion and ion implantation. The program simulates transport by both diffusion and drift and allows for the proper treatment of two-species interaction due to the electric field effect. Both vacancy-enhanced diffusion and oxidation-enhanced diffusion are treated by the program, as is the effect of arsenic clustering. The effect of the self-induced electric field due to a steep impurity gradient is, of course, included in the physics built into the program. Diffusion from a polysilicon-to-monosilicon interface is a very important feature of the program which, of necessity, involves the possible use of a segregation coefficient and interface barrier at the poly/monosilicon interface. (The reader is directed to the companion paper [8] for a description of the physics and mathematics upon which the SAFEPRO program is based.)

Figure 2 shows a cross-sectional drawing of a typical submicrometer bipolar transistor. Impurity profiles might be expected to be one-dimensional along the dashed lines but have a two-dimensional nature inside the rectangle shown. For any given process, experimental SIMS (Secondary Ion Mass Spectroscopy) profiles can be obtained (when process hardware is available) for describing the profiles along the dashed lines, but there is not an accurate experimental method available for obtaining the two-dimensional contours in the region of the emitter and base perimeters. The SAFEPRO 2D impurity profiles are generated within a solution region large enough that the profiles along the vertical edges of the solution rectangle are essentially one-dimensional.

Of particular interest is the shape of the doping profiles in the region identified as the sidewall region in Fig. 2 where the emitter edge, intrinsic base, and extrinsic base profiles essentially merge. Experience has shown that for small micrometer-size emitters, the device characteristic is a strong function of the doping contours in this region. In order to obtain a two-dimensional solution of this region with a high level of accuracy, SIMS data were first used to check a one-dimensional version of the program in the intrinsic device region and in the extrinsic device region. This allows one to fit several of the less known parameters such as the vacancy-enhanced diffusion parameter, the arsenic clustering effect, and the oxidation-enhanced diffusion coefficient with measured data. Having obtained a good fit, then, along the side boundaries of the sidewall solution region, the program is used to obtain a full two-dimensional solution in the entire sidewall region. (Once all the diffusion parameters are known, the user can continually use the program as a two-dimensional program without the need for performing one-dimensional solutions on the boundaries.)

Shown in **Figure 3** is a typical set of simulation doping contours for an advanced bipolar transistor with polysilicon base and emitter contacts, as shown in Fig. 2. **Figure 4** is a

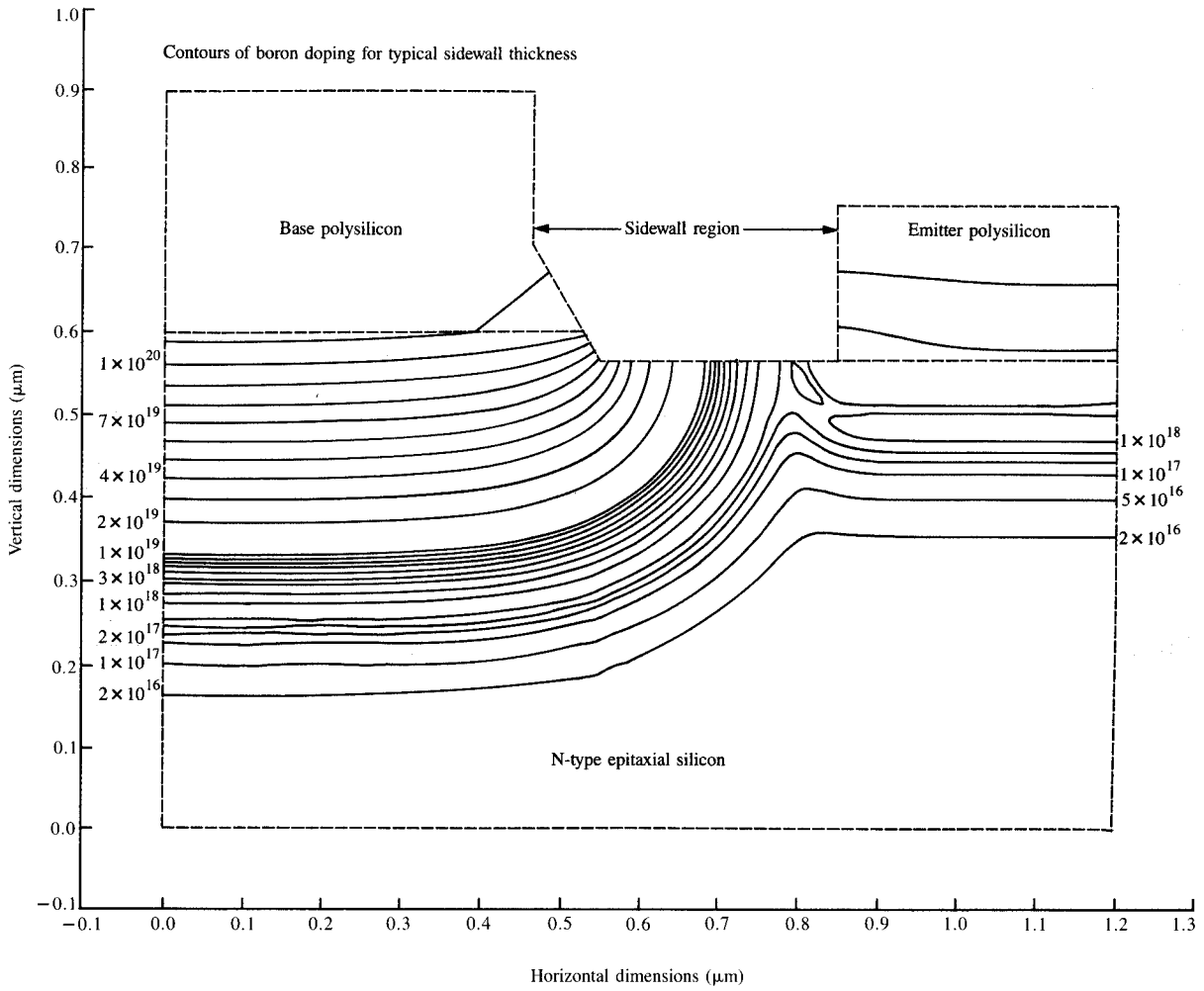

Figure 3

Simulated two-dimensional process model contours for the bipolar device shown in Fig. 2.

blow-up of the Fig. 3 contours showing the sidewall region in greater detail. Arsenic emitter doping contours have been superimposed on the boron base profiles in Fig. 4 and the base-emitter junction has been delineated. The boron concentration at the emitter-base junction, which is strongly influenced by the proximity of the extrinsic base profile to the emitter profile within the sidewall region, is the basic factor in determining the emitter-base breakdown voltage (BV_{EBO}). The link-up of the extrinsic base profiles is another area of interest, since it has a strong influence on the predicted forward and inverse punch-through voltages (BV_{CES} and BV_{ECS}) and the device base resistance. It is also known that the device current gain will be a strong function of the boron concentration in the sidewall vicinity of the emitter since this will strongly impact the sidewall injected hole current.

Figure 4 illustrates one of the key features of the SAFEPRO program, that is, the interaction of the arsenic and boron concentration gradients during the diffusion process. The electric field due to the steep arsenic gradient causes a portion of the lighter boron atoms to drift back into the emitter during the emitter drive-in cycle. This effect causes a characteristic dip in the boron concentration right at the emitter-base junction. SAFEPRO properly models this physical effect, which can be seen in the contours on Figs. 3 and 4. This interaction effect is even more visible in **Figure 5**, which shows the predicted vertical one-dimensional profile through the intrinsic region of the transistor.

After SAFEPRO generates the two-dimensional profiles, a software link is used to interpolate and save solution points from the SAFEPRO finite-element grid in a finite-difference grid for the 2DP program. In addition, the subcollector

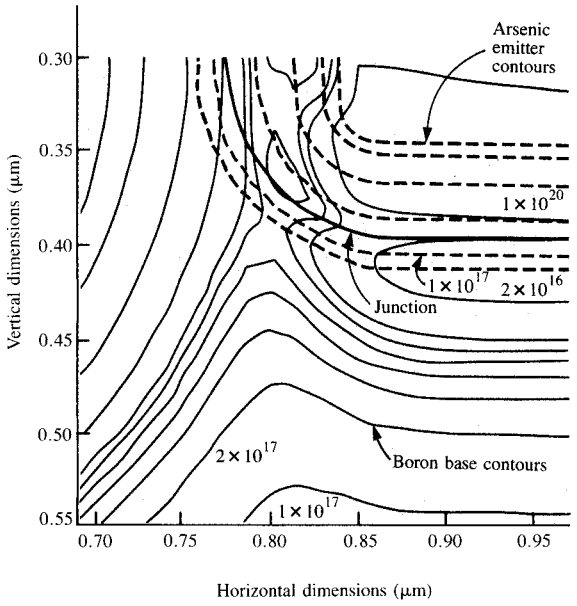

Figure 4

Magnified view of the predicted doping contours shown in Fig. 3.

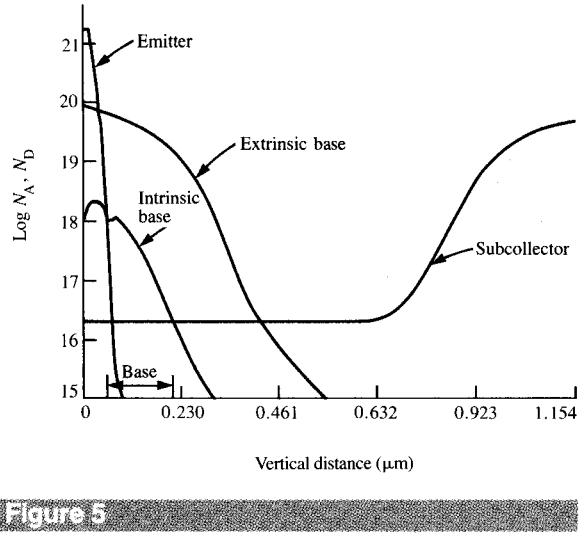

Figure 5

Predicted vertical profile in the intrinsic device region.

profile is superimposed upon the SAFEPRO-generated base and emitter profiles, and the solution region is extended toward the intrinsic and extrinsic regions of the device, as specified by the device horizontal geometry, until the entire set of device profiles is defined. The modeling flow now moves into the device physics modeling program 2DP.

- *The device physics simulator*

The 2DP program uses a finite difference method to numerically solve Poisson's equation and the electron and hole continuity equations in two dimensions. A separate dc solution is found for each combination of base-emitter and base-collector bias. A full set of 35 or more solutions was selected to completely model a transistor for forward and inverse operation. To characterize the forward mode a set of forward emitter-base biases is applied for each of several collector-base reverse biases. For inverse mode modeling a reduced set of forward bias base-collector voltages is analyzed. (A limited set of 12 bias cases is sometimes run if there is no requirement for both an accurate inverse model and extensive collector-base voltage variation modeling.)

In addition to solving the coupled set of Poisson's and the continuity equations to calculate the electrostatic potential and the mobile electron and hole concentrations, 2DP solves a set of auxiliary equations to obtain the electron and hole current, the electron and hole Fermi potentials, and the electric field. A bandgap-narrowing (BGN) model is used in the regions of heavy emitter and base doping to calculate an effective intrinsic carrier concentration. This, in turn, is related to the Fermi and electrostatic potentials via Boltzmann statistics. In addition, Shockley-Read-Hall and Auger recombination rates are calculated by the program, along with field-dependent carrier generation rates. (For a detailed description of the physics and mathematics upon which 2DP is based, the reader is referred to the third paper in this series [9].)

All the device dc parameters are calculated at each bias point. These include the collector current I_C, the base current I_B, the current gain $\beta = I_C/I_B$, and the base sheet resistance R_{BS}. In addition, the collector-base capacitance C_{CB} and emitter-base capacitance C_{EB} are found by calculating the change in the device charge by a slight perturbation in collector-base or emitter-base voltage, respectively. The device transit time is then calculated from the other parameters and converted to unity gain-bandwidth product f_t. Consequently, a set of 35 2DP runs yields a full set of device parameters for a two-dimensional transistor: I_C, I_B, β, R_{BS}, C_{CB}, C_{EB}, and f_t versus V_{BE} and V_{CB}. Additionally, the program can be run at various temperatures to obtain the desired parameter temperature dependence.

The program is run in a user-specified device region with finite-difference grid points specified by the user. As stated earlier, the program receives two-dimensional impurity profiles inputted from the SAFEPRO program auto-link. (However, an alternate option for the user is to specify one-dimensional profiles for the emitter and base regions and allow 2DP to determine the two-dimensional nature of the emitter and base junctions by a built-in analytical algorithm.) Boundary conditions are specified by the user at all device contacts and along the entire solution region

boundary. Device symmetry is often assumed in order to reduce the solution region to one half the actual device size. **Figure 6** illustrates a typical 2DP solution showing contours of predicted electron and hole current flow. Output files saved for each 2DP solution contain desired resultant characteristics and calculated parameters as a function of position from the intrinsic device/emitter region to the extrinsic base region. These files are used later to construct the three-dimensional distributed model.

For process optimization studies and process sensitivity calculations, 2DP results may be of immediate interest without going any further toward the generation of an equivalent-circuit model. One question of interest in the development of an advanced transistor, as stated above, is the nature of the "link-up" region between the extrinsic base diffusion and the device intrinsic base region. **Figure 7** shows the predicted base sheet resistance as a function of distance between the emitter and the extrinsic base contact at a given sidewall thickness for various base-emitter biases. The particular example chosen shows a peak in resistivity in the sidewall region at low V_{BE} bias. As the bias increases, conductivity modulation reduces the resistivity in both the intrinsic base and sidewall regions and also is seen to reduce the relative height of the resistivity peak in the sidewall region. This behavior obviously has a direct bearing on the calculated device base resistance.

• *The equivalent-circuit model generator*

The device physics simulation program 2DP analyzes a two-dimensional structure. However, today's micrometer-dimension bipolar transistors are truly three-dimensional devices in that the sidewall portion of the device has a significant influence on the overall device terminal characteristics. Thus, the need exists to do three-dimensional modeling. In concept a three-dimensional device physics simulation program can be written [17]; however, practical use of such a program becomes extremely costly in terms of CPU running time. Also, a more basic need is for a simplified equivalent-circuit model that can be used in numerical circuit analysis programs, such as the IBM ASTAP program. Consequently, rather than develop a three-dimensional device physics simulation program, the approach was taken here to develop an equivalent-circuit model generator program (MGP) that would effectively model a three-dimensional device but that would use as input the output of the 2DP analyses.

The MGP program is loaded by a full set of 35 (or more) 2DP simulations for the various operating bias cases described above. (Alternately, the program may be loaded by actual measured device characteristics, after some manipulation of the data, if these are preferred and available.) Once the program is loaded, devices of various geometries may be modeled for a fixed set of process profiles by merely inputting to MGP the particular device geometry to be modeled. If it is desired to model a process change or study the effect of process variations upon the device behavior, a new set of SAFEPRO and 2DP simulations is done and the MGP program is reloaded with new input.

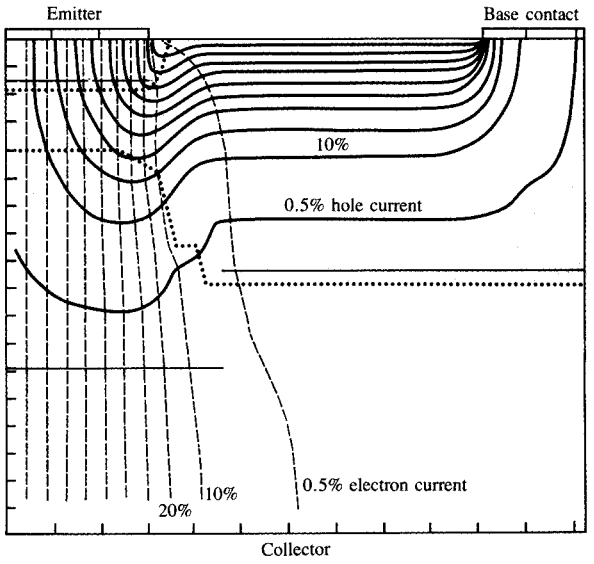

Figure 6

Electron and hole current flow contours for typical 2DP solution.

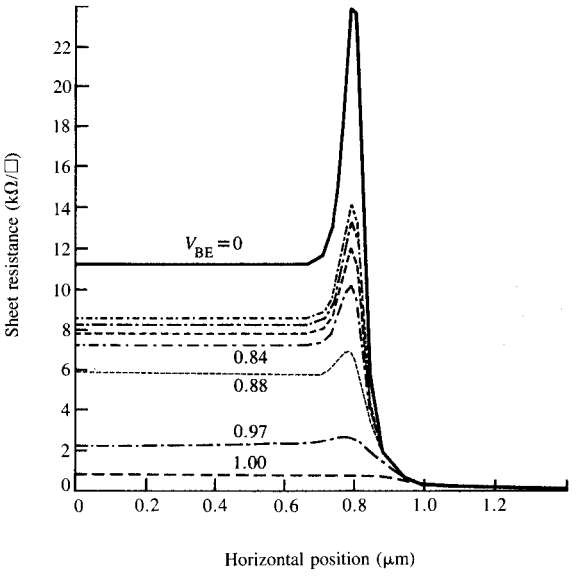

Figure 7

Base sheet resistance versus position between intrinsic and extrinsic base for given sidewall thickness and various base-emitter biases.

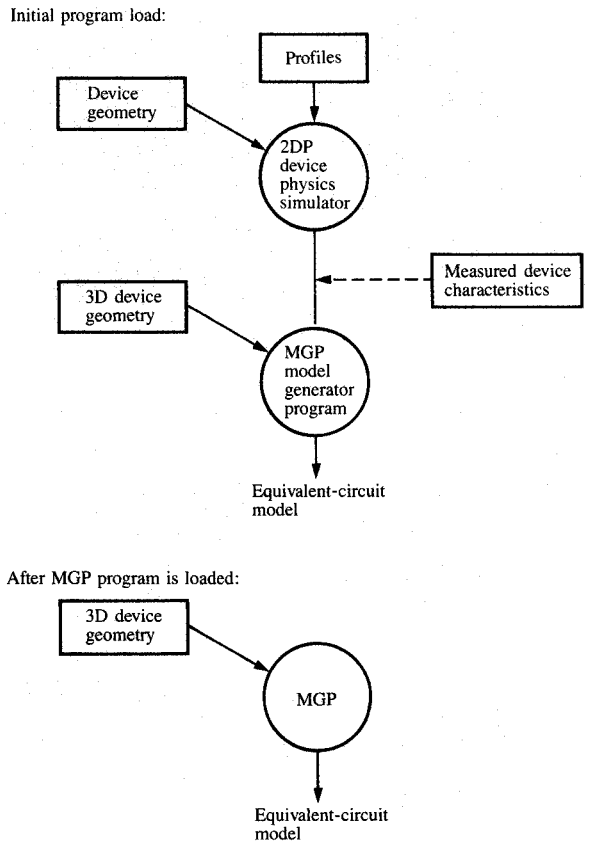

Figure 8

Equivalent-circuit model generator program input loading strategy.

Typically, once a process has solidified, the program need not be reloaded except for the generation of statistical models and/or for sensitivity studies. This concept of 2DP-MGP linkage is illustrated in **Figure 8**.

The first step of the MGP program is to build a complex three-dimensional distributed model. The procedure is illustrated in **Figure 9**. Filamentary transistors are defined for the intrinsic device region with characteristics determined from the intrinsic device portion of the 2DP simulations. The intrinsic device region is divided into $m \times n$ sections, each with a filamentary transistor, and linked together by way of distributed base resistances. Emitter and collector nodes are considered in general to be equipotential. Typically, 5×5 intrinsic filamentary devices are used.

In the sidewall portion of the device, additional filamentary transistor sections are connected into the distributed model to account for the sidewall region device action. These transistor sections again have characteristics determined from the sidewall portion of the 2DP analyses. In the extrinsic part of the device, collector-base diode sections and distributed base resistance elements are interconnected and hooked to the sidewall section resistive elements. Finally, additional resistive elements are added to account for resistance of the base polysilicon where it extends over the nondevice, oxide region. The entire distributed model may contain well over 1000 elements which, in most cases, are functions of voltage (or current) and temperature.

A program called MGPLINK has been written to accumulate and sort the results from the various 2DP simulations and store these in a link file for automatic loading into the MGP program. MGPLINK can be used to print useful summary files of the 2DP analyses or to plot device parameter characteristics from the 2DP results by using the ASTAP GRAPHICS program, in addition to providing the front-end loading to the MGP program. For a description of the MGP and MGPLINK programs, the reader is referred to the fourth paper in this series [10].

After the distributed model has been assembled, it is analyzed via the ASTAP circuit analysis program developing a set of terminal characteristics for forward and inverse operation. The MGP program then fits these terminal

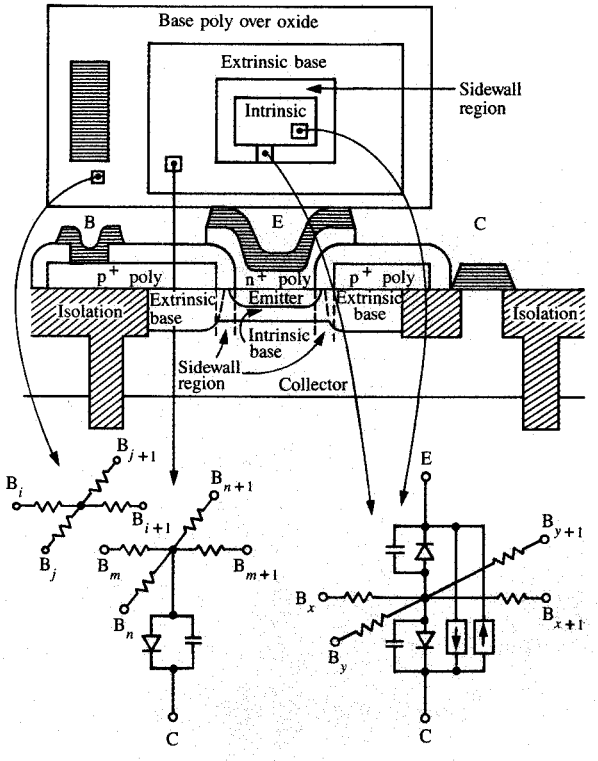

Figure 9

Construction of three-dimensional distributed model by the MGP program.

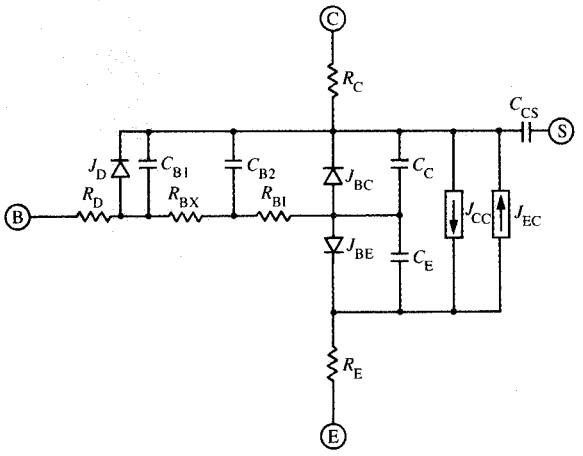

Figure 10

Lumped equivalent-circuit model topology.

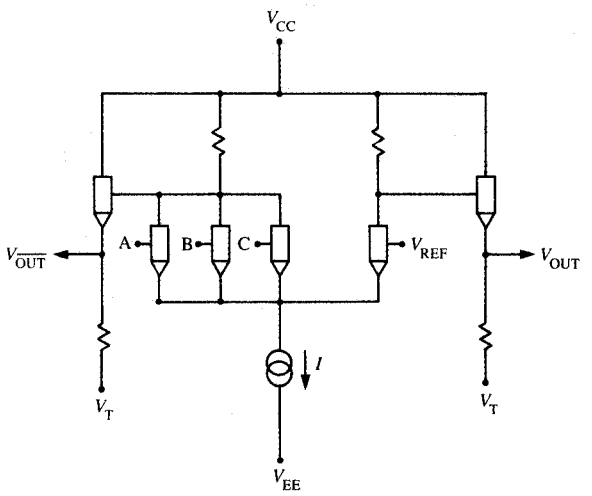

Figure 11

Standard current switch emitter follower (CSEF) circuit used for performance comparisons.

characteristics to a simplified lumped equivalent-circuit model using the topology shown in **Figure 10**. The equivalent-circuit model is based on the bipolar transport model [18] with distributed base sections and single emitter and collector resistances. The elements in the lumped model are represented as equations and/or tables in the model code and are specified as functions of voltage (or current) and temperature. In addition, by specifying these model elements as appropriate functions of independent process parameters, a statistical bipolar model can easily be developed. Such a circuit model finds valuable use in circuit sensitivity analysis and statistical circuit design.

• *Numerical circuit analysis*

One is often interested in performing technology comparisons by using the above equivalent-circuit models to simulate the transient response of some "benchmark" circuit by using a numerical circuit analysis program. Shown in **Figure 11** is a standard current switch emitter follower (CSEF) circuit that is typically used for these comparisons. The circuit shown has a logic fan-in of three and might typically drive three CSEF inputs for each output shown (FI = FO = 3). The MGP program is used to model each transistor in the circuit plus any other devices shown in the current source I, input driving circuits, and/or output loading circuits. **Figure 12** shows a typical set of predicted power-delay curves for various technologies with progressive improvements in performance. The curves were generated by calculating the delay of the Fig. 11 circuit while varying the power by changing the values of the current source and the resistors in the circuit. By using the power-delay approach shown in Fig. 12, MGP-generated models, and the

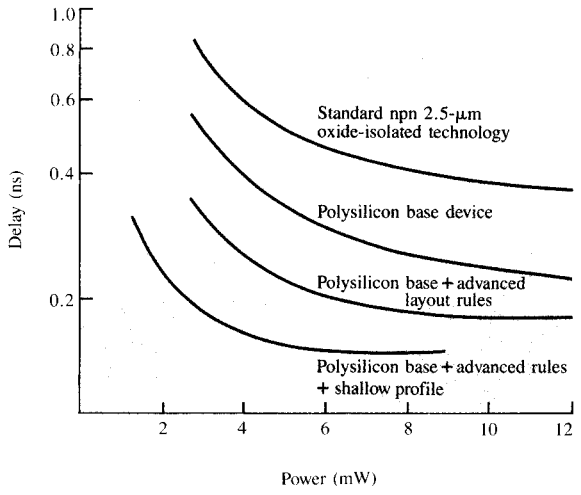

Figure 12

Predicted power-delay curves showing comparison of various technologies.

ASTAP circuit analysis program, numerous technologies and technology improvements have been studied in regard to improving circuit performance.

Application of modeling methodology

One of the key design parameters for the device structure shown in Fig. 2 is the oxide sidewall thickness. Figure 7

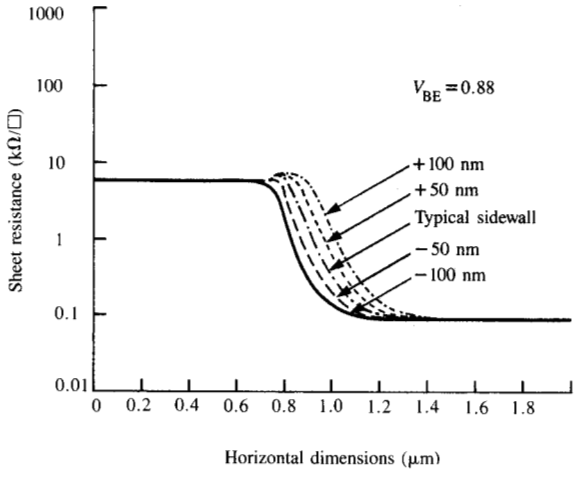

Figure 13

Base sheet resistance versus position between intrinsic and extrinsic base for constant V_{BE} and various sidewall thicknesses.

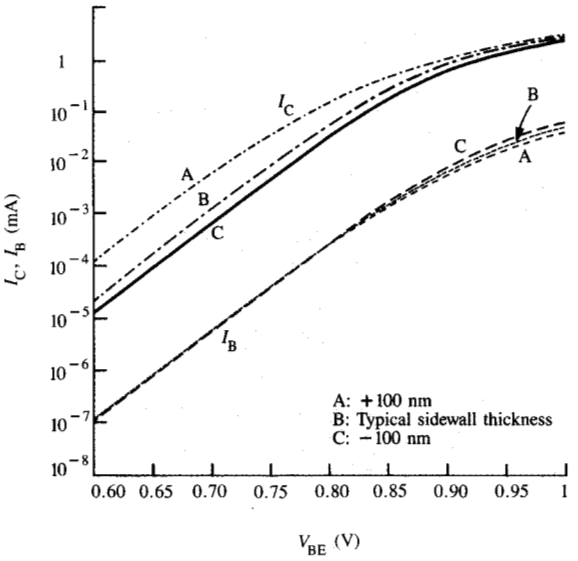

Figure 14

Predicted collector current and base current versus base-emitter bias for a 1.5 × 1.5-μm emitter device at several sidewall thicknesses.

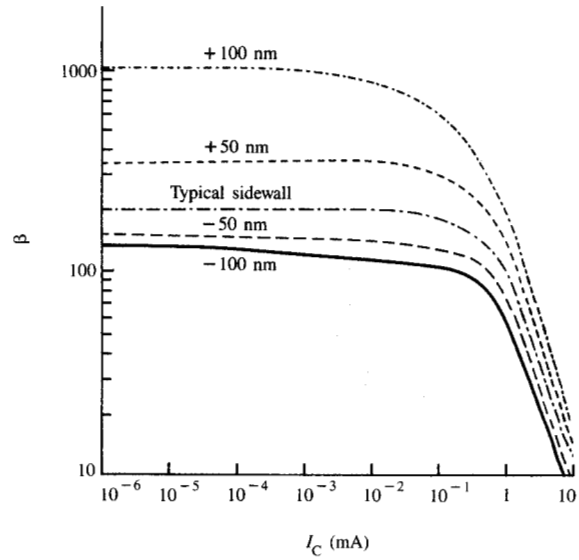

Figure 15

Predicted current gain versus collector current for the device of Fig. 14.

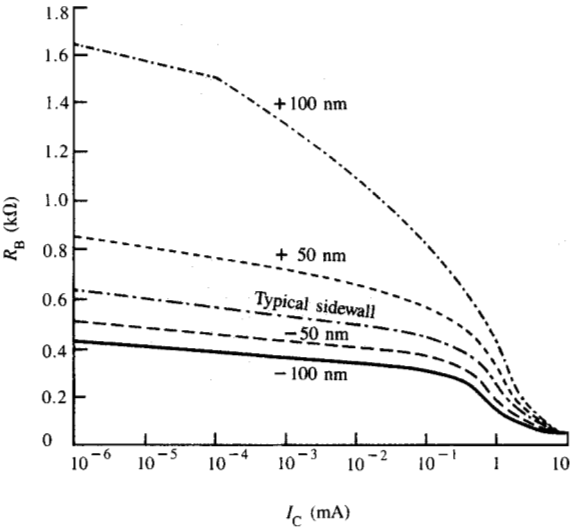

Figure 16

Predicted base resistance versus collector current for the device of Figs. 14 and 15.

showed a 2DP calculation of the base sheet resistivity through the sidewall region for a typical 1.5-μm-emitter-width transistor at a given sidewall thickness and various emitter-base biases. The same transistor simulations are illustrated again in **Figure 13**, where a set of base resistivity calculations for given V_{BE} bias but various sidewall thicknesses is shown. The plot shows that at operating bias a thick sidewall may impact overall device behavior, causing an increase in base resistivity within the sidewall region. At thinner sidewalls, however, the effect disappears, and the program predicts no adverse effect on the total base resistance.

Figures 14–17 show plots of predicted device parameters generated from MGP-derived three-dimensional models for a device with a 1.5 × 1.5-μm emitter at the same sidewall thicknesses as in Fig. 13. **Figure 14** shows the collector and base currents as a function of applied base-emitter bias and **Figure 15** gives the current gain calculated from the Fig. 14 curves. At a thick sidewall the current gain in the sidewall region dramatically increases due to the reduced boron doping attributed to lack of a solid link-up region. Although the collector current and beta are considerably increased at this sidewall thickness, the device is obviously more difficult to control and is prone to punch-through. On the other hand, the model shows that the thin sidewall exhibits a lower beta but obviously less beta sensitivity.

Figure 16 shows predicted total base resistance as a function of collector current for varying sidewall thickness. The base link-up region for the +100-nm case causes a seriously high base resistance, whereas the other cases indicate a much better link-up.

Finally, **Figure 17** presents the predicted emitter and collector capacitances versus collector current for varying sidewall thickness. These plots predict reduced capacitance at thicker sidewall due to the more lightly doped sidewall region. The proper choice of sidewall thickness might be considered a trade-off between base resistance and device capacitance (in addition to the considerations of emitter-base breakdown voltage and emitter-collector punch-through voltage).

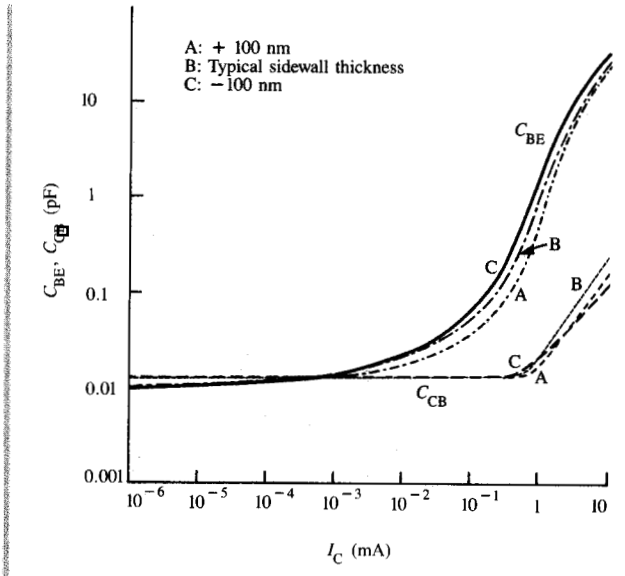

Figure 17

Predicted emitter and collector capacitances versus collector current for the device of Figs. 14–16.

Conclusion

A device modeling methodology has been described that involves the use of two-dimensional process modeling, two-dimensional device physics modeling, and an equivalent-circuit model generator to obtain quasi-three-dimensional device models for numerical circuit analysis. The three simulation programs are linked together by automatic software links in order to load each program with the output of the previous program. This approach to predictive device modeling has made it possible to do process sensitivity studies on advanced bipolar technology, aid process optimization efforts, provide early feedback on the expected performance improvements with technology changes long before any hardware can be obtained, and develop statistical device models for new technology. The entire modeling sequence from process description to circuit simulation can be completed in several working days. The methodology is being used at the IBM East Fishkill laboratory to study various advanced bipolar technologies with polysilicon contacts and shallow profiles.

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