M. A. West
S. M. DeFoster
E. C. Baldwin
R. A. Ziegler

Computer-Controlled Optical Testing of High-Density Printed-Circuit Boards

The increased densities of multi-layer printed-circuit boards have required development of unique approaches to product testing. An optical automatic inspection system developed to test interplanes of the printed-circuit board used in the IBM 3081 processor (TCM board) is described. This system scans the features of the product and locates surface defects of 25.4 μm (1 mil) or larger through changes in reflectivity. It is capable of finding over 90% of the errors on subtractively plated printed-circuit interplanes, as well as shorts and opens of 50 μm or more on glass masters of printed-circuit boards. Alternative approaches to the inspection problem are discussed, together with the technical trade-offs which were made that led to the final system configuration. The tester theory and some hardware/software trade-offs are also covered.

Introduction

Commercial electronic computers have become more powerful since their introduction, yet they have been reduced in physical dimensions from room size to desk size. As their size has decreased and the number of interconnections due to more powerful logic has increased, the printed-circuit boards used have become denser and more complex. Today's printed-circuit boards can be extremely dense, with very small geometries and with many layers, called interplanes.

The cost and difficulty of repairing a multi-layer board after it has been laminated have led to the testing of individual layers of the board for shorts and opens before lamination. For example, the features (land, pad, clearance hole) of the IBM 3081 printed-circuit board (PCB), referred to at IBM as the TCM board [1], are small and closely spaced anywhere on the 600 × 700-mm board surface.

Since the board is constructed of epoxy-fiberglass, it changes dimensions with variations in humidity and temperature. These dimensional changes introduce a degree of uncertainty in the location of features. For example, an individual layer of a TCM board can exhibit a growth or contraction of up to ≈0.1 mm along either axis of the board as the moisture level varies.

Traditionally, PCBs have been tested using a contact-type test system. However, because of the small test-pad sizes and the imprecision of the contact location, a fixed test head may or may not make contact with any given test point. Thus, a reliable non-contact test method had to be developed. One type of non-contact test investigated was visual inspection. However, the high density of the wiring and holes of this board made visual inspection both tedious and inefficient.

Since both contact testing and visual inspection were ruled out, an automated, non-contact testing method was considered. The test method chosen was a computer-controlled image-dissector system. This system determines circuit imperfections as changes of contrast in reflectivity between copper and the dielectric as it scans only the dielectric or only the copper portions of the interplane.

Automated non-contact testing was selected because it provided the best solution to our testing problem at the time

the system was developed in the early 1970s. This paper explains in detail the development, architecture, and trade-offs of this unique electro-optical test system. We discuss the product description and test characteristics, the alternative methods for testing, the reasons and justifications for the choice of method, the engineering trade-offs and decisions made, the strengths and weaknesses of the method, and its future applications.

Overview

Including the ground planes, the printed-circuit board for the IBM 3081, or TCM board, has 12 interplanes for power distribution. These planes are solid copper except for holes that are etched for vias through the board. The board has a woven fiberglass base with copper power planes laminated on both sides. There are over 30 000 holes in each plane, with each hole having a nominal diameter of a little over 1 mm. These via holes are subtractively etched from the copper.

The typical problem with these holes is under-etch, in which the copper is not completely etched away and some metal remains in the hole. If this copper is connected to the side of the hole and is not removed, interplane shorts can develop when the holes are drilled and plated through in the composite board. Figure 1 shows a schematic of a multi-layer board with an interplane short.

There are six signal interplanes (printed circuit layers) in a finished TCM board. These planes are made by an additive copper process on a fiberglass substrate. The lines are nominally 0.081 mm wide.

The typical types of defects found when testing a signal plane are shorts, near-shorts, and opens. A near-short is defined as any extraneous piece of copper that narrows or closes the gap between an adjoining feature to less than an engineering-specified number. Typical printed-circuit features are shown in Fig. 2. An open is a void in a copper line larger than a given limit that causes a certain risk for a circuit to "open."

Each individual plane of the TCM board is made by an additive or a subtractive copper process. In either case, a glass master of the individual planes is used to expose pre-determined features. These features are then added to or subtracted from the individual layer, leaving a finished interplane. Since the glass master is used to generate the finished product, it must be as nearly perfect in quality as possible. Since glass masters may have nicks, scratches, and missing or misplaced features, they must be tested for defects and repaired before being used in production.

All of the various methods which can be used to inspect the individual layers and glass masters of printed circuits can be placed in one of two categories, contact or non-contact.

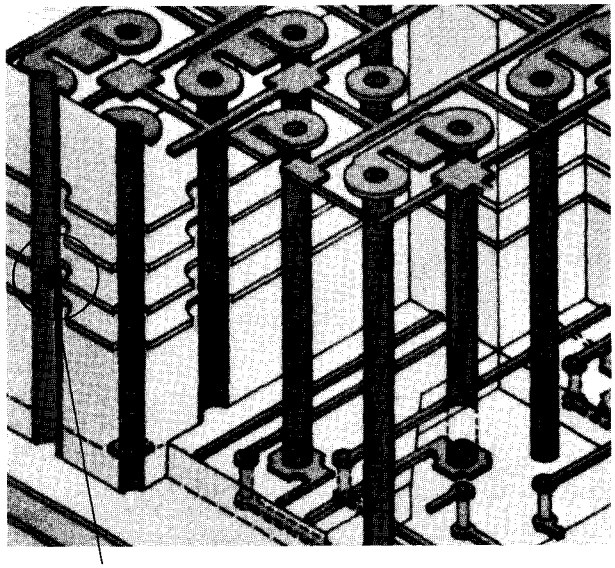

Figure 1 Typical cross section of a TCM board, illustrating a power plane via hole short.

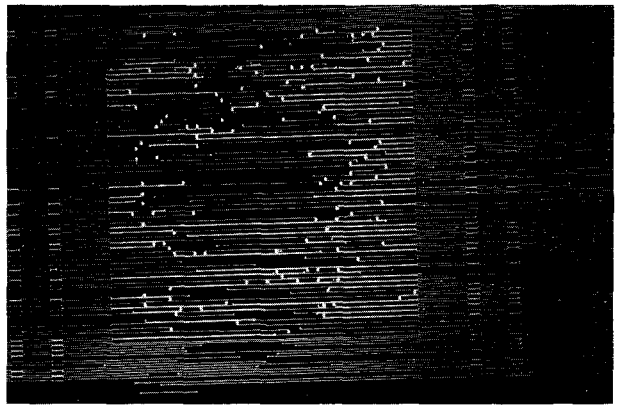

Figure 2 Typical signal lines on a TCM board signal plane. Circles represent via holes. Note that both 45° and 90° line jogs are used.

Contact testing

Contact testing, as the name implies, involves making contact with the product to be tested. The most common type of contact tester is a "bed of nails" machine. It uses probes that make contact with strategically located features and then applies various signals that determine whether or not a short, open, or marginal condition is present. One method of determining a marginal situation is to stress the circuit electrically. Neckdowns or possible opens can be current-

stressed while extraneous copper circuits can be voltage-stressed. The neckdowns tend to open up and the extraneous copper circuits tend to break down (fuse out). The problem with contact testing is that the PCBs are large and the features are very dense, thus making a contact scheme difficult if not impractical.

Non-contact testing

The most obvious method of non-contact testing is visual inspection. This method consists of having the panel inspected by a person for extraneous copper and voids. In early experiments we found that it takes an average of six man-hours to inspect one side of a signal plane, resulting in a very labor-intensive and tedious test.

Another method of non-contact testing is comparison testing. A "good" panel is used as reference and the panel under test and the reference panel are scanned simultaneously and compared. An error is detected if the panel under test differs from the reference [2]. This method has an inherent problem in that when the error size is close to uncertainty and tolerance dimensions, a large number of false errors are generated. Thus, considering that our error size is in fact close to the uncertainty and tolerance values, comparison testing turned out not to be a viable alternative for TCM board products.

There are a number of non-reference methods for inspecting interplanes which are presently being used elsewhere. Most of these methods are independent of part numbers in that they scan the panel, looking only for good and bad characteristics [2–6]. This is similar to the method an inspector uses to look at the printed circuitry with a microscope. This practice works under the assumption that entire lands, lines, or holes are neither misplaced nor missing. Thus, it depends on thoroughly checking the glass master to ensure that it is free of missing or mislocated features.

Test system selection

The system that was selected to test TCM board interplanes was a computer-controlled image-dissector system. Clearance holes on power distribution planes are scanned inside the perimeter looking for extraneous copper. Printed-circuit lines and pads are scanned down the center looking for voids and along the edges looking for extraneous copper. These scans can inspect along the edge of features in steps as small as 0.5 μm, although the typical step is 25 μm. As described in detail later, the scans are generated by modifying data from which the glass master is made.

At the time of initial development in the early 1970s, the required capabilities were not available from commercial vendors. Also, the assumption on which the discarded methods were based was that there were no missing or misplaced features. Since this assumption did not necessarily apply to our glass masters (unless they had first been checked for this type of error), the resulting PCBs made from such masters would have had the same errors, and a scan without comparison to the design data could never have found them. Our system scans the printed-circuit features on the basis of design data, and does it to both glass masters and PCB layers, resulting in a double-checked system wherein misplaced features are found and corrected at the glass master stage before production commences.

The PCB layer is illuminated by a thalium iodide high-intensity discharge lamp (570 nm). The light is delivered to the product through a fiber optic bundle which is designed to deliver a uniform light at a controlled oblique angle to form a dark-field illuminator. The substrates of the panels under test are dyed to provide a high visual contrast using the 570-nm light. Each panel is chemically and/or mechanically cleaned to make the metallic surface of the board a uniform reflector and to enhance contrast.

Error detection is accomplished using a level detector. The light reflected from the surface under test is translated into a video voltage signal. The more light reflected back to the camera, the greater the amplitude of the video signal. An amplitude reference level is generated using a special algorithm. Video voltages above the reference level are defined as being due to copper; those below the reference level are defined as being due to the substrate. Two separate reference levels were developed. One is used when scanning the dielectric material, looking for extraneous copper. The other is applied when scanning copper lines looking for voids or opens.

Many engineering trade-offs were considered when selecting components for this system. When this concept was being developed, charge-coupled devices (CCDs) and other digital imaging devices were not available with the required resolution. Vidicon television tubes were available and exhibited good resolution characteristics, but they exhibited image retention and could not be scanned randomly. The Vidicon was therefore ruled out as too slow for this application.

The image-dissector tube was available and seemed ideally suited for our particular application. It has unique non-storage characteristics and can be randomly scanned. Its output voltage is proportional to the light hitting the face of the tube. The output is also independent of scan velocity. The camera chosen has an image dissector tube with a cathode 44 mm in diameter. The center 645 mm^2 of the tube, called the *handler*, is used in conjunction with a 1× lens to capture a unit area of the PCB layer image. By stepping across the surface and capturing these unit areas at each step, the entire area of the board surface can be examined.

Figure 3 shows the sensitivity characteristics of the image dissector. It clearly illustrates why the 570-nm thalium iodide light was chosen. The light reflected from the product strikes the face of the tube and is amplified, thereby causing an output video voltage. A particular spot may be examined by applying currents to both the x- and y-deflection yokes of the camera. Typical gain exhibited by the tube is 5×10^5 at 10^{-10} A.

The x- and y-deflection currents are originally in digital form obtained from the same data base from which the glass master is created, called *part-number* data. Part-number data basically provide locations of features to be scanned and use up to 1.5 megabytes of memory per panel side. Data for part numbers are stored in the plant's manufacturing data base and can be accessed when needed and stored on the disk file of the host computer.

The system operation involves registration, unit area scanning, comparing scanned against part-number features, recording errors, if any, for later operator inspection, and board indexing to the next unit area where the registration, scanning, etc., are repeated until the entire board surface has been examined. Error detection is accomplished using a level detector which is armed by software before each scan. The video voltage of the features being scanned is compared to the reference level set by an algorithm in the software. When triggered by an error on the board, the level detector interrupts the computer, which then records the x-y location of the error.

Control compensation and correction

The physical properties of the board, as well as the electronics and optics of the test system, introduce a number of distortions. The magnitude of these distortions contributes enough error that it is difficult to use the raw design data to find features on the board without appropriate compensation and correction. Fortunately, all of these distortions in the product and tester can be approximated as linear functions.

After the board is exposed and processed, it shrinks slightly across its width and expands slightly along its length, on the order of 0.1 mm. Therefore, it no longer matches the original data. A linear coefficient of expansion is added to the positioning data of the x-y table that is used to move the product. This correction is added to both x and y and is multiplied by the distance from the center of the board to the feature.

The next correction is to fit the camera image to the original data. The camera introduces a small but significant amount of nonlinear distortion to the video image of the part. This nonlinear distortion cannot be corrected electronically in any simple manner. The first step in correcting this distortion involves dividing the 645-mm^2 handler area into a mosaic of 25 equal parts, called *partitions*. These smaller squares have been found to include a piece of the distorted image small enough that the distortion in each small piece can be approximated linearly. A linear correction is then made with software on each of the 25 parts (see later discussion).

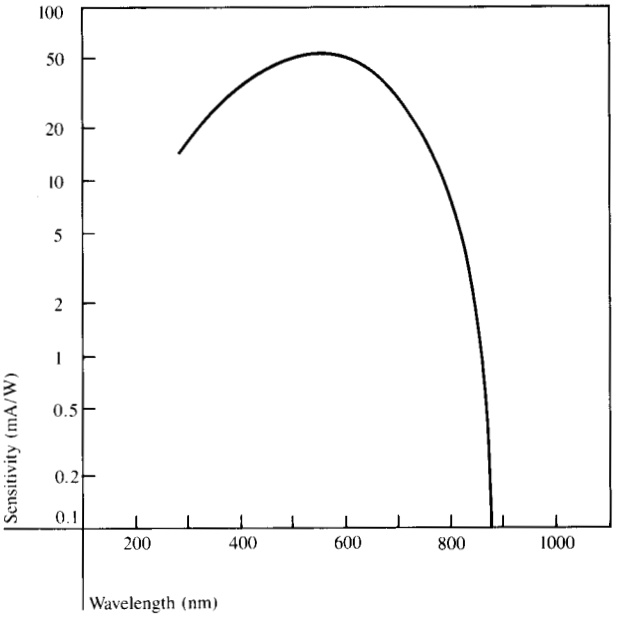

Figure 3 Typical image dissector response curve.

The final corrections for rotation, offset, and linear dimensional errors due to slight variations from board to board, and the fixturing of the tester, etc., are accomplished in the electronics of the camera control unit (CCU). Actually, the board is scanned concurrently by two image dissector cameras to increase tester throughput, and there is one CCU for both cameras. The CCU consists of an IBM Series/1 computer and custom-designed digital electronics which performs the real-time correction, as discussed in greater detail later.

All of the compensations and corrections to adjust the original data for use in driving the camera to the specified features are accomplished by the CCU. The original data are kept intact in the manufacturing data base. Figure 4 summarizes the entire distortion correction process.

• *Camera distortion corrections*

Of all the investigated electronic and optical distortions to the image of the board, the camera was found to be a major contributor; it was also the most interesting to compensate for. The image area or *handler* was divided into 25 partitions

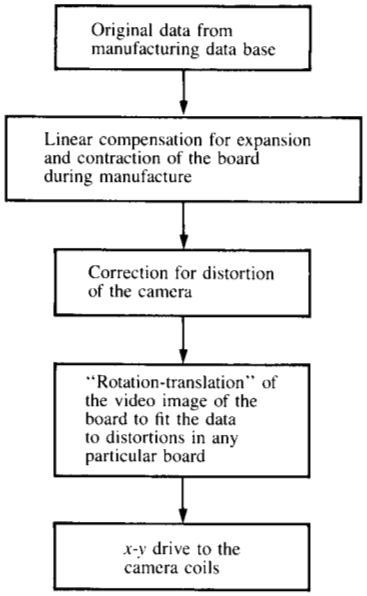

Figure 4 Transformation of design data into camera x-y drive-coil current flow.

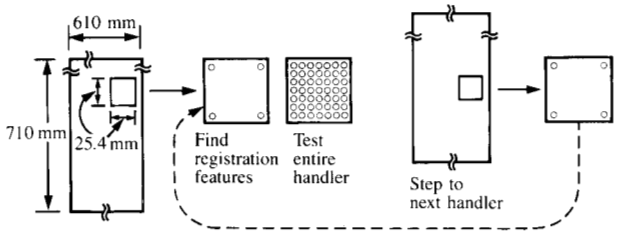

Figure 5 Power plane inspection illustrated. The plane is stepped under the camera using an x-y positioning table. Four hole positions selected from the design data are then used for registration adjustments. Compensation coefficients are calculated and then applied to all 25 sectors in a handler area. The handler is then scanned and tested using the power-plane models, and errors detected are recorded for later use in human verification. The plane is then stepped to the next handler position, and the process is repeated until the whole plane has been scanned.

because it was discovered experimentally that 25 was the smallest number of sections that will yield an acceptable linear approximation of the nonlinear distortion in the system.

Using a 0.635-mm precision grid pattern exposed on glass, called a calibration glass, linear corrections are derived as follows. The exact location of each intersection on the calibration glass is known with a certainty of 25.4×10^{-4} mm. For each 25.81 mm^2, the camera scans and locates 81 intersections. The location at which each intersection is found is subtracted from the true location of the intersection. These 81 differences are applied to a least-squares, best-fit equation, and a linear approximation of that partition is generated.

The same procedure is repeated for the remaining partitions for both x and y, and 25 sets of equations are produced and associated with their corresponding partitions of the handler. They are saved and applied to the compensated part-number data whenever the camera is scanning within a given partition. For every handler scanned, regardless of the part number or product type, these corrections are used. These compensations are only changed when the camera tube is moved or changed, or when the electronics drifts.

• *Board distortion corrections*

Another type of distortion which needs compensation is the difference between the idealized board feature coordinates and the actual board coordinates due to environmental effects. The expected coordinates are adjusted by means of rotation and/or translation. This correction is needed because of slight variations from board to board of the same part number and the fact that the image rotates as a function of light intensity. These distortions are, for the most part, linear. Three types of feature distortions are compensated here: 1) enlarged or reduced features, 2) wrong angles, and 3) off-sets.

The digital electronics of the rotator-translator in the CCU adjusts the video image for all three of these distortions. The machine finds the actual or corrected location X', Y' of several features in the handler. It then compares these locations to the locations specified in the raw data for the same features. The differences between the given locations from the raw data and the locations where the features were actually found are put into a least-squares, best-fit equation which produces six coefficients A, B, C, D, E, and F, where A is the X magnification, B is the X rotation, C is the X offset, D is the Y rotation, E is the Y magnification, and F is the Y offset.

These six variables, along with the original X and Y, are put into the hardware and mathematically operated upon in the following manner:

$$X' = AX \pm BY \pm C; \tag{1}$$

$$Y' = \pm DX + EY \pm F. \tag{2}$$

The rotation-translation calculation could have easily been done in the Series/1 computer, but the Series/1 is not fast enough to perform the board test in a reasonable amount of time. Instead, the CCU was outfitted with high-speed logic circuitry that does the addition, subtraction, and multiplication. One complete set of (X', Y') calculations [Eqs. (1) and (2)] can be executed and sent to the camera coils in 11 μs.

Fast transfer of data from the Series/1 located in the CCU to the high-speed logic circuitry is made possible by a special direct-memory-access attachment card in the Series/1. Once the 25 X' and Y' equations are set up for a given handler, the x-y position data are applied to the corresponding equation for the partition under test. When the x-y position data for a given handler are exhausted, the test goes to another handler. The entire rotation-translation process is then repeated and new coefficients are generated (Fig. 5).

Thus far, all the corrections discussed have been made for the location of features. It turns out that the light and video signals also require corrections. A voltage reference, mentioned earlier, must be established and the non-uniformity in gain across the face of the tube needs compensating. In each handler of the power plane, four features are selected to use for registration. These four features are also used to set the voltage reference levels for the handler.

Each registration feature is scanned across in 19 places, as illustrated in Fig. 6. About half of the 19 observations fall within the feature, while the other half fall outside the feature. A video voltage level is noted for each of the 19 points. The points outside the feature should fall on copper, and thus should present comparatively high video levels. The points within the feature should fall on dielectric, and thus should present relatively low video levels. The reference level V_{ref} is set with

$$V_{ref} = a(V_{hi} - V_{lo}) + V_{lo}, \quad (3)$$

where a is a programmable constant, usually between 0.3 and 0.5, V_{hi} is the average of the four highest readings, and V_{lo} is the average of the two lowest readings. This formula is used because it was found to set a level that minimizes false errors, yet finds defects 25 μm wide or greater.

Just as in the optical distortion of the handler area, the image-dissector tube does not exhibit uniform gain over its entire scannable area. The gain drops off as the distance from the center of the tube increases. Also, the light source does not deliver entirely uniform light. If these properties were not compensated for, the test sensitivity would not be uniform over the entire scanned area. Therefore, a procedure was developed to compensate for these distortions.

A uniform reflective surface is placed under the camera and is illuminated exactly as if it were the product under test. For each partition, 400 points are sampled and the video voltage of each point is normalized with respect to the other 399 points. The average video level for each of the 25 partitions is compared to the partition with the highest video level and is expressed as a percentage of the video level of the highest partition (normalized percentages). The reference level for each partition is then adjusted by multiplying all of the percentages by a typical reference value, as derived from the registration algorithm. The resulting compensation values for non-uniform gain of the image-dissector tube for each of the partitions are then used to maintain the video voltage sensitivity and the effectiveness of the total test constant.

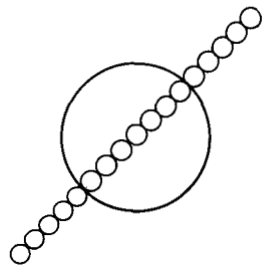

Figure 6 Power-plane hole scanned in 19 places for setting a video reference level.

Registration and testing

Testing of the product must be divided into two distinct categories because power distribution layers are tested differently from signal planes. Testing of power planes consists of checking the inside of via holes for extraneous copper, whereas testing of signal planes consists of checking pads and lines for shorts and voids. Both tests need to be registered each time the test area is indexed across the board surface.

- *Registration*

Registration involves the location of a number of specified features in the given handler (e.g., four holes for power planes). The differences between where these features are actually found and the given data are used to arrive at a new set of transform equations. Equations of the form $(AX \pm BY \pm C)$ and $(\pm DX + EY \pm F)$ are combined with the calibration transform equations (1) and (2) for each of the 25 partitions and are then used to test one handler of the product.

For power plane registration, one is first concerned with finding the centers of four selected holes in each handler. Geometrically, the center of a circle is the intersection of the perpendicular bisectors of any two chords of a circle, as shown in Fig. 7(a). Registration is done at 45°, with the chords mutually perpendicular to simplify the mathematics. The inside of the hole is scanned until four edges are found. These four edges define two mutually perpendicular chords. The center of each chord is found and the equation for the perpendicular bisection line is generated. The center of each circle is found by simultaneously solving the equations of both bisecting lines for X and Y; see Fig. 7(b). After the corrected center is found, it is used to do another registration, this time in smaller increments, resulting in a more accurate location for the center.

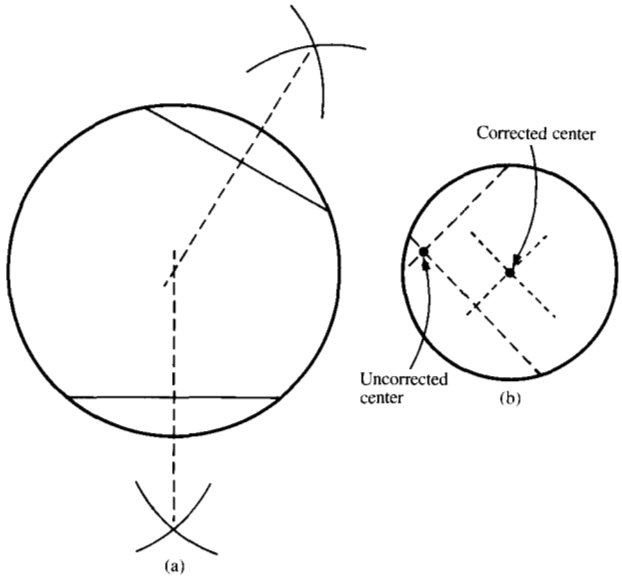

Figure 7 (a) Locating the center of a circle. (b) Locating the center of a circle with coarse (—) and fine (---) resolution.

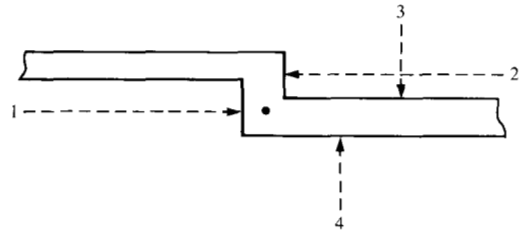

Figure 8 Registration of a printed-circuit line.

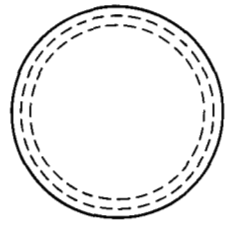

Figure 9 Power-plane hole model; dashed lines represent feature scans.

The final four centers found in a unit handler area are then compared to the original test coordinate data. The differences are used to find a least-squares solution for the coefficients A–F. The resulting coefficients are substituted in the registration equations, which are combined with each of the 25 calibration equations. In this manner, registration need be done on only four of the many features in a handler area, and testing of the holes in the handler can continue thereafter.

Registration of signal planes is done in a very similar manner. As shown in Fig. 8, four scans are done. Scans 1 and 2 locate two edges from which an x-center coordinate is found. Scans 3 and 4 locate the y center. Again, these data are compared to the test coordinate data and are used in a least-squares fit to find coefficients for the transform equations. As before, this method eliminates the need to register on every feature in a given handler area. Once registration is accomplished, the product is scanned using feature models.

- *Error detection*

A feature model is simply a set of camera scan commands that can be applied to a given feature (hole, line, pad) on a board. After registration determines an exact reference location of a feature, the tester data calls out the appropriate model for the feature and applies it.

For example, on a power core, the hole size of each hole is known from the original data used to make the glass master. The tester uses the same data for the model of the hole, which consists of two circular scans close to the inside edge of the hole drawn about the corrected hole center as determined by the registration procedure (Fig. 9). Since the scans are inside the hole where no copper should be present, the level detector is set to detect an error if the voltage from the camera received while scanning the inside of the hole exceeds the previously described reference level. Because the holes on a given power plane are virtually identical in size, the same model can be used for each hole. Basically, the hole model draws a circle of a given size about the center of the hole. For a 1-mm-diameter nominal clearance hole, two scans are made, one with a 97% diameter and the other with an 85% diameter about the center of the hole. For a typical board with some 30 000 clearance holes, it takes about five minutes to inspect one side.

For signal planes, models of lines, jogged lines at 45°, and pads are available to scan feature edges for protruding copper and about feature centers for voids (Fig. 10). A line is scanned along both edges, looking for protruding copper, and along its center, looking for voids. Using other models, each land and pad can be checked for shorts and opens (Fig. 11). Just as in the power-plane hole-registration operation, correction coefficients are calculated and these are then applied to the original coordinates of feature-location data to find the positions of the features on the scanned board. For a typical board, this takes about fifteen minutes per side.

Conclusions

The printed-circuit boards used in the IBM 3081 presented a real challenge to the test engineers. The expense of building

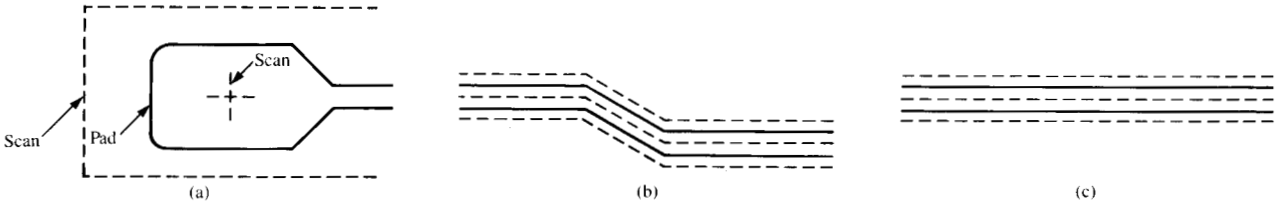

Figure 10 (a) Model for a signal pad. (b) Model for a printed-circuit jogged line. (c) Model for a printed-circuit straight line. Dashed lines represent feature scans.

this multi-layer PCB has dictated the testing of individual printed-circuit and power-distribution planes before lamination. Because the individual signal layers are made using a woven fiberglass substrate, environmental influences can cause these layers to expand and shrink. This leads to an uncertainty of position which makes contact testing difficult if not impossible. Manual inspection of these printed circuits is too expensive and is also very tedious. What was needed was a fast, effective automatic test system that would examine interplanes for shorts and opens optically. While we do not go into the cost justification of the system in this article, with the desired throughput the system described costs little more than half as much as the annual cost estimated for a purely manual (human) inspection system.

The system has been very effective on process defects for which it was designed. It locates all defects on power distribution layers with a greater than 92% accuracy. These interplanes are made by using a subtractive etching process, which results in reasonably well-behaved defects.

Testing printed-circuit layers made by an additive process has been a more complex task because of the types of defects encountered (e.g., dishdowns, neckdowns). For example, if there is only vertical thinning of lines and this thinning does not extend to the dielectric surface (as in dishdowns), the error is not silhouetted by the dielectric and no positive contrast is detected. In order to capture these defects, the system's sensitivity needs to be increased. When this is done, a large number of false calls are made, thereby requiring every defect called out by the system to be verified manually. Defects due to subtractive etching processes are found with a much lower false-call rate.

Since other systems investigated also depend on contrast to find defects, they would not detect dishdowns either. This type of defect requires ways to increase contrasts in the product and also, possibly, new ways to process incoming video signals.

Our method does have the advantage over other systems in that it can test not only printed-circuit and power interplanes

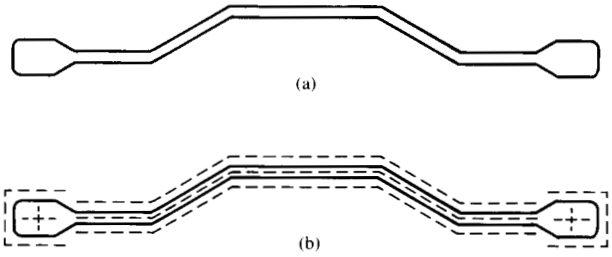

Figure 11 (a) Complete feature for models to scan. (b) Dashed line illustrates feature scan as used on TCM board signal planes.

but also the glass masters that were used to create the planes themselves. These glass masters can have mislocated features. Part-number data, as used in our system, are required to detect this type of problem. This results in finding defects before large numbers of PCBs with misplaced features are manufactured. Our system is also quite flexible. As configurations of features change with the evolution of the product (different hole sizes, pad styles, etc.), it is a simple matter to change existing models or create new ones.

In today's electronic environment, the trend is towards more and greater miniaturization. As this occurs, contact testing of printed circuits becomes increasingly difficult. New and unique methods of non-contact testing must continue to be developed. As features become smaller, testers may use systems which utilize electron-beam or non-visible optical wavelengths for the detection of defects. The test processors will continue to get "smarter." Use of digital image processors and better computers should yield even better results [7–10].

The test system designed is applicable to inspection of ceramic substrates, masks, and x-ray images. In fact, it is flexible enough to be used on any surface on which specified features with a given contrast from the background can be found.

References

1. Donald P. Seraphim, "A New Set of Printed-Circuit Technologies for the IBM 3081 Processor Unit," *IBM J. Res. Develop.* **26,** 37–44 (1982).
2. Roy Pope, "Computer with Eyes," *Indust. Res./Develop.*, 105–108 (1978).
3. Warren M. Sterling, "Automatic Non-reference Inspection of Printed Wiring Boards," *IEEE Computer Society Conference on Pattern Recognition and Image Processing*, Chicago, IL, Aug. 6–8, 1979, pp. 93–100.
4. Robert C. Restrick III, "An Automatic Optical Printed Circuit Inspection System," *Proc. SPIE* **116,** 76–81 (1977).
5. William A. Bentley, "The Inspectron: An Automatic Optical Printed Circuit Board (PCB) Inspector," *Proc. SPIE* **201,** 37–47 (1979).
6. Masato Nakashima, Katsumi Fujihara, and Takefumi Inagaki, "Automatic Mask Pattern Inspection for Printed Circuit Boards (PCBs)," *Fujitsu Sci. & Tech. J.* **17-2,** 105–117 (1981).
7. Jan Van Daele, Andre Oosterlinck, and Herman Van den Berghe, "Television Scanners," *Proc. SPIE* **130,** 75–82 (1977).
8. *Digital Image Processing*, Kenneth R. Castleman, Prentice-Hall, Inc., Englewood Cliffs, NJ, 1979.
9. Roger R. A. Morton, "Use of Software for Pattern Classification," *Proc. SPIE* **130,** 61–65 (1977).
10. Masato Nakashima, Katsumi Fujihara, and Takefumi Inagaki, "Automatic Mask Pattern Inspection for Printed Circuits Based on Pattern Width Measurement," *Proc. SPIE* **182,** 38–48 (1979).

Received September 8, 1981; revised August 26, 1982

Edwin C. Baldwin *IBM General Technology Division, P.O. Box 6, Endicott, New York 13760.* Mr. Baldwin is a development engineer at Endicott, where he joined IBM in 1962. His main interests are in electron-beam deflection control and phototrace machine development. Mr. Baldwin received his B.S. in electrical engineering in 1962 from the Rochester Institute of Technology, New York. He received an IBM Outstanding Innovation Award in 1976 for his work on electron-beam deflection control. In 1982, he received an IBM Outstanding Innovation Award for his work on a two-camera optical test system. Mr. Baldwin obtained his First-Level Invention Achievement Award in 1971.

Steven M. DeFoster *IBM General Technology Division, P.O. Box 6, Endicott, New York 13760.* Mr. DeFoster is an associate engineer in the in-process test area in Endicott. He joined the company in 1978. He has done work on contact test systems, and between 1979 and 1981, he worked on building and debugging the test system described in the paper. Currently he is working on developing new automatic optical inspection techniques. Mr. DeFoster holds an A.A.S. in electrical technology from Onondaga Community College, Syracuse, New York; a B.S. in biology from the State University of New York, College of Environmental Science and Forestry, Syracuse, New York; and will receive a B.S. in electrical engineering technology from the State University of New York, Binghamton, in 1983. Mr. DeFoster is a member of the Institute of Electrical and Electronics Engineers.

Mark A. West *IBM General Technology Division, P.O. Box 6, Endicott, New York 13760.* Mr. West is a senior associate engineer, currently working on development of new automatic optical inspection techniques. After joining IBM in 1980 in Endicott, he worked on thermal analysis techniques for detecting shorts in multi-layer printed circuits. Mr. West received his B.S. from the University of Michigan, Ann Arbor.

Richard A. Ziegler *IBM General Technology Division, P.O. Box 6, Endicott, New York 13760.* Mr. Ziegler is a development engineer manager responsible for ACP test engineering. He has worked on the development of process test equipment used in the TCM program. Since joining IBM in Endicott in 1961, he has held various managerial positions in test equipment for package development and manufacturing. He was an associate professor at Broome Community College, Binghamton, New York, from 1973 to 1976. Mr. Ziegler received his A.A.S. in electrical engineering from Broome Community College.