

Precise Numerical Control for the Thermal Conduction Module

Automated manufacturing processes have been developed and put into practice for the high-volume production of the thermal conduction module, the high-density circuit package used in the IBM 3081 processor models. The very precise work required on the ceramic surface required the solution of many problems. The small but significant residual distortions (warpage) which resulted from firing the multi-layer ceramic substrates made it difficult to locate tooling precisely for subsequent processes. A unique scheme for measuring the module and precalculating numerical control data has made it possible to achieve full automation. The nature of the problem, the attempts at a simple solution, and the algorithms finally used for numerical control data calculation are presented.

Introduction

The thermal conduction module (TCM) is a reworkable multi-layer ceramic (MLC) module which has been described previously [1]. Two types of TCMs are used in IBM 3081 processors, a 100-chip version (all logic) and a 118-chip version containing both logic and logic arrays.

The multi-layer ceramic substrate is produced by laminating as many as 32 layers of metallized ceramic sheet (formed from alumina mixed with binder material) and sintering the lamination at high temperatures [2]. Each ceramic sheet has a metallic pattern printed on it, and holes are punched into the sheet to permit metal interconnections (vias) between printed-circuit layers. During the firing, the whole substrate shrinks approximately 17%. For this reason, each layer is intentionally printed oversize so that the resultant product will meet the nominal dimensions within prescribed tolerances. However, the shrinkage is not completely uniform. Although a small amount of warpage and distortion is permitted by these tolerances, the deviation becomes quite significant when the subsequent numerically controlled manufacturing processes, such as engineering changes, are considered.

The purpose of an engineering change action is to correct design errors, enhance design performance, or modify the logic due to changing design specifications. This is usually

accomplished by redesigning a section of the previous circuitry. In the manufacturing line, an EC action manifests itself as chips being replaced by new ones, line deletions, and discrete wire additions. Following these actions, the module is tested at the new EC level [3] by probing on the EC pads, and ultimately by testing the entire TCM [4, 5].

Rework of the module is accomplished by disconnecting a chip termination from the internal wiring and reconfiguring the chip-to-chip interconnections with surface discrete wires bonded to specially designed metallic pads called engineering change (EC) pads. Each logic input/output (I/O) of a chip runs to such an EC pad, and all connections to that I/O from the rest of the substrate are also made through the same EC pad. Figure 1 illustrates such an interconnection. The signal runs from the chip I/O through a printed-circuit layer to an EC pad on the top surface of the module. On that same surface, a narrow printed-circuit line (which can be cut) makes the connection to an interplane via hole from which all further printed-circuit interconnection takes place.

A line-deletion operation on the top layer between the EC pad and the first via hole can be used to disconnect the printed-circuit wiring from the chip; discrete wires must then be used to reconnect the severed I/O to a new circuit (if that is what is desired). The discrete wires are placed in design-

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nated orthogonal wiring channels, as shown in Fig. 2. By this means, the chips, the line-delete points, and the EC pads are not overlaid by discrete wires, so that rework requiring chip changes, line deletions, and discrete wiring can be accomplished.

Although only a few EC pads are involved in any one engineering change, every EC pad on a module is a candidate for EC action. In the TCM family, each 90-mm-square TCM (identified by part number, serial number, and EC level) has between 10 900 and 11 600 EC pads.

Whereas wire bonding is used as a detailed example in the rest of this paper, the methods developed can also be applied for the precision required in the operations of line deletion, chip placement, and probing for test operations. Since a module part number goes through an engineering change action several times in its lifetime, it is desirable to take measurements just once, and to calculate the required tool positions from then on in, as needed.

Module rework repair system

To identify the precise location of each and every EC action point on the warped ceramic surface, a module rework repair system (MRRS) was developed to run in conjunction with the hierarchical manufacturing system installed at our site, and briefly described by Barry [5]. MRRS runs on the host System/370 virtually "paperless" [6].

The release interface tape (RIT) is the vehicle used to transmit module design and test data from the engineering laboratory to the manufacturing site. These RITs are released for newly designed modules and also for ECs. Newly arrived RITs are separated by the manufacturing system into several subsets of data for further processing. Figure 3 shows the data flow and distribution to the various manufacturing subsystems. *Substrate-build* data are routed to the multi-layer ceramics facility, and *module-test* data to the module-test facility. MRRS receives the *module assembly* and *EC rework* data and stores them in the *part number* file with their EC levels. The *serial history* file contains all the data required to track the rework history of every TCM produced. A separate "record" is maintained for each serial number of each generic part number [7].

The MRRS computer programs prepare the NC data for each job passing through the process. As shown in Fig. 3, the appropriate data are passed on to the IBM Series/1 controllers (which control the build and rework tools) to issue the positioning and other commands for carrying the tools through their sequences of operation. An interactive console at each controller presents the information needed by the tool operators to perform their tasks without intervening paper work.

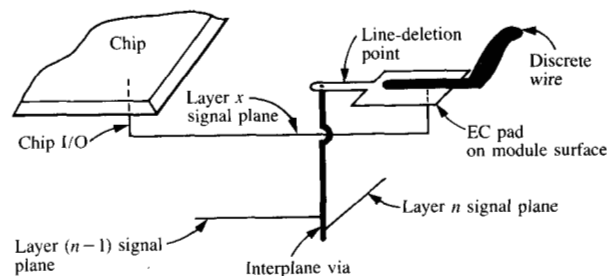


Figure 1 Method of module rework. Every chip I/O is led to its closest surface EC pad before being connected to the rest of the electrical net. The line-delete tool may now be used to sever the chip I/O from the rest of the net by interrupting the path between the EC pad and the via point. A new wire may also be bonded onto the EC pad and to reconnect the chip pin to the original or to any other net.

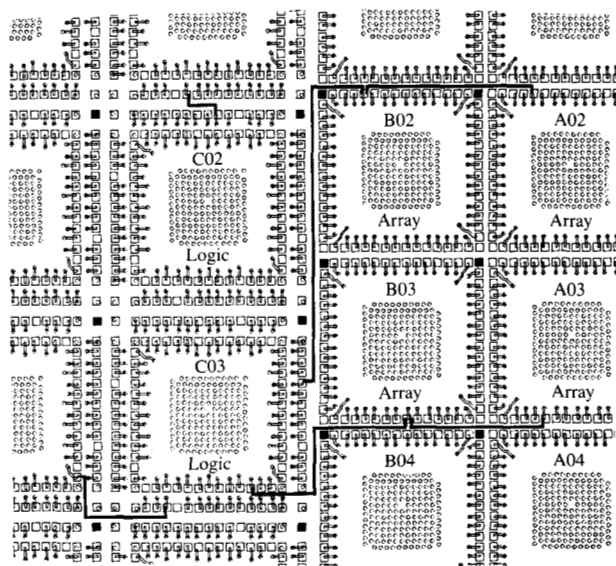


Figure 2 Discrete wires in wiring channels. Note that mapped pads are shown as darkened squares.

Discrete wire bonding

Repair and rework on the TCM is performed with the use of insulated wires which are placed and bonded on a printed-circuit EC pad [8]. The discrete automatic bonder (DAB) places and bonds up to two of these wires, if required, on a single EC pad without operator intervention. Wires are placed at fixed levels above the module surface so that crossing wires will not interfere. The NC data required to accomplish this are the coordinates of a series of points in three-dimensional space for each wire.

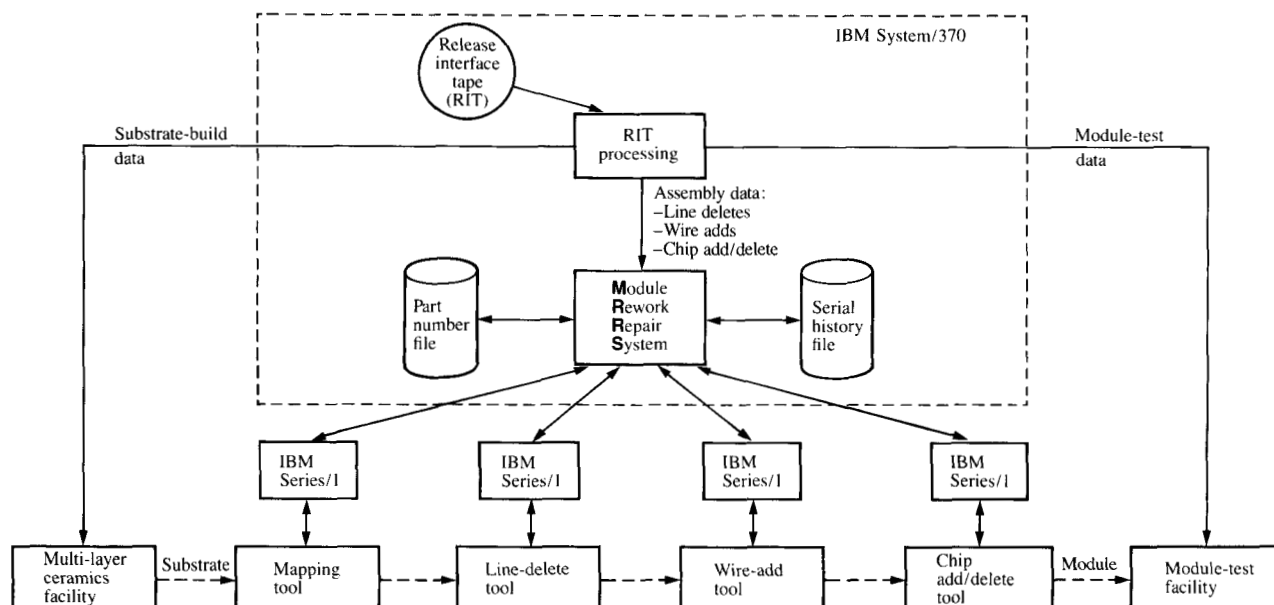


Figure 3 Simplified module and data-flow diagram.

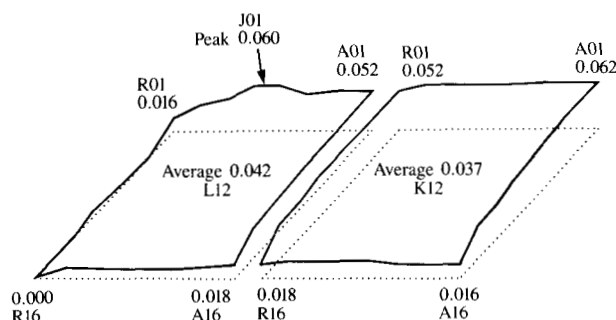


Figure 4 Topography of two chip sites. Variations between peaks and valleys can run as high as 0.07 mm. Measurements are relative in Fig. 5; locations are identified by EC pad names.

The action starts when the DAB bonds a wire on the first EC pad. Then, through the action of the wire passing through a feed tube while the substrate is moving, wire is laid in designated wiring channels between rows of EC pads. When a bend is required, as at the intersection of channels, there is a rotation. Finally the wire is bonded to the second EC pad and cut off. The insulation is then removed before any bonding is commenced by arc-stripping sections of wire at the bond location. To illustrate the precision required, a position error of one wire diameter places the wire at the edge of the EC pad.

The tooling and positioning tolerances are rather tight but not unusual in today's world of miniaturization. However, the slight amounts of distortion encountered due to warpage

from firing the MLC product do compound the problem. As a result, nominal locations of the top surface features, such as the EC pads, cannot be used. However, the specifications call for this product to be wired automatically, without operator intervention, and the length of the wire must be precalculated. For this reason the precise location of each EC pad in three-dimensional space is needed.

Preliminary measurement scheme

A preliminary measurement scheme involved measuring the center of each chip site on the top surface. The data could be stored until required for each job (chip placement, line deletion, wire addition, etc.) on the module. The wire bonding and line-delete positions were calculated by adding the nominal x and y offsets to the chip center.

Since the preliminary method could not compensate for distortions within the chip site, the bonds were frequently placed closer to the edge of the EC pads than was desired. However, the situation with the z -axis data was far more serious, since it was incorrectly assumed that all EC pads around a chip had the same z -axis height. Consequently, if the EC pad was higher than the NC data specified, the bonding tool would be driven too close to the surface and would exert too much force on the bond, thereby tending to crush the wire. On the other hand, if the EC pad was too low, the force would be insufficient, leading to a weak bond.

Topographical analysis

Prompted mainly by the need for more accurate z -axis data, a topographical study was made of the top surface of the

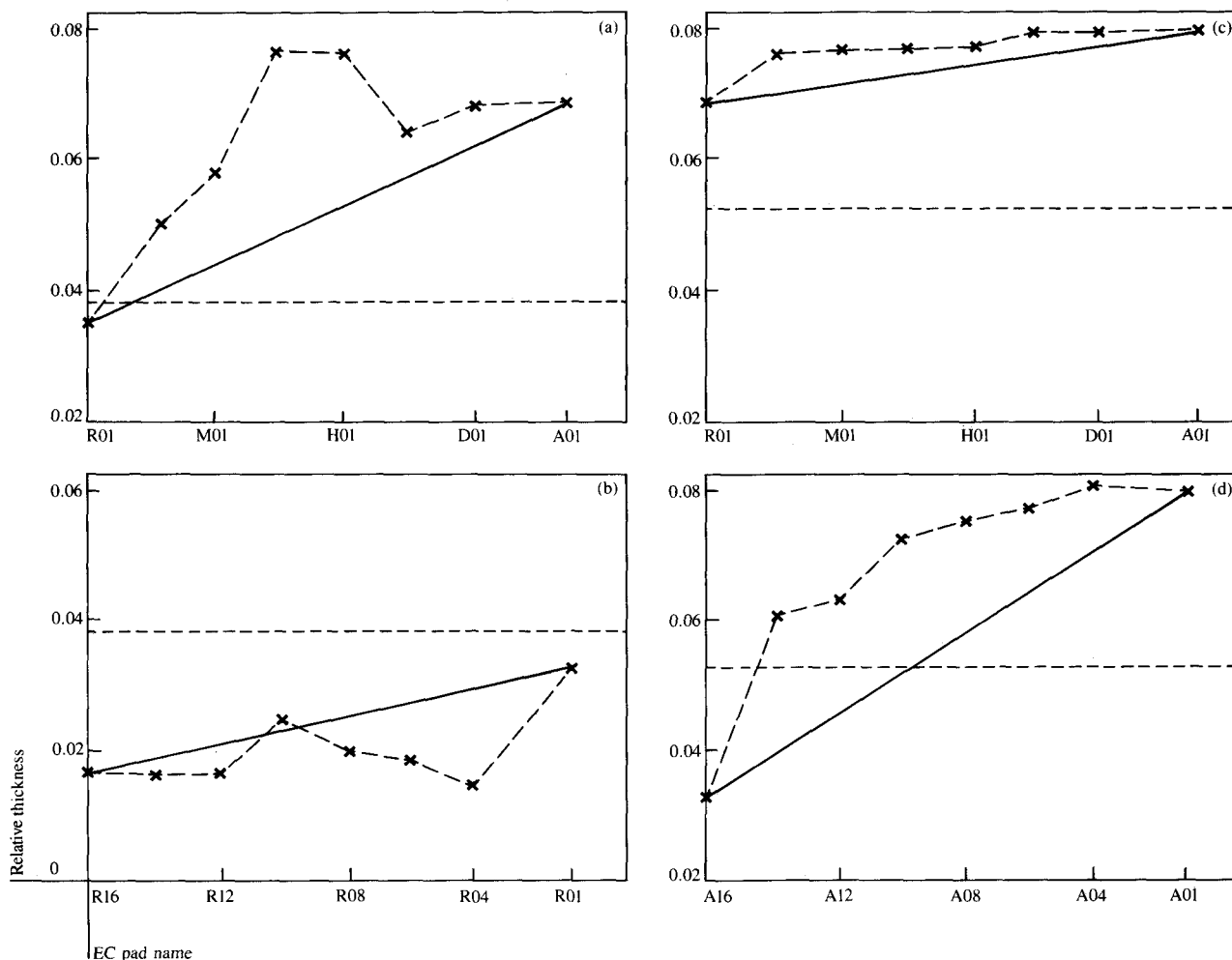


Figure 5 Examples of relative module thickness measurements taken at the chip sites of Fig. 4 and interpolation results (solid line) compared to the actual (- x -) and average (---) data: (a) L12 top row, (b) L12 left side, (c) K12 top row, and (d) K12 right side.

module. It was found that the module thickness varied gradually from point to point, tapering off considerably in going toward the edges, probably because of the absence of internal circuitry in that region. The results for two typical corner regions of a substrate are shown in Fig. 4. These regions are more varied than the central portions of a substrate which, in comparison, are quite flat, and thus could be approximated by one value per chip site.

There are occasional thick places, as shown by the peak on chip site L12 (Fig. 4). The preliminary method of calculating the NC data for the z axis frequently deviated from measured values.

Prompted by an analysis of the data accumulated on several substrates, the use of linear interpolation between measurements at corner EC pads was studied. Graphs are shown in Fig. 5 for two chip sites designated L12 and K12.

These two chip sites represented the worst situations encountered in the study. Because it was possible to maintain the error at acceptable values in all places except at the peak on chip site L12, a modified scheme of mapping and calculating NC data by linear interpolation was adopted.

Interpolation method

• Initial mapping

Key EC pads are selected for mapping. These are located at the intersections of major wiring channels. In order to calculate values by interpolation, each subsequent EC pad has to lie between two already mapped EC pads. The selected EC pads include the upper right-hand EC pad of each chip site on a 100-chip TCM and those EC pads located along the edges of the module. On the 118-chip TCM, since there are distinct logic and logic array regions for chip sites, additional mapped EC pads are included in the left-hand edge of each

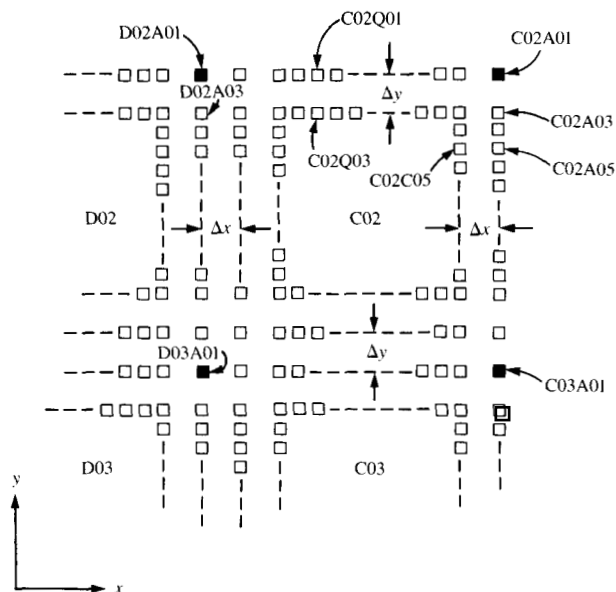


Figure 6 EC pads used in derivation of the interpolation factor (see text for details). Each EC pad on a module has nominal coordinates (x, y) and mapping or NC coordinates (X, Y, Z) . The mapping data are measured once and stored for future use (filled-in EC pads). The NC data for the rest of the EC pads are derived using the horizontal and vertical interpolation factors applied to the measured data.

region. With this approach, it is sufficient to map just 121 points to precisely locate the 10 900 EC pads; only 166 points are required to locate the 11 600 EC pads of the more populous TCM. The mapped EC pads have been darkened in Fig. 2.

The location of each mapped EC pad is measured in three-dimensional space to the nearest 0.002 mm. The mapping tool is a custom-built semi-automatic piece of equipment which is connected through an IBM Series/1 into the host computer and runs under MRRS, as shown in Fig. 3. It consists of a three-dimensional precision positioning table, a closed-circuit TV monitor, and some operator controls.

A substrate is mounted on the table and is identified to the host system by having its serial number entered on the operator console. The host responds by sending the nominal position points of each EC pad back to the Series/1. The Series/1 then uses these data to position the substrate, one EC pad at a time, for the operator to view through a reticle and confirm the x - y location. If the EC pad image is not correctly centered, the operator jogs the table with a series of commands until it is properly centered on the TV monitor; he then confirms this location by pressing a button which causes the Series/1 to read and record the precise x - y position. The machine then finds the z value of the EC pad by automati-

cally adjusting the height of the substrate until a reflection from the EC pad of a light beam aimed at it has reached maximum intensity. This process is repeated for each selected EC pad until all 121 or 166 pads are mapped. The mapped data are transmitted to the host computer and stored for the life of the module in the serial history data base. In addition to mapping data, the serial history file contains a record of all the activity the module has ever gone through, including chip additions and deletions, line deletions, and wire additions. Each time work is performed on the module for an engineering change update, or if it is returned from the field for repairs, etc., appropriate NC data are generated from the originally saved mapped points.

● Simplified interpolation algorithm

Figure 6 diagrams four chip sites, C02, C03, D02, D03, and their associated EC pads, which are identified by a three-character chip name, e.g., chip C02, and a three-character pad name, e.g., Q01. That EC pad then has a nominal three-dimensional-space location of $(x_{C02Q01}, y_{C02Q01}, z_{C02Q01})$, and an NC point-in-space location of $(X_{C02Q01}, Y_{C02Q01}, Z_{C02Q01})$. The latter is either measured (mapped and illustrated by the filled-in EC pads) or interpolated (calculated NC data illustrated by the hollow EC pads on the figure). The interpolated X , Y , and Z values for the center of an EC pad are determined by the following algorithm:

- Find two mapped EC pads between which the pad of interest lies.
- Calculate an interpolation ratio F .
- Apply the interpolation ratio to the three dimensions.

Again referring to Fig. 6, we note four cases of EC pads: two lie in a direct line between mapped EC pads and two are slightly displaced (Δy or Δx) from the direct line between mapped EC pads. For example, EC pad C02Q01 lies in a horizontal line between the two mapped pads D02A01 and C02A01. Yet another EC pad, C02Q03, although it lies in a row of EC pads, does not lie in a direct horizontal line between the mapped pads. This can be overcome by mapping two additional points, C02A03 and D02A03; otherwise, it must be compensated for in the algorithm. Similarly, EC pad C02A05 lies in a vertical line between the two mapped pads C02A01 and C03A01, while EC pad C02C05, although it is in another vertical column of EC pads, is displaced (Δx) from the direct line between the EC pads. Again, two additional mapping points would have simplified the NC data calculation. However, the implications for the manufacturing environment of increasing the number of mapped points per chip must be considered.

Four additional mapped points per chip would have required additional time to do the initial mapping. This would have resulted in the need to store much more mapped

information over the life of each module. The cost implications of the additional mapping time, the increased storage capacity requirements, and the added retrieval and data-transfer times which this would have entailed clearly must be balanced against other methods of obtaining the same results. An attempt was then made to find the simplest calculations that would still provide precise NC data to meet the manufacturing requirements. Nonlinear interpolation calculations and bidirectional interpolation calculations were investigated but were found to be unnecessary to obtain the required precision. The method chosen, which is next described by means of examples, was found to be the simplest and amply adequate.

Instead of a single interpolation factor, two are defined: a horizontal factor F_H and a vertical factor F_V . The horizontal interpolation factor is used in calculating the NC point for EC pad C02Q01 as follows:

$$F_H = \frac{x_{C02Q01} - x_{D02A01}}{x_{C02A01} - x_{D02A01}} \quad (1)$$

The NC coordinates in space can then be defined as

$$X_{C02Q01} = (1 - F_H)X_{D02A01} + F_H X_{C02A01}; \quad (2)$$

$$Y_{C02Q01} = (1 - F_H)Y_{D02A01} + F_H Y_{C02A01}; \quad (3)$$

$$Z_{C02Q01} = (1 - F_H)Z_{D02A01} + F_H Z_{C02A01}. \quad (4)$$

When a horizontal pad is not directly between the two mapped pads, e.g., C02Q03, it is found that the nominal offset Δy can be used on the Y coordinate, while the other coordinates do not need modification. Thus,

$$X_{C02Q03} = X_{C02Q01}; \quad (5)$$

$$Y_{C02Q03} = Y_{C02Q01} - \Delta y; \quad (6)$$

$$Z_{C02Q03} = Z_{C02Q01}. \quad (7)$$

Likewise, EC pads in a vertical column use the vertical interpolation factor. The calculations for EC pad C02A05 are as follows:

$$F_V = \frac{y_{C02A05} - y_{C03A01}}{y_{C02A01} - y_{C03A01}}; \quad (8)$$

$$X_{C02A05} = (1 - F_V)X_{C03A01} + F_V X_{C02A01}; \quad (9)$$

$$Y_{C02A05} = (1 - F_V)Y_{C03A01} + F_V Y_{C02A01}; \quad (10)$$

$$Z_{C02A05} = (1 - F_V)Z_{C03A01} + F_V Z_{C02A01}. \quad (11)$$

When a vertical pad is not directly between two mapped pads, e.g., C02C05, the nominal offset Δx is used on the X coordinate, and the other coordinates remain unchanged. Thus,

$$X_{C02A05} = X_{C02A05} - \Delta x; \quad (12)$$

$$Y_{C02C05} = Y_{C02A05}; \quad (13)$$

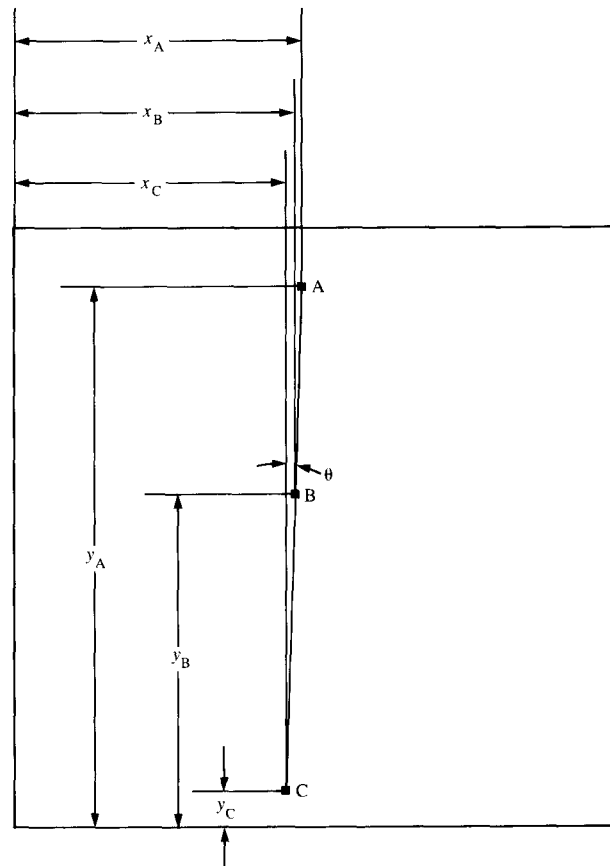


Figure 7 Measurements used for rotational corrections. The pads selected here are mapped pads which are later used to set up the module for wiring on the discrete automatic bonder.

$$Z_{C02C05} = Z_{C02A05}. \quad (14)$$

The EC pad center value calculated in this manner is also used in module test when probe coordinate data are required. For bonding purposes, each of the two bond sites is slightly offset from the EC pad center. Each line-delete point also has a unique offset from the EC pad center. The offset values are obtained from a look-up table and are applied to the pad of interest when needed.

• Additional corrections

The discrete automatic bonder needs one additional correction. The wiring channels must run parallel to the ways of the x - y table. There is usually a small but significant amount of skew of the top surface pattern with respect to the edges of the module. This can run in either direction. All data for a wiring job on a module are mathematically rotated about a central EC pad calculated from three mapped EC pads forming a straight line taken from the top, middle, and bottom of a module (Fig. 7). The angle θ , in radians, is then calculated for use in correcting the x - and y -axis NC values

as follows:

$$\theta = \frac{x_A - x_C}{y_A - y_C}; \quad (15)$$

$$x' = x - (y - y_B)\theta; \quad (16)$$

$$y' = y + (x - x_B)\theta. \quad (17)$$

Because the angles are small, this method assumes that $\cos \theta = 1$ and $\sin \theta = \theta$. When the module is set up on the bonder, the operator makes a slight rotational adjustment in order to force the reference line running through EC pads A, B, and C to run parallel to the ways of the machine.

Generation of chip site center data for chip placement is another part of NC data preparation. This center is calculated from the four mapped EC pads surrounding the chip site. In most cases, the actual corner EC pad on the site must be calculated from the adjacent mapped EC pads using the interpolation equations described earlier. Following this, the chip site center values are calculated by averaging the corresponding values of the four corner EC pads of the chip site. These values are also stored for the life of the module.

Conclusion

The mapping and NC data calculation techniques described here have supported the entire thermal conduction module line in IBM plants worldwide for almost five years. High-volume module production has been achieved because NC data, customized for each module passing through the production line, are available at the appropriate tool when the module arrives at the work station. This process has been one of the key factors leading to the successful production of IBM 3081 processor models.

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3. The latest engineering change (EC) is said to be at a higher EC level than a previous one. Each design is identified by an EC number on a part; the highest EC number on the part is referred to as its latest level.
4. R. L. Pierson and T. B. Williams, "The LT1280 for Through-the-Pins Testing of the Thermal Conduction Module," *IBM J. Res. Develop.* **27**, 35-40 (1983, this issue).
5. P. L. Barry, "Failure Diagnosis on the LT1280," *IBM J. Res. Develop.* **27**, 41-49 (1983, this issue).
6. By "paperless" we mean that manufacturing operators are given the information necessary to do their job via computer terminals, rather than by a printed document.
7. A generic part number is a particular part, like a model line of a manufactured car, e.g., compact. The serial number (of the car) then contains additional information, such as features, color, etc. In TCM manufacturing, the same is true, but instead of features and color, it is NC data and rework history (e.g., serial 1 of a generic part was produced perfectly with printed circuitry, while serial 2 had three discrete wire additions to make up for some faulty printed connections). This information becomes important once rework must be performed.
8. H. K. Hazel, "Discrete Automatic Bonder," *Manufacturing Engineering*, in press (1982).

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