

Product Quality Level Monitoring and Control for Logic Chips and Modules

In the manufacture of chips and modules, it is important to minimize defects in order to maximize quality levels and product reliability at each level of product assembly (chips, module, card, system). These objectives are best achieved by controlling defects through manufacturing process controls and testing at the lowest possible level of assembly. Defective product remaining after test and inspection must be repaired or discarded. The ability to detect and reduce or eliminate these defects is crucial to ensuring maximum product quality. The amount of such defective product is typically described quantitatively in terms of statistical sampling plans. The problem with such approaches is that the absolute defect level is imprecisely defined. This paper defines an absolute number for such product defects, which we will call "product quality level" (PQL). PQL categories found in logic chips and modules after completion of electrical testing are described and a methodology for the monitoring and control of the PQL in chips is presented. The impact of chip defects on module, card, and system performances is discussed with the aid of examples. By using the described comprehensive design, process control, testing, and user-feedback approach at each assembly level, final product can be manufactured with the lowest possible level of defects that must then be repaired at the machine level.

Introduction

Quantitative measures of the amount of defective product which must be repaired or discarded have traditionally been discussed in terms of their *quality levels*. These quality levels are defined in terms of statistical sampling plans, which imprecisely define the absolute defect levels. This paper defines an absolute measure for product defects, which is called the *product quality level* (PQL). The PQL of a component or an assembly is here defined as the percentage of a product that is defective and was not detected during the preliminary testing procedures but which must be repaired or discarded. Defective components may be detected initially by incoming acceptance tests and/or after mounting and testing at subsequent (higher) levels of assembly. In a sequentially assembled product such as a computer (chip, module, card, board, system), defects that contribute to failure must be controlled and removed at the lowest possible level of assembly in order to minimize costs.

Table 1 shows the levels of assembly associated with a typical product and the testing associated with each level. Ideally, testing at each assembly level is designed to ensure pre-specified performance at succeeding levels.

Definition of product quality level (PQL) and defect categories

To illustrate the concepts of PQL, let us consider the testing of LSI integrated circuits. The testing process separates product into two categories: *accepted* and *rejected*. Because the testing may not be 100% effective, some defective product may be inadvertently accepted, leading to more expensive repair steps at a later assembly level. The amount of defective product determines the product quality level (PQL). In addition, we define four categories of defects which make up the PQL: those that are 1) detectable with "dc testing" (*dc-detectable defects*), 2) undetectable with dc testing (*dc-undetectable defects*), 3) detectable with "ac testing" (*ac-detectable defects*), or 4) undetectable with ac testing (*ac-undetectable defects*). In addition, these categories exist for each assembly level, i.e., chip, module, card, etc. These categories and the factors which affect the PQL are treated in detail in the subsequent sections of this paper. The definition of dc and ac testing as used in this paper is given in the next section. With proper test sequences and process controls, the chip PQL, abbreviated as PQL_{chip} , can be quite small.

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• DC testing

Testing at a repetition rate which is low compared to the frequencies encountered in normal system use is defined as *dc testing*; it includes both parametric and functional pattern testing. Thus, the *dc-detectable PQL* consists of tested product which has dc defects that are detectable but for some reason (e.g., tester miscalibration) have not been detected.

During dc functional testing, test patterns are provided which test the logic for *stuck-at-0* and *stuck-at-1* faults; in this paper, we define this as *stuck-fault* testing. Thus, a *dc-undetectable PQL* results if the logic contains untested faults when the test patterns provided have less than 100% test coverage.

• AC testing

The testing of product for circuit propagation delays is referred to as *ac testing*. Thus, the *ac-detectable PQL* consists of tested product which has ac defects that are detectable but again for some reason have not been previously detected.

In contrast, product that is defective during ac testing, but which was not detected in the final test by any of the previously mentioned ac or dc parametric and functional tests, is defined as *ac-undetectable PQL*. This defect category exists, for example, if the product contains ac delay failures in paths that the available test patterns did not test.

Control objectives of PQL

The basic objective of controlling the product quality level is to manufacture products with few or none of the defects that cause failures at higher assembly levels, since these are more expensive to repair at a later assembly level. The calculation of PQL is determined through measurements at final testing; however, in-line processes and process controls determine the inherent defect levels entering final testing. Some types of defects will not cause failures at higher levels of assembly, while others will. With this in mind, some general objectives for the control of the PQL have been developed:

1. Minimize the number of PQL defects produced at each assembly level.
2. Design tests for each level specifically to detect prior-level defect escapes efficiently in order to catch them at the lowest possible subsequent assembly level.
3. Reduce sensitivity to defects, such as delays, where high detection efficiency is not possible through redesign.

These objectives are achieved by using design and application ground rules to ensure PQL values which approach zero. This can be accomplished by designing products so that potential ac delay faults are tester-detectable, by instituting design rules for testability to facilitate high dc logic stuck-fault test coverage, and by using redundant circuit features,

Table 1 LSI product levels of assembly and testing. The tests are described in the text.

Assembly level	Testing procedure used
LSI chip	dc parametric and stuck-fault ac delay and test chips on wafer
Multi-chip module	dc stuck-fault
Module on card	dc functional and/or stuck-fault
Card on board	ac/dc subsystem
System	ac system

such as double contacts on critical integrated circuit components (this results in a trade-off of redundancy vs testability). In addition, PQL-related defects can be minimized by using in-line process controls to reduce in-line defect densities, by monitoring detectable and undetectable PQL values continuously, and by applying corrective actions, in the form of product redesign or process, equipment, or test modifications, to reduce PQL values as defect causes are identified.

Monitoring and controlling the chip PQL

• Determination of dc-detectable PQL

At semiconductor manufacturing locations, numerous controls and monitors are placed on testing and product handling to eliminate defective product escapes from the chip and module levels. These include tester qualification, running of tester diagnostics, periodic retesting of random samples of accepted product to verify the PQL, and, where available, reference modules run on similar testers.

The performance of the PQL is monitored by the quality assurance organization through analysis of product rejected at higher levels of assembly. This product is returned to previous levels to isolate and identify the causes of the defects. Product returned is then retested and either found to contain no defects or it is failed. Failing product is physically analyzed to determine the causes of failure; this provides a basis for further corrective action. Product in which no defects have been found may be further analyzed by forwarding it to the next assembly level for card or system testing to verify diagnostics and to analyze the need for improved chip or module testing to cover the system application.

• Estimation of dc-undetectable PQL

The number of untested stuck-faults can be minimized through the use of level-sensitive scan design (LSSD), which was developed by Eichelberger [1]. This approach has been implemented in a test-generation system developed by Bortoff and others [2]. The power of LSSD lies in its potential application at all levels of assembly.

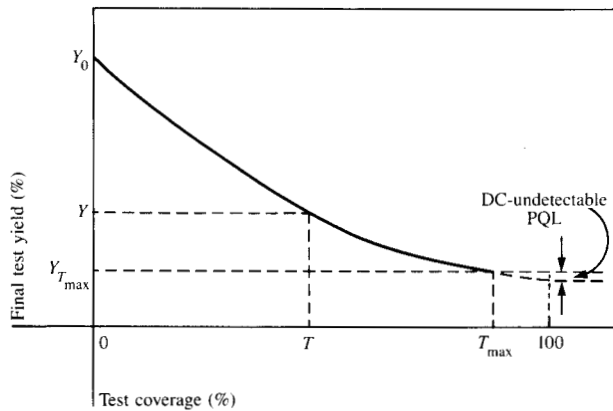


Figure 1 Final test yield Y as a function of test coverage T . The shape of the curve is that of a generalized Poisson equation, as discussed in the text. The yield slope is a measure of the percentage of yield loss per percentage of test coverage. The PQL slope is the percentage PQL per percentage test coverage. See the text for calculation of the actual part or product PQL.

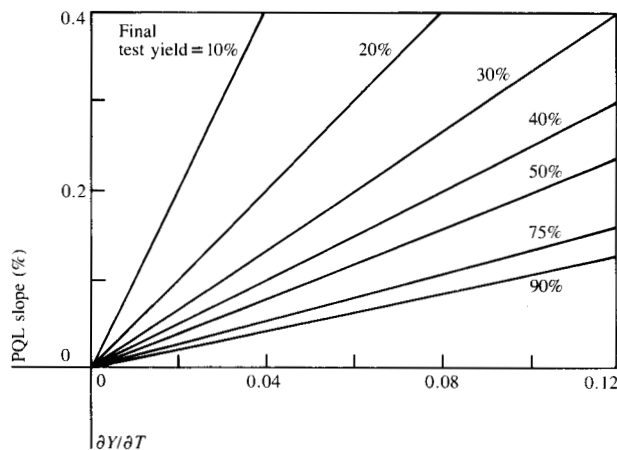


Figure 2 Generalized curve showing the influence of final test yield on the PQL slope.

A model for dc-undetectable PQL is essentially equivalent to a yield model at high test coverage. A Poisson model was first used to describe the dependency of the yield on the circuit area, using a generalized Poisson equation:

$$Y(T) = Y_0 e^{-\lambda T}, \quad (1)$$

where $Y(T)$ is the yield at test coverage T , Y_0 is the yield at zero test coverage, and λ is the defect density. The model was then refined to a mixed Poisson form, as described by Stapper [3].

A mixed Poisson model was used by Griffin [4] to estimate dc-undetectable PQL for medium-scale-integration chips.

The approach to using the model is as follows. At low test coverage, large area defects and clustered defects cause chip failures. In this region, the defect density λ has a clustered defect value, as described by Griffin. At higher test coverage, λ has a value represented by random or unclustered defects. This λ and test yield are the factors which influence dc-undetectable PQL.

Figure 1 shows a generalized plot of the final-test yield as a function of the stuck-fault test coverage for logic chips. The dc-undetectable PQL is estimated by varying the test coverage at final test and plotting the yield vs test-coverage curve. The slope of this curve (see Fig. 1) is determined by

$$\partial Y / \partial T = \frac{Y_T - Y_{T_{\max}}}{T_{\max} - T}. \quad (2)$$

The yield slope is the percent yield loss per percent test coverage. The percent PQL per percent test coverage (PQL slope) is then calculated:

$$PQL \text{ slope} = \frac{\partial Y / \partial T}{Y_{T_{\max}}}. \quad (3)$$

A plot of Eq. (3) as a function of the final test yield is shown in Fig. 2. For example, if the yield slope were 0.05% and the final test yield were 50%, the PQL would be 0.10% per percent test coverage. This PQL, measured just below the maximum test coverage, can be used to estimate the dc-undetectable PQL by extrapolating to 100% test coverage. The PQL of any particular part or product is then a function of the $T_{\max}$ for that part. That is,

$$PQL = (100 - T_{\max})(PQL \text{ slope}). \quad (4)$$

Thus, at 100% test coverage, the dc-undetectable PQL equals zero.

• Monitoring the ac PQL

AC delay failures are characterized as being caused by either nonrandom or random defects. Nonrandom defects, such as high capacitance, affect all circuits on a chip similarly. Random defects are considered to cause individual logic circuit delays.

Good ac circuit performance may be ensured 1) by ac delay testing (where propagation delays of logic chains are measured), 2) by in-process measurements of device parameters, and 3) by recirculating loop frequency (RLF) measurements [5] on test-site chips located on each product wafer and used for product and process monitoring. The technique applied depends on the product requirements of a particular technology. AC delay testing is used to minimize the ac PQL of logic circuits. In direct analogy to the dc-undetectable PQL, the ac PQL depends on the slope of the ac yield vs the ac test-coverage curve, and on the maximum ac test cover-

age. In-process measurements of component parameters, such as capacitance, are also performed to monitor and control ac performance.

An additional means of ensuring good ac performance involves RLF measurements [5]. A loop is wired so that it will oscillate at a frequency f determined by the number of stages and the propagation delay of each stage:

$$f = \frac{1}{2nt_p}, \quad (5)$$

where n is the number of stages and t_p is the propagation delay (propagation time) per stage. This frequency can be readily measured on automatic equipment during wafer testing. Nonrandom ac defects are monitored through RLF and other performance tests, and accept/reject criteria on a wafer basis are applied to the results. Product is rejected because of too little circuit delay (too high an RLF) or too great a circuit delay (too low an RLF). The actual tolerances used depend on the particular technology and application requirements.

• Monitoring random ac defects

A random ac defect occurring in a logic path can be considered to affect one logic circuit. The size of such a defect is characterized electrically by the shift in delay caused by the defect. The frequency with which these defects occur is characterized by a defect density term θ :

$$\theta = \frac{\text{number of defects}}{\text{number of wafers} \times \text{logic circuits per wafer}}. \quad (6)$$

For example, for random ac defects affecting 1 in 10 000 logic circuits, $\theta = 10^{-4}$.

In order to detect random ac defects, a comparison technique is used on the test-site data, and both the ac defect density and the distribution of ac defect sizes are determined over a large number of wafers. These data can be used to project ac PQL on product chips. The data differences among chip sites are normally within the chip circuit-delay tracking tolerance, i.e., the expected limiting values of the delay time across a chip. If these differences exceed the tracking tolerance, a random ac defect is assumed. The size of each ac defect (i.e., the delay time t caused by it) and its probability of occurrence can be calculated.

For example, Fig. 3 shows a distribution of random ac defects obtained through analysis of RLF data. Such information can be obtained from various other tests as well. The probability density function of an ac defect being of a given time interval can be expressed by the relationship

$$f(x_d) = be^{-bt}, \quad (7)$$

where t is the defect size (delay time) in ns and b is a

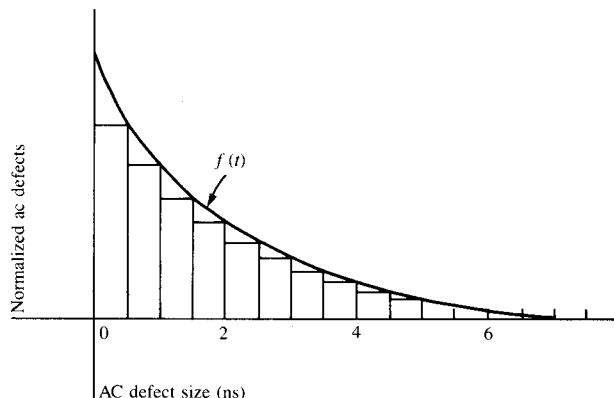


Figure 3 The data gathered from the RLF loops are compared against the expected ac defect-size model; $f(t) = e^{-0.5t}$.

distribution shape factor. Thus, the probability of a defect being of a given size m can be obtained from

$$m = \theta \int_A^B be^{-btdt}, \quad (8)$$

where b ranges between 0.5 and 1.0 for 700-circuit bipolar logic chips.

• Calculation of the ac PQL

The ac PQL is projected for a technology by using an algorithm based on the random ac defect probability, the system sensitivity (the fraction of ac defects that will cause a system failure), and the ac-delay test coverage. System sensitivity S_s can be determined through simulations accomplished by superimposing random ac defect size distributions on the nonrandom ac distribution for representative machine logic path lengths. Thus, system sensitivity to ac defects is expressed as the ratio of the number of defects causing system failure to the total number of defects. For a given defect density, S_s varies with the distribution of ac defect sizes; typical systems are less sensitive to small defects.

The algorithm developed for calculating the ac PQL is given as

$$\text{ac PQL} = [1 - (1 - \theta S_s)^{N_c}](1 - T_c), \quad (9)$$

where θ is now the ac defect density per circuit, N_c is the total number of circuits present, and T_c is the delay-path test coverage for ac delay tests performed.

System sensitivity expresses the probability that a given defect will produce a system fault. By including system sensitivity in the equation, an adjustment can be made for defect categories such as marginal delays at the chip or module level, which have little impact on system perform-

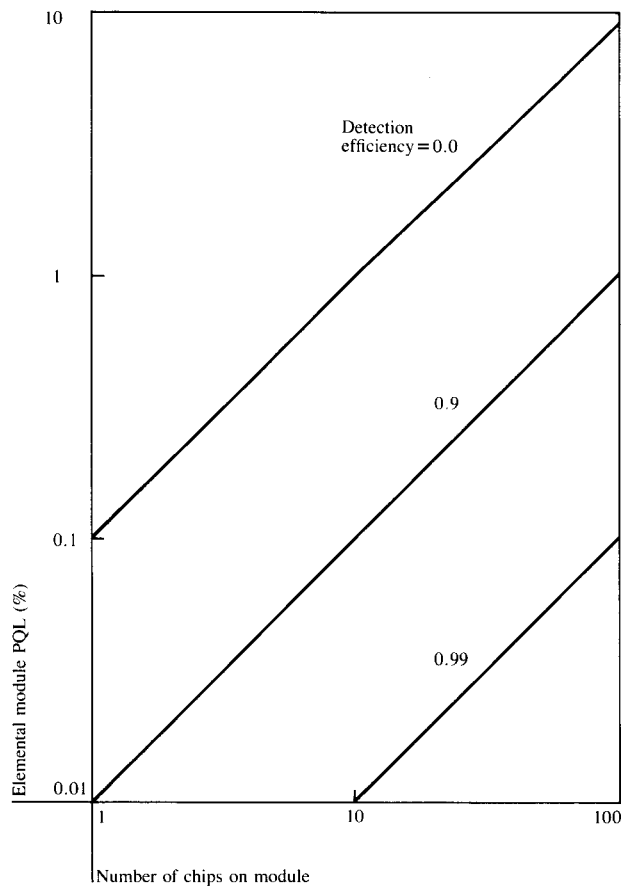


Figure 4 Generalized plots of the module PQL for one term ($1 - A$) of the PQL summation as a function of the number of chips on a module and the detection efficiency.

ance. For example, if $\theta = 10^{-4}$, $S_s = 0.01$ (1%), $N_c = 600$, and $T_c = 0.80$ (80%), one would obtain an ac PQL of 0.00012 (0.012%). Please note that the decimal form of all percentages must be used in these equations.

Algorithms for calculating the PQL

At the module level, the PQL is defined by an algorithm which assumes separate contributions from individual PQLs for the chips and substrates used to build the module. A general algorithm for calculating the module PQL is of the form

$$PQL = 1 - (A \times B \times C \times D \times \dots), \quad (10)$$

where $A, B, C, \dots$ represent probabilities that the module does *not* contain a defect of a particular defect category. In Eq. (10), these probabilities are usually near unity; thus, the PQL is usually small. A simplified form of the algorithm, from a computational standpoint, is

$$PQL = (1 - A) + (1 - B) + (1 - C) + (1 - D) + \dots \quad (11)$$

This equation gives results within 1% of the general algorithm when the total PQL is less than 5%.

The contribution to the module PQL, PQL_m , of various chip defect categories is a function of the defect density, the chip defect detection efficiency E_c of module test, and the number of chips in the module assembly n_c . The PQL of a module is expressed as

$$PQL_m = PQL_{D_m} + \sum_1^{k_c} 1 - [1 - PQL_c(1 - E_c)]^{n_c} \quad (12)$$

Here, PQL_{D_m} is the module-detectable PQL caused by module mistest or tester calibration errors, PQL_c is the PQL of a particular chip PQL category such as dc-detectable PQL, E_c is the detection efficiency of the chip, which is the ability of the module test to detect the specific chip PQL category, and k_c is the number of different chip defect categories.

In (12), the detection efficiency depends on the PQL defect category. Figure 4 shows a plot of the module PQL for one term (the $1 - A$) in the PQL summation as a function of chip population and chip detection efficiency E_c . For $E_c = 1.00$ (100%), the chip PQL contributor is completely detected; thus, no contribution is made to the module PQL.

At the card level, the same general algorithms, (10) and (11), apply. The module contribution to the card PQL is given by an algorithm of form similar to Eq. (12):

$$PQL_C = PQL_{D_C} + \sum_1^{k_m} 1 - [1 - PQL_m(1 - E_m)S_s]^{n_m} \quad (13)$$

Here, PQL_{D_C} is the card-detectable PQL, e.g., due to tester variations, etc.; PQL_m is the PQL of a particular module PQL category, such as dc-detectable PQL, E_m is the detection efficiency or the ability of the card test to detect the specific module PQL category, n_m is the number of modules in the card assembly, S_s is the system sensitivity to a particular defect, and k_m is the number of module defect categories.

Examples of PQL calculations

The multi-chip modules (MCMs) used in the IBM 4300 have been described by Clark and Hill [6]. The PQL calculations for an MCM with nine logic chips ($n_c = 9$) using the values from Table 2 are illustrated. According to Eq. (12), the module PQL is made up of the parts of the chip PQL not detected by module test plus a module mistest factor (here, 0.00050). Thus,

$$\text{Chip dc-undetectable PQL} = 1 - [1 - 0.0005 (1 - 0.99)]^9 \\ = 0.00005 (0.005\%);$$

$$\text{Module dc-undetectable PQL} = 1 - [1 - 0.0005 \\ \times (1 - 0.30)]^9 = 0.00315 (0.315\%);$$

$$\text{Module ac-undetectable PQL} = 1 - [1 - 0.00012 \\ \times (1 - 0.10)]^9 = 0.00097 (0.097\%);$$

$$\text{Total module PQL, } PQL_m = 0.00005 + 0.00315 + 0.00097 \\ + 0.00050 = 0.00467 (0.467\%).$$

This module PQL represents the percentage of modules which are projected to contain post-testing defects. Since some of these defects will reach the system level, an estimate of the system effects can be made if a system sensitivity factor is applied, as previously discussed. The assembly level at which system sensitivity is applied is somewhat arbitrary, but once applied, it must be used consistently. In the examples in this paper, system sensitivity is applied at the chip level for ac components and at the card level for dc components.

The following calculation of the PQL for a card with four modules ($n_m = 4$) uses the values given in Table 3. Again, from Eq. (13), the card PQL is made up of the parts of the module PQL not detected by card testing plus the card mistest factor (here, 0.00050). Thus,

$$\text{Module dc-undetectable PQL} = 1 - [1 - 0.0005 \\ \times (1 - 0.99) (0.5)]^4 = 0.00001 (0.001\%);$$

$$\text{Card dc-undetectable PQL} = 1 - [1 - 0.00315 (1 - 0.60) \\ \times (0.10)]^4 = 0.00050 (0.050\%);$$

$$\text{Card ac-undetectable PQL} = 1 - [1 - 0.00097 (1 - 0.20) \\ \times (1.0)]^4 = 0.00310 (0.310\%);$$

$$\text{Total card PQL, } PQL_c = 0.00001 + 0.00050 + 0.00310 \\ + 0.00050 = 0.00411 (0.411\%).$$

To illustrate the improvements in PQL that have taken place as a result of a combination of high test coverage and reduced system sensitivity, Fig. 5 shows the projected PQL of a hypothetical subsystem consisting of four cards containing 144 chips ($n_c = 144$) and using the example module and card given earlier. What we see is that the testing is able to catch roughly ten out of every eleven defects before they reach the machine assembly level. At the machine assembly level, final system testing removes any residual defects.

Summary

The product quality level (PQL) represents defects in a pre-shipped product which have escaped earlier testing at lower assembly levels and which must thus be repaired at the machine level. At a particular level of assembly, the PQL can be divided into detectable and undetectable categories, and each of these can be further segregated into contributions from dc or ac components. The general strategy for minimiz-

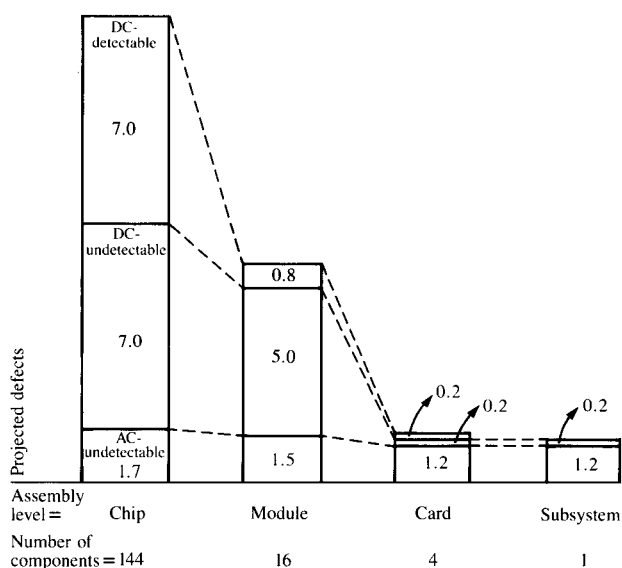


Figure 5 Example of the reduction in the defect level of a 144-chip subsystem due to testing and adjustments to the system sensitivity. Note that the testing is able to catch roughly ten out of every eleven defects before the machine assembly level.

Table 2 Illustrative module PQL data. Note that the numbers used here are not actual production data; they are used merely to illustrate the computations.

	PQL values (%)	Module detection efficiency for this PQL component (%)
Chip dc-detectable	0.050	99
Chip dc-undetectable	0.050	30
Chip ac-undetectable	0.012	10
Module-detectable	0.050	—

Table 3 Illustrative card PQL data. Note that the numbers used here are not actual production data; they are used merely to illustrate the computations.

	PQL values (%)	Card detection efficiency (%)	System sensitivity (%)
Module dc-detectable	0.050	99	50
Module dc-undetectable	0.315	60	10
Module ac-undetectable	0.097	20	100
Card-detectable	0.050	—	100

ing the PQL is 1) to minimize component defect levels, 2) to increase the test coverage, particularly at subsequent assembly levels to catch previously undetected but detectable defects, and 3) to reduce the sensitivity of the system to

defects which cannot be detected readily. Monitoring of the PQL is performed by in-process measurements of device parameters and with the aid of individual chip test sites located on product wafers. The techniques utilized include plotting the yield vs test coverage to measure the dc-undetectable PQL and recirculating loop frequency measurements on the test sites to determine the ac PQL. Algorithms for calculating the PQL at the card and system levels have been developed, and examples are given of the calculation of card and module PQLs. By using this comprehensive approach, product at each level of assembly can be fabricated with a very low level of defects which might lead to failure at a higher level. Final system testing removes any residual defects.

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