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Semiconductor Final Test Logistics and Product Dispositioning Systems

As product lines at the IBM East Fishkill plant have expanded in the last few years, and as the number of technologies and semiconductor wafer and module volumes have increased, more sophisticated software systems were introduced which not only drove test times downward, but also reduced the development time previously required to accommodate testing new technologies. This paper discusses two such systems developed for the bipolar semiconductor line. They are a final test logistics system which provides for computerized tracking of each device in the production line through both testing and diagnostic analysis, and an automatic product dispositioning system which immediately identifies shippable product batches after flow through the test sector or schedules the batches for additional diagnostic analysis.

Test strategy

The East Fishkill test facility encompasses stuck-fault (*i.e.*, defects which lock a circuit at an electrical one or zero, such as with opens or shorts) and environmental testing for all bipolar logic wafer and packaging components shipped from the IBM East Fishkill site. In addition to these, disturb tests (which check the ability of the memory cells to retain their programmed states under a variety of environmental conditions, such as pattern sequencing, pattern profile, noise, power supply or signal I/O variations, etc.) and performance tests are also applied to all array products. The bipolar product line is used in the IBM System/38, the IBM 4300, and the IBM 3081 processors. The semiconductor components, ranging in density from several hundred to several thousand circuits, are tested on one of several sophisticated tester systems. The computer configuration used for virtually all the testers is an IBM Series/1 or an IBM 3791 minicomputer harnessed to a manufacturing-developed controller or microprocessor (MP). The MP activates the hardware for handling and probing the devices, wafers, and modules. Depending on the tester requirements, the mini-computers are linked to different types of data processing and peripheral equipment, which in turn feed into a host IBM System/370 computer (see Fig. 1) dedicated to testing and test analysis activity. The tester configuration fits into, and is part of, the distributed manufacturing control system architecture described by Kerner and Strong [1] and Bean and Binninger [2].

Testing of logic wafers is accomplished through a four-step operation. The first is a screen test for gross defects in which power supply voltages are set and currents are measured. The second series of tests, parametric, evaluate the die I/O for faulty driver/receiver circuits. After this, a pseudo-functional test is performed, within both nominal and worst-case electrical environments, to detect logical *stuck-at-x* faults on the die or *chip* as we refer to it in this paper, indicating a circuit input or output stuck at a logical 1 or 0 level. AC assurance testing is accomplished for logic wafers by testing the recirculating loop frequency (rlf) on test site chips, which are strategically placed non-product chips on a wafer, containing technology-dependent devices characteristic of the transistors and latches throughout the wafer. These test site measurements, which are taken and compared against predefined product specifications, become an integral part of the automatic job dispositioning algorithm described later. Logic wafer test times, which are highly dependent on wafer size and product circuit densities, range from 8½ to 26 minutes per wafer.

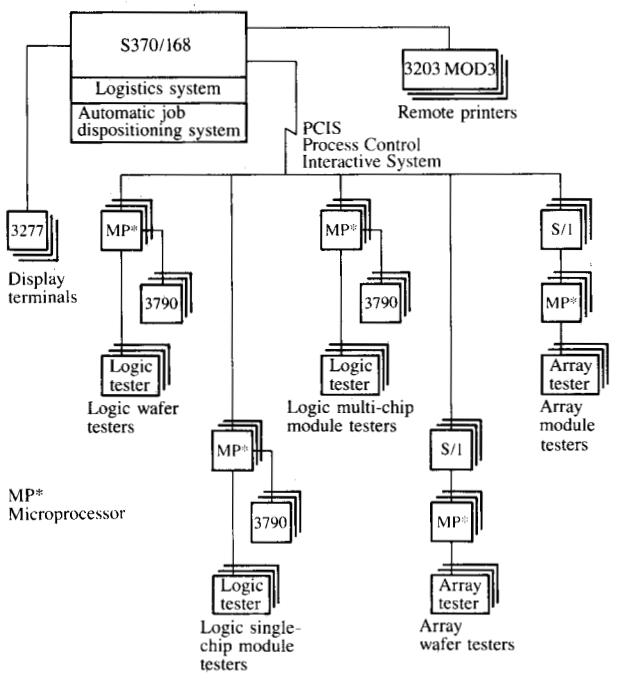


Figure 1 Final test hardware configuration. The System/370 host computer is interconnected to a network of Series/1 computers and microprocessors that, in turn, drive the different test systems. Remote printers and display terminals facilitate communication with test personnel.

Array wafer testing includes the basic aspects of logic wafer dc testing, but it goes beyond, to achieve true functional testing at machine speeds and to guarantee complete functionality, performance, and stability across both system-level temperature and voltage extremes. Test times reflect this additional testing, extending upward to 70 minutes per wafer.

The multi-chip module (MCM) product that is tested contains a combination of logic and array chips. MCM testing is a two-step operation. The first test, a terminator opens/shorts test (TOST), verifies correct loading of each MCM pin and tests pin connections for the presence of opens or shorts. The second test performed is a functional test which can detect logical stuck-at-x faults internal to the chip or on the intra-chip connections. Despite the extremely large densities per module, testing of a nine-chip module, for example, is accomplished in less than one minute.

Product flow

As described in Fig. 2, the source of product enters the test sector either through normal build procedures at the wafer and module level or through the rework cycle commonly used for the MCMs. In spite of testing differences among the products, technologies, or packaging, each device, wafer, or module follows the same test procedure. Upon arrival, the product is scheduled for tests based on tester availability, handler configurations (*i.e.*, I/O pad configuration), and production priority. After testing, each job is routed for immediate shipping or it is held for diagnostic analysis. As a result of the diagnostics performed, the product is shipped, retested, or recommended for rework activity.

Logistics system

The logistics system was developed to provide product and tester tracking and control throughout the test sector from all production lines including the IBM Quick-Turn-Around-Time single-wafer semiconductor production line [3]. The system resides on an IBM System/370 host computer, and is operated using IBM 3277 display terminals equipped with light pens. Because tester operators and test technicians are the predominant users, the system was designed to require minimal terminal experience and little or no operational instruction. The use of light pens reduces keyboard activity, thus reducing operational delays and inaccuracies. Users are provided with ongoing instructions and operating options on every screen. Feedback is transmitted after each input to inform the user of an error or to confirm the completion of a requested action. Remote printers located throughout the test area are used for printed reports and computer-generated forms.

Technology test characteristics

Prior to the implementation of the logistics system, technology test parameters were communicated from the test engineer directly to test system support personnel. All changes or additions became effective immediately upon entry by software support personnel. In order to improve efficiency in establishing new technologies, a technology update facility was incorporated in what came to be known as *the* logistics system. A set of product characteristics and test parameters were identified and normalized across each of the package types. The list included I/O pad configuration, wafer size, test sequencing codes, and standardized multiple-part-number wafer map layouts. Yield criteria for each technology were also established.

The update facility allows test engineers to supply, display, add, or change any of these characteristics for a new or existing technology and to specify an effective date for use of any data. In this way, changes are predefined by the engineers and automatically utilized by the system immediately or on a prescribed date. Introduction of a new technology requires one to two hours of terminal input time, depending on the number of wafer map part number configurations.

This time can be substantially reduced through a copy and edit feature which allows the engineers to use existing

technologies as a skeletal base for the new technology. Changes to parameters can be accomplished normally in approximately one to two minutes. Since all logistics applications retrieve technology information from this one central data base, any change is instantly proliferated to all functions.

Test setup

Test setup, or job build, as it is frequently called, is a two-step process which is initiated before the product is introduced into the test sector. As soon as the product is released into the production line, data indicating job makeup are transmitted to the final test sector and stored in the host system. This product preview information indicates the identity of all modules or wafers in the job, and their associated part numbers; for wafer product, it further defines the part number configuration of each wafer in the job. When the product is entered into test, the job content is verified against the preview information. All wafers or modules removed from the job during earlier process stages are also eliminated from the job preview.

The product data are then matched with the test parameters in the technology file and a tester job file is created. Any special test overrides requested by test engineering can be applied on an individual job basis at this time.

After the job file is created, an internal routing sheet is created by the logistics system identifying detailed job content and all product characteristics and test parameters designated for the job. Originally this form was set up by hand and key product statistics were entered into a log book. Job build was accomplished by keying the same information into a display terminal at the test station just prior to test. The total job entry and job build operations, which originally required up to sixty minutes of manual input per job, have been reduced to an average of five minutes, and virtually all data entry errors have been eliminated.

Testing

Product testing is handled exclusively by the controller/mini-computer network. The tester system software plan allows eight hours of stand-alone testing, encompassing the required data storage capacity. Logic wafer testing is the most limited of the test systems because of its high dependence on the host computer for part-number test information. Under normal test operations, all test result data are transmitted to the host computer for automatic job dispositioning immediately upon test completion.

Job dispositioning bottlenecks

Due to major differences in testing strategies, testing systems, and product characteristics among different technologies, the need for uniquely determining whether the product

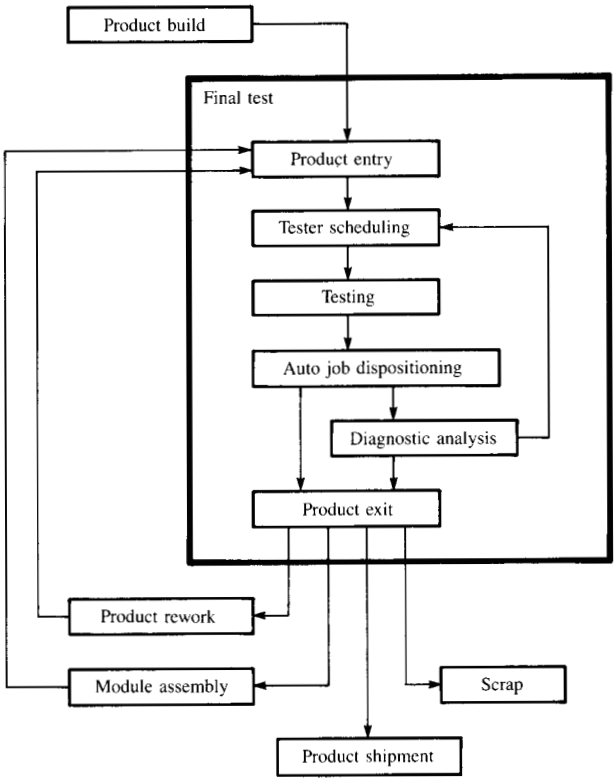


Figure 2 Product flow through a test sector.

should be transferred to the next process area arose. This gave rise to what we termed unique dispositioning systems. Each system was designed and tailored to the differences listed and the needs of users. The remaining topic deals with the dispositioning system used for logic wafers.

Product dispositioning for logic wafers had become a serious bottleneck in the final test sector. Contributing factors were as follows.

- Increases in product volume throughout the final test sector made product dispositioning a significant detractor of test sector throughput.
- Dispositioning of advanced technologies required more complex algorithms and calculations, placing an additional load on the test engineer (T/E) responsible for manually determining the disposition.
- Due to the increasing complexity of the technologies, the data volumes required to make the dispositioning decision had increased substantially.
- Round-the-clock T/E support to provide product dispositioning upon test completion was not always available for all shifts throughout the week, and was also not available on weekends.
- Jobs that could otherwise be shipped to the next sector immediately after test completion, *i.e.*, dicing and picking,

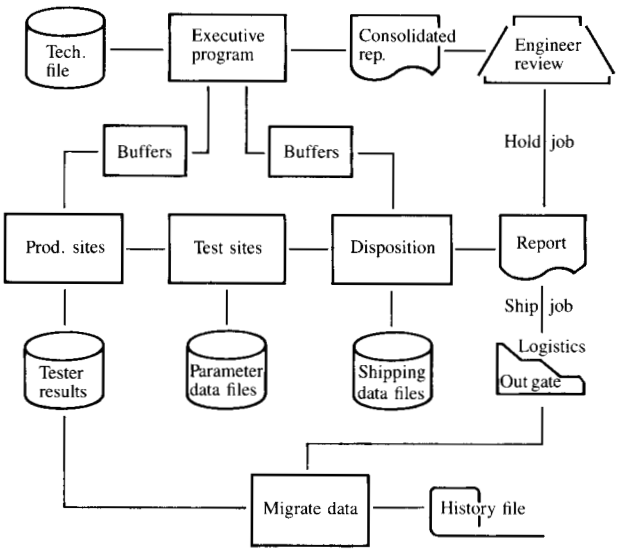


Figure 3 Overview of automatic job dispositioning system.

had to be placed into a wait state until a T/E was available to review the accumulated test data.

Development of an automatic product dispositioning system was viewed as a cost-effective solution to the job-dispositioning bottleneck, since all other alternatives required additional T/E manpower.

Automatic product dispositioning system

An automatic job-dispositioning program is initiated upon the completion of testing. It determines whether a job is to be shipped or held for further analysis by the T/E (see Fig. 3). The program itself is composed of a number of structured modules which analyze, summarize, diagnose, and act on the wafers based on inputs from both test results and the supporting technology-dependent data files. This computer-based decision process works with four major categories of data: yields, common mode failures (CMFs), failure codes, and test site parameters (all to be discussed later). The software to provide this information is composed of three functions: product site analysis, test site analysis, and the dispositioning process. All the functions are controlled, monitored, and linked together through an executive program. The executive program is initiated automatically at the completion of data transmission from the test controller to the host. Along with the job disposition report, a number of additional reports are generated at a remote job printer located near the tester.

Supporting data files

In order to incorporate the unique test characteristics and dispositioning requirements for each technology, a number of supporting data files were designed. Each technology has its own data files, allowing for generalized programming modules capable of handling wafers from all technologies. Included within this support data base are the following:

- Technology file—Contains device structure, conversion tables (used to correlate actual tests made at the tester to alphanumeric codes and failure names), and sort information (used in determining failure characteristics).
- Parametric limit and recirculating loop frequency files—Contain test limits and codes used to identify various arithmetic operations for device characteristics and scaling factors.
- Process yield file—Contains the algorithms to calculate process yields, further described by Stapper *et al.* [4]. These include processes to be monitored, screening equations (used to determine the proper sample size and to eliminate invalid and/or redundant data), process yield equations, and their exponents (used to adjust the yield for circuit density).
- Dispositioning file—Contains all technology-dependent variables and equations used for dispositioning.

Product site analysis function

The product site analysis function is used to summarize and report the product site chip test results and to provide yield, CMFs, and failure code information to the dispositioning function.

Yields calculated for use in the dispositioning decision are compared against target and/or projected figures. Yields calculated include

- Job yield—percent of good devices for the total job.
- Wafer yield—percent of good devices for each individual wafer in the job.
- Part-number yield—percent of good devices for each unique circuit design in the job.
- Wafer/part-number yield—percent of good devices for each unique logic implementation on each individual wafer.

CMFs are defined as the multiple occurrence of a unique failure. They are generated for each circuit design in the job for each wafer. Information provided by a CMF includes test failure code, pattern number, first failing pin address, number of pins involved in the test, and the number of times the failure occurred. Standard sort/merge routines are utilized along with additional sorting information from the technology file in determining a CMF. CMFs are used to identify failures which can indicate design problems, tester problems, process defects, or test pattern problems.

A failure code is an alphanumeric character used to represent failure categories. Each chip in the job is assigned a

code, whether the chip fails, passes, or is not tested. Codes are monitored in the dispositioning function for each part number and each wafer. They can identify tester-related problems, such as mis-probing, and also aid in determining which chips require retest.

Test site data analysis

Test site data are used to analyze characteristic circuit components (transistors and latches) not directly accessible on the product chips. The data, which are in the form of measurements taken from the test as a result of each test applied, are then compared to accept/reject criteria in the parametric limit and rlf files to determine if the device satisfies the ac or dc technology requirements. The parametric limit and rlf files contain both the upper and lower boundaries and unique codes for each test. These codes are used as flags to notify the test site software packages that additional computations are needed to interpret these results. This additional computation supplied by the T/E is translated into software code so that more than one test measurement result can be applied to a given test. For example, this analysis can compute the β measurement or a three-point resistance measurement [5] for better tester accuracy. Another important feature of the test site analysis is the conversion of all measurements into a prespecified uniform scale for use during diagnostic review. After all of the test cases are performed, the program extracts prespecified essential tests and the algorithms are applied to determine whether this wafer is to be accepted or rejected, independent of the pass/fail disposition of the product sites. All of the results are then printed, wafer by wafer, within the overall report package. After all of the wafers have been processed individually, the entire batch is summarized on a single report to provide the T/E with a snapshot of all the wafers.

Before these data are transferred to the next function within the software system (product disposition), an expected job yield is derived. The first step is to calculate process yields. The specific process yields to be included are specified within the technologies' process yield file. To determine a process yield, redundant data between processes and/or invalid data are first eliminated. Predefined tests are then applied on the remaining valid readings and compensations are made for circuit density. Process yields are multiplied together to derive expected yield (Fig. 4) and stored into the logistics yield system for a weekly process yield report. As job size increases, accuracy of this algorithm increases, due to the larger sample size. This procedure is useful to the T/E in identifying job yield detractors.

Upon completion of all of the product and test site processing, only the relevant information for the wafers in the job is loaded into a temporary buffer and transmitted to the dispositioning function via the executive program.

```
******  Y I E L D   P A R A M E T E R S  ******

    TERM      DESCRIPTION OF TERM
(1) Y/0       DESIGN LIMITED YIELD
(2) Y/LLY     LEAKAGE
(3) Y/SBD     SCHOTTKY-REVERSE LEAKAGE
(4) Y/K       1ST METAL OPEN/SHORT
(5) Y/1-2IL   INTERLEVEL SHORTS 1-2 METAL
(6) Y/1-2V    1-2 VIAS
(7) Y/M       2ND METAL OPEN/SHORT
(8) Y/2-3V    2-3 VIAS
(9) Y/2-3IL   INTERLEVEL SHORTS 2-3 METAL
(10) Y/RES    RESISTANCE

******  P R O J E C T E D   Y I E L D   F O R M U L A  ******

                A       B       C       D       E       F       G       H       I
Y/0 * Y/LLY ** Y/SBD * Y/K * Y/1-2IL * Y/1-2V * Y/M * Y/2-3V * Y/2-3IL * Y/RES
```

Figure 4 Yield parameters and formula used to calculate projected yield. The exponents A through I are supplied by technology engineers.

Dispositioning function

The final phase of this system is to determine whether the product should be shipped to the next sector or held for further analysis by the T/E. This process is performed through software on analyzed test data provided by the two previous functions and the job disposition file. The job disposition file contains the operations to be applied against the analyzed test data. These operations include comparing yields against targets, monitoring occurrences of specific CMFs and fail codes, and ensuring that processes meet specifications. Each data file is technology-dependent, so we can monitor or edit each technology's critical parameters throughout its life. A typical data file parameter set contains items such as

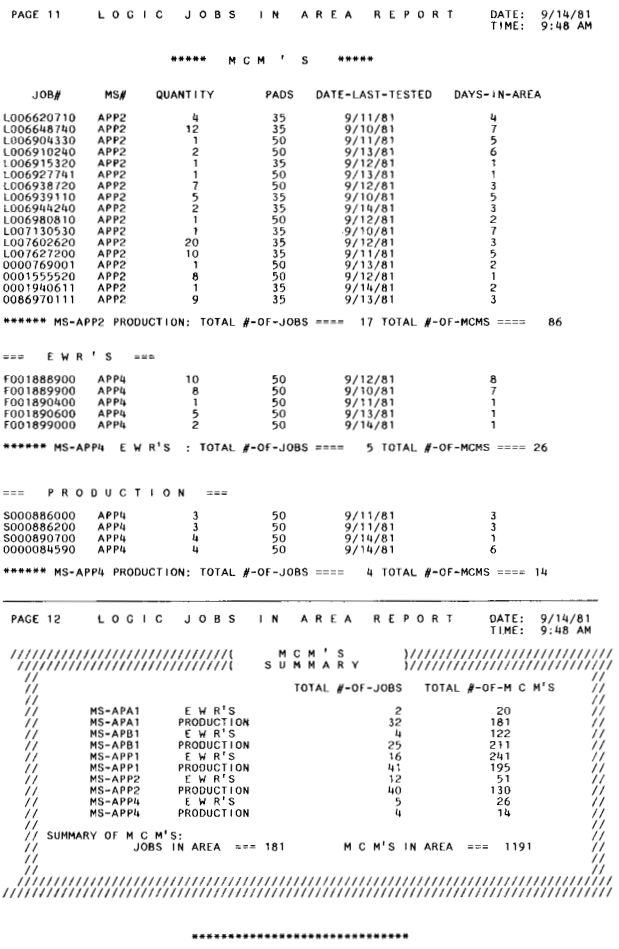
- Minimum yield on a batch of product.
- Minimum yield on a part number.
- CMFs on a wafer for any number of failing categories.
- CMFs on a job basis (group of wafers).
- Minimum yield based on selected failure types.
- Test site, dc, and ac test criteria.

The software first extracts all operations and variables from the file. Procedural flow is determined by the menu of operations. After all operations are performed, the job disposition report is generated and an indication of the final job status is transmitted to the logistics system, which tracks the percentage of jobs which are automatically shipped by the dispositioning system.

The final result, the job disposition report, specifies whether to *SHIP* or *HOLD* the job. On jobs that are held, information identifying why the job was held is included for T/E review. As discussed, multiple factors contribute to the disposition decision. Jobs designated as *HOLD* are reviewed by the T/E and *SHIP* jobs are moved out.

Historical data

The data associated with automatic job dispositioning in the final test sector work hand in hand with the data from all



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PAGE 11     L O G I C   J O B S   I N   A R E A   R E P O R T      DATE:  9/14/81
                                                                   TIME:  9:48 AM

                        *****   M C M ' S   *****

    JOB#        MS#     QUANTITY      PADS    DATE-LAST-TESTED    DAYS-IN-AREA

L006620710      APP2         4          35        9/11/81              4
L006648740      APP2        12          35        9/10/81              7
L006904330      APP2         1          50        9/11/81              5
L006910240      APP2         2          50        9/13/81              6
L006915320      APP2         1          35        9/12/81              1
L006927741      APP2         1          50        9/13/81              1
L006938720      APP2         7          50        9/12/81              3
L006939110      APP2         5          35        9/10/81              5
L006944240      APP2         2          35        9/14/81              3
L006980810      APP2         1          50        9/12/81              2
L007130530      APP2         1          35        9/10/81              7
L007602620      APP2        20          35        9/12/81              3
L007627200      APP2        10          35        9/11/81              5
0000769001      APP2         1          50        9/13/81              2
0001555520      APP2         8          50        9/12/81              1
0001940611      APP2         1          35        9/14/81              2
0086970111      APP2         9          35        9/13/81              3

****** MS-APP2 PRODUCTION: TOTAL #-OF-JOBS ====  17 TOTAL #-OF-MCMS ====   86

===   E W R ' S   ===

F001888900      APP4        10          50        9/12/81              8
F001889900      APP4         8          50        9/10/81              7
F001890400      APP4         1          50        9/11/81              1
F001890600      APP4         5          50        9/13/81              1
F001899000      APP4         2          50        9/14/81              1

****** MS-APP4  E W R'S  : TOTAL #-OF-JOBS ====   5 TOTAL #-OF-MCMS ==== 26


===   P R O D U C T I O N   ===

S000886000      APP4         3          50        9/11/81              3
S000886200      APP4         3          50        9/11/81              3
S000890700      APP4         4          50        9/14/81              1
0000084590      APP4         4          50        9/14/81              6

****** MS-APP4 PRODUCTION: TOTAL #-OF-JOBS ====   4 TOTAL #-OF-MCMS ==== 14

PAGE 12     L O G I C   J O B S   I N   A R E A   R E P O R T      DATE:  9/14/81
                                                                   TIME:  9:48 AM

                        M C M ' S
                        S U M M A R Y

                                          TOTAL #-OF-JOBS   TOTAL #-OF-M C M'S

        MS-APA1      E W R'S                      2                20
        MS-APA1      PRODUCTION                  32               181
        MS-APB1      E W R'S                      4               122
        MS-APB1      PRODUCTION                  25               211
        MS-APP1      E W R'S                     16               241
        MS-APP1      PRODUCTION                  41               195
        MS-APP2      E W R'S                     12                51
        MS-APP2      PRODUCTION                  40               130
        MS-APP4      E W R'S                      5                26
        MS-APP4      PRODUCTION                   4                14

SUMMARY OF M C M'S:
            JOBS IN AREA  ===  181        M C M'S IN AREA  ===  1191

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Figure 5 Sample logic jobs in area report showing the wafer inventory on a specified day using the activity report option. Engineering work requests (EWRs) represent experimental modules submitted for testing, as opposed to actual production modules. **Note:** *numbers and dates are not actual production data, but are given solely to demonstrate the program.*

previous jobs which have been tested within the area. These data are routinely transferred from the test area to a historical data base system to help the T/E in evaluating potential trends on products. By interrogating these data the T/E can locate any trends which may not be visible in a small sample size. If a trend does arise later, it is possible to modify the automatic job ship criteria to reflect this trend.

Before the automatic system was available, the user manually submitted these data. Not only was this a burden to the user, but it also created problems resulting from erroneous data.

Automatic job dispositioning advantages

Through the use of the wafer dispositioning system, the test sector has realized the following advantages:

- Dispositioning time has decreased from an average of twelve minutes spent by the T/E in diagnostic reviews per job (averaging nine wafers) to approximately twenty CPU seconds on the host computer.
- An increase in product throughput for the test sector has been realized due to immediate shipment of a significant percentage of product by manufacturing personnel upon receipt of the dispositioning report.
- The time required by T/Es to determine the disposition of jobs has been eliminated, thus providing them with additional time for product diagnosis.
- Dispositioning criteria have been formalized by using system software to contain all necessary engineering-specified algorithms and computations.
- Jobs that are held are accompanied by all constraints warranting a hold disposition.
- Human error in the dispositioning decision process has been eliminated.

Through automation, the need for additional manpower to maintain efficiency and consistency in product dispositioning was averted, thus providing a direct effect on production costs.

MCM diagnostic tracking

The production cost investment in the multi-chip module necessitates rework for all failing modules. Based on this strategy, all failing modules are held for detailed diagnostic analysis. Because the diagnostic analysis represents a significant percentage of total test time, the logistics system was extended to track MCM testing and diagnostic analysis activity separately. Logistics programs automatically route all failing MCMs from the test sector into a diagnostic sector utilizing appropriate accounting procedures. Based on the outcome of the diagnostic analysis, the product is either designated for retest and re-introduced into the test sector, or shipped. Activity reports monitor the fluctuating volumes of each sector, detailed product volumes, and length of stay in each area.

Product shipment

When a job is marked for shipment, the logistics system is used to transmit the job out of the test sector. The test results are summarized and an adjusted job yield is calculated using predetermined verified-process-yieldable chips. The yield for each wafer is then recalculated using the appropriate accounting code such as rlf reject, engineering purchase, prior process loss, etc., many of which are identified by the job dispositioning program and confirmed by engineering review. Final jobs are adjusted to include wafer losses, and the resulting yields are added to a cumulative yield data base which drives product yield analysis and reporting.

Upon completion of job accounting procedures, the logistics system executes a program which creates a wafer pick

map to match the good chip data identified during test. In addition, a flag is set to migrate the test data from disk packs to archive tapes, thus providing an automatic test data management system. Finally, the job is logged out of the test sector and an entry is made into a history file which allows cumulative product analysis and aids in field return studies.

Logistics reports

Product information is available via display terminals tied into the host system. Queries can be made regarding a specific job, a particular technology, or specific parts. These analyses can be made against product in test, undergoing diagnosis, or dispositioned and shipped within the previous six months. This feature has eliminated the use of all handwritten and manually maintained log books. Special requests for data from product control, chip picking, or process engineering regarding the product or test result summaries are answered within minutes. These requests would previously have required long, detailed searches through log books and extensive compilation.

In addition to the terminal reporting system, most information is available from remote printers conveniently located throughout the manufacturing site. The reports identify specific jobs and provide summaries by technology. As with the terminal query system, these reports provide key product statistics for jobs in test or in diagnostics (Fig. 5), or for shipped product (Fig. 6).

Logistics and auto job dispositioning extensions

The logistics system has been operational on the logic test floor for more than a year, with many of the features discussed added after initial installation. Within the next year, another logistics system will be added to monitor array testing. Although the base operations will be unchanged, certain modifications will be made to the technology data base to incorporate the use of partial yield array chips. Tracking operations will be adjusted to monitor two-temperature testing and job build will be modified to take advantage of the relatively small array part number set.

Other extensions include development of a tester utilization monitor to track the product tester parameters. In addition to identifying tester availability (by negative claiming of all hardware, software, test engineering problems), the actual output of each test system will be calculated and reported. This, coupled with the product data from logistics, will allow measurement of the actual test time variations between failing and acceptable product for each technology.

Finally, a test scheduler is planned to allocate dynamically all product to an appropriate tester on the basis of production priority, tester availability, and test handler constraints. The system will react to fluctuations in product mix and unexpected changes in tester availability or production priorities.

PAGE 7 L O G I C J O B S O U T G A T E D R E P O R T DATE: 12/20/81
(09/06/81 - 09/12/81) TIME: 9:52 AM

***** W A F E R S *****

JOB #	MS#	LINE	QTY	ACPTS	O-YLD	REMOVED	OUTGATED	DAYS-IN-AREA
=== P R O D U C T I O N ===								
*EP112	APP1	Q	11	11	0	0	09/12/81	2
PQT176	APP1	Q	17	16	1	0	09/11/81	2
*PRT957	APP1	Q	18	17	0	0	09/10/81	8
*PRT961	APP1	Q	18	18	0	0	09/09/81	6
P7T178	APP1	Q	6	6	1	0	09/11/81	2
*P7T424	APP1	Q	1	1	0	0	09/07/81	10
SP953	APP1	Q	3	2	1	0	09/09/81	6
*SP984	APP1	Q	8	8	0	0	09/10/81	1

	JOBS	WAFERS	ACCEPTS	O-YLD	REMOVES
**** MS-APP1 PRODUCTION: TOTAL #-OF ===	8	82	79	3	0

=== P R O D U C T I O N ===								
*GX894	APP2	Q	18	18	0	0	09/10/81	10
GX944	APP2	Q	3	2	0	1	09/09/81	8
*GX948	APP2	Q	16	16	0	0	09/09/81	7
*GX958	APP2	Q	8	8	0	0	09/09/81	6
*GX960	APP2	Q	7	7	0	0	09/11/81	2
*GX965	APP2	Q	26	26	0	0	09/07/81	2
*GX968	APP2	Q	11	11	0	0	09/10/81	5
GX974	APP2	Q	8	7	1	0	09/08/81	1
*GX975	APP2	Q	1	1	0	0	09/11/81	2
GX980	APP2	Q	6	6	0	0	09/12/81	1
*GX982	APP2	Q	15	15	0	0	09/10/81	5
*GX983	APP2	Q	1	1	0	0	09/08/81	2
GX991	APP2	Q	18	18	0	0	09/09/81	2
PGX195	APP2	Q	17	9	0	8	09/10/81	3
*PGX196	APP2	Q	18	18	0	0	09/10/81	3
*PGX230	APP2	Q	17	17	0	0	09/08/81	2
PGX231	APP2	Q	7	6	1	0	09/11/81	1
*PGX232	APP2	Q	9	9	0	0	09/07/81	4
PGX232A	APP2	Q	13	13	0	0	09/11/81	10
*PGX280	APP2	Q	17	17	0	0	09/08/81	1

	JOBS	WAFERS	ACCEPTS	O-YLD	REMOVES
**** MS-APP2 PRODUCTION: TOTAL #-OF ===	20	236	225	2	9

* INDICATES AUTO SHIPPED JOBS

PAGE 20 L O G I C J O B S O U T G A T E D R E P O R T DATE: 12/20/81
TIME: 9:48 AM

WAFERS S U M M A R Y

	TOTAL #-OF:	JOBS	WAFERS	ACPTS	O-YLD	REMOVES
MS-APP1	PRODUCTION	8	82	79	3	0
MS-APP2	PRODUCTION	20	236	225	2	9
MS-APP3	E W R'S	2	6	6	0	0
MS-APP3	PRODUCTION	1	2	2	0	0
MS-APP4	PRODUCTION	23	262	261	0	1
MS-APP5	PRODUCTION	12	75	73	1	1
MS-APP6	PRODUCTION	2	25	25	0	0
SUMMARY OF WAFERS:		68	688	671	6	11

Figure 6 Sample logic jobs completed report showing multi-chip module shipment during a specified period of time using the activity report option. **Note:** *numbers and dates are not actual production data, but are given solely to demonstrate the program.*

Summary

In response to the increasing semiconductor wafer and module volumes and the more complex technology menu in East Fishkill, two software systems, logistics and job dispositioning, were developed to help handle the increasing demands placed on the manufacturing test community. These two systems have alleviated serious bottlenecks in product test and have curtailed growing manpower requirements to support the increasing product projections, thereby indirectly affecting the ultimate product cost.

The logistics system provides computerized product track-

ing and more efficient tester setup capability. Operated almost exclusively by manufacturing personnel, the system performs scheduling and monitoring of product flow throughout the test sector. Report capability has been computerized, creating more extensive product analysis through an on-line query system with corresponding remote printer operations.

The automatic job dispositioning system provides computerized product dispositioning immediately upon completion of test. Through the use of sophisticated technology-dependent algorithms, product sites and test sites are analyzed and a decision to ship the job or hold it for engineering diagnostic review is mostly automatic. In addition to the actual disposition decisions, engineers are provided with a report detailing potentially critical product parameters which might affect overall product performance.

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