A. S. Bergendahl
S. F. Bergeron
D. L. Harmon

Optimization of Plasma Processing for Silicon-Gate FET Manufacturing Applications

The development and implementation of plasma processing techniques for silicon-gate FET manufacturing applications is described. Process requirements are discussed for the stripping of photoresist and the isotropic etching of thin films. A systematic approach for the optimization of these processes, involving the use of statistically designed multiparametric experimentation (MPE), is presented. This approach, in combination with the use of response-surface analysis techniques, is illustrated by examples of its application to typical processing problems. In addition, the multiparametric optimization of anisotropic etching is presented for potential plasma processing enhancements.

Introduction

Plasma processing, in the manufacture of VLSI silicon-gate FET logic and memory products, is fostered by economic and environmental factors as well as improved lithographic performance. The replacement of standard "wet" etching and resist stripping processes with plasma methods reduces deionized water and bulk chemical usage as well as chemical waste treatment requirements, while providing improved product design ground rules for more dense and productive chip designs.

A typical "wet" resist strip or a polycrystalline silicon (ϕSi) etch results in a primary chemical waste of 300 to 500 ml of concentrated liquid acid and consumes approximately 200 liters of deionized water. This compares with typical plasma processing requirements of about 12–15 liters (STP) of gaseous reactants, less than 2 ml of vacuum pump oil (which can be recycled), and no deionized water. To illustrate the improved lithographic control achieved with plasma etching *versus* that of "wet" etching, consider the definition of a ϕSi line in a manufacturing environment. For a 400-nm-thick resist film, a 2.5-μm-wide line in photoresist shrinks to $\approx$1.5 μm in ϕSi using "wet" etching, but only to $\approx$2.3 μm using isotropic plasma etching.

The development of processes for manufacturing applications requires experimentation to demonstrate that the process design criteria are satisfied and that the effects of all important parameters are understood at least empirically. The large number of plasma etching parameters complicates the development of plasma processes. This is especially true since the effects of such variables as the geometry of the reaction chamber, the nature and pressure of the discharge gas, the input power, and the frequency of excitation are not completely understood. Additional problems arise due to plasma-surface interactions that are affected by temperature and electrical bias of the substrate. The situation is further complicated by the number of etching characteristics (*e.g.*, rate, selectivity) which must be optimized for a particular process application. These factors combine to form a complex system that has defied conventional analysis. As a result, most process development to date has consisted of trial-and-error experimentation with only minimal attempts at optimization.

The most widely used approach has been to select arbitrarily a set of processing parameters and to evaluate separately the effect of each parameter on the etching process, holding all others constant. This approach is iterative and ignores interactions between parameters. As a result, the conclusions are often invalid, making the approach neither efficient nor desirable. An alternate approach to process development that overcomes most of these inadequacies uses

statistically designed multiparametric experimentation (MPE) to determine etching characteristics as functions of the processing parameters [1–5]. This approach, when combined with response surface analysis techniques, minimizes the trial-and-error aspect of process development and simplifies the identification of optimum operating conditions.

This paper describes the successful application of this approach at IBM to the development of resist stripping and etching processes for the manufacture of VLSI silicon-gate FET logic and memory chips. In addition, experimental results of process investigations aimed at improved lithographic performance are presented.

Experimental design

The problem of definition and optimization of useful plasma processes is simplified if the functional relationships between the controllable parameters (*e.g.*, gas flow, rf power, chamber pressure) and the system response (*e.g.*, etching rate, etching selectivity) can be adequately represented by a polynomial of degree d within the parameter space of interest. If this is true, the polynomial coefficients may be estimated by applying a least-squares fit to the values of the response observed for a set of points in the k-dimensional parameter space. The design of an experiment which allows this estimation is known as a dth-order design; it consists of a set of appropriately selected experimental points. These points are chosen to permit accurate approximation of the polynomial in the region of interest, to allow the determination of the adequacy of the polynomial fit, to minimize the required number of observations, and to simplify the extension to a design of order $d + 1$.

The authors have found that experimental designs which are appropriate for plasma processing development and which satisfy the above criteria can be defined on the basis of early designs introduced by Box and Wilson in 1951 [1] and by application of the techniques of Box and Hunter [2]. These experimental design methods and associated analysis techniques have been implemented via interactive APL programs.

The experimental designs used for the process optimization, and described in subsequent sections of this paper, are second-order central-composite rotatable designs that exhibit uniform precision. The choice of second-order designs ($d = 2$) is based on the variation of plasma processing responses observed by these authors and reported by others in the literature. The central-composite aspect of these designs refers to the construction of the designs from a group of central-point observations which have the parameter space coordinates $(0, 0, \cdots, 0)$. These points are enclosed by concentric circles, spheres, or hyperspheres of additional observation points. Two of these arrays of points are required for second-order designs. Third- or higher-order designs can be easily constructed by the addition of successive concentric arrays. The points on the innermost hypersphere form a hypercube with coordinates $(\pm 1, \pm 1, \cdots, \pm 1)$ and correspond to the standard 2^k factorial points. The points on the second hypersphere have coordinates $(\pm\alpha, 0, 0, \cdots, 0)$, $(0, \pm\alpha, 0, \cdots, 0), (0, 0, \pm\alpha, \cdots, 0), \cdots (0, 0, 0, \cdots, \pm\alpha)$, where α is chosen to satisfy other design requirements. For example, α can be chosen to produce a rotatable design in which the variance of the estimated response is constant at a fixed radius ρ from the design center. The further condition that the variance at $\rho = 0$ be equal to the variance at $\rho = 1$ is referred to as *uniform precision* and can be approximated by varying the number of experimental observations made at the design center.

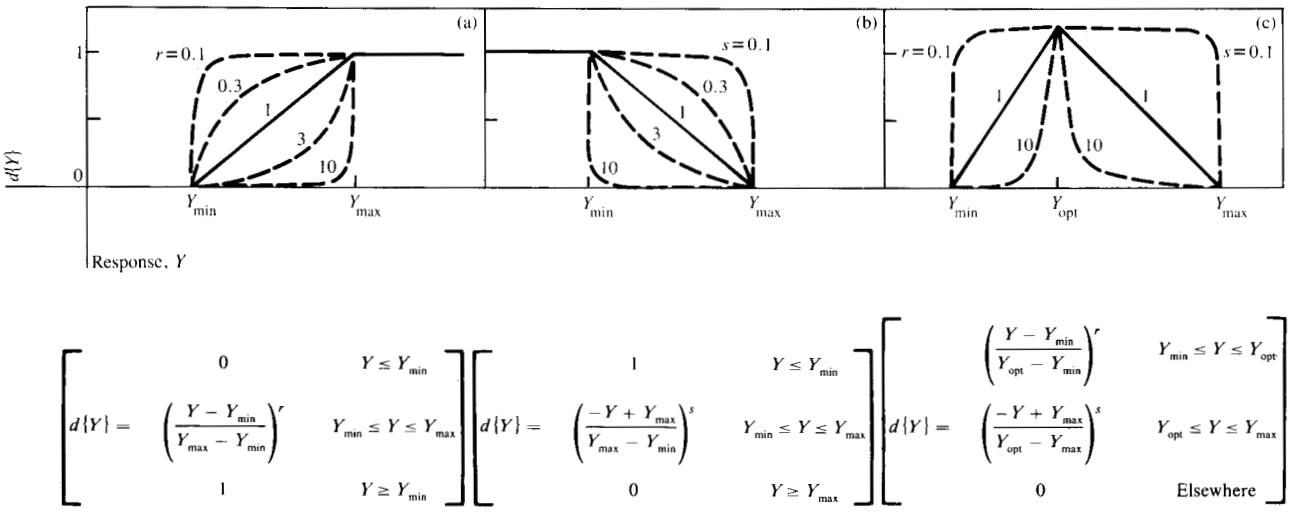
Response surface analysis

The least-squares polynomial fit to the experimental data can be accomplished by standard multivariate regression techniques. These techniques also provide the experimenter with information regarding the relative significance of each of the parameters. This information can be used to determine which parameters must be controlled for the optimization of individual responses.

There are a variety of techniques beyond standard regression analysis which can also be used with MPE to provide the experimenter with useful information. The following discussion deals with two of these techniques which have been particularly useful: ridge analysis [3] and desirability-function analysis [4].

Ridge analysis provides a method for selecting those conditions within the range of an experimental design that have the "best" response when either a minimum or maximum value is desired. In this technique, the maximum (or minimum) response is determined for each of a series of hyperspheres about the design center, with radii ranging from 0 to the largest radius within the experiment. These values can then be used to determine the absolute maximum (or minimum) response and the corresponding processing conditions. In addition, a comparison of the changes required in each of the parameters to produce a desired change in the response can be used to rate the relative importance of the parameters.

Although ridge analysis is effective for maximizing or minimizing one or at most two responses [5], this in general is not sufficient for optimization of a process. Many processes require the simultaneous optimization of multiple responses. Furthermore, the desired value of a particular processing characteristic may be within a range of acceptable values rather than at a minimum or maximum. For these cases, the use of desirability function analysis may be preferred. With



$$d\{Y\} = \begin{cases} 0 & Y \le Y_{min} \\ \left(\dfrac{Y - Y_{min}}{Y_{max} - Y_{min}}\right)^r & Y_{min} \le Y \le Y_{max} \\ 1 & Y \ge Y_{min} \end{cases} \quad d\{Y\} = \begin{cases} 1 & Y \le Y_{min} \\ \left(\dfrac{-Y + Y_{max}}{Y_{max} - Y_{min}}\right)^s & Y_{min} \le Y \le Y_{max} \\ 0 & Y \ge Y_{max} \end{cases}$$

$$d\{Y\} = \begin{cases} \left(\dfrac{Y - Y_{min}}{Y_{opt} - Y_{min}}\right)^r & Y_{min} \le Y \le Y_{opt} \\ \left(\dfrac{-Y + Y_{max}}{Y_{opt} - Y_{max}}\right)^s & Y_{opt} \le Y \le Y_{max} \\ 0 & \text{Elsewhere} \end{cases}$$

Figure 1 Desirability transforms $d\{Y\}$ for a response which is required (a) to be maximized, (b) to be minimized, or (c) to exist within a range of acceptable values.

this technique, the optimum value, as well as the minimum and maximum acceptable values of each response Y_i, are used to define desirability transforms $d_i\{Y_i\}$.

The definition of these transforms is illustrated in Fig. 1 for the cases where the desired response is a maximum, a minimum, or within a range of acceptable values. For these transforms, a value of 0 indicates an unacceptable response and a value of 1 indicates an optimum response. An overall desirability function for the process D can then be obtained for any set of conditions by first performing the desirability transformations of the individual responses and then calculating the geometric mean:

$$D = \left[\prod_{i=1}^{n} d_i\{Y_i\}\right]^{1/n}, \tag{1}$$

where n is the number of responses. The value of D has the same meaning for the process as $d_i\{Y_i\}$ has for the ith response. Note that an unacceptable value for any of the transformed responses results in an unacceptable process desirability. Since the desirability of a given set of processing parameters can now be expressed by the single function D, standard univariate computer searching techniques can be used to maximize D and, thus, to optimize the process.

Plasma resist stripping

The successful manufacturing application of plasma resist stripping in the early 1970s [6] preceded the plasma etching of thin films. However, trace metallic components (mostly tin) of commonly used negative photoresists were not removed during the ashing or stripping process [7]. Small amounts of halogen-containing gases were added to the oxygen-stripping gas to both enhance the stripping rate and trap the metal contaminants in a surface reaction so that they could be removed in subsequent cleaning steps [8]. However, occasionally etching of the exposed silicon was observed.

A similar problem arose when positive photoresists, which require inorganic developers containing potassium or sodium salts, were stripped by using an oxygen plasma [9]. Such resists contain trace amounts (ppms) of sodium, a source of mobile ions which might diffuse into the SiO_2 surfaces during plasma stripping in the presence of high temperatures. Although Na, Li, and K may diffuse into the surface of SiO_2 films during oxygen plasma resist stripping, no cross-contamination from Na-doped wafers to previously Na-free wafers was observed. Small amounts of CF_4 could be added to the stripping gas to trap the alkali metal ions on the surface for removal by subsequent processing. This technique is effective because the dielectric integrity of thick ($\gtrsim$100 nm) SiO_2 gates is insensitive to the slight SiO_2 etching which results from the presence of CF_4 in the oxygen discharge. In the case of thin gate oxides, an alternate approach is required.

• *Processing criteria*

Numerous plasma resist stripping requirements must be satisfied for the successful manufacture of silicon-gate FET devices. Oxidation of silicon and ϕSi films must be minimized to permit formation of buried ohmic contacts. Etching of thin oxide films should be minimized to prevent degradation of the gate thickness tolerances or device breakdown voltages, or loss of dielectric strength. Silicon and ϕSi etching must be minimized to maintain dimensional control and to prevent modification of the silicon surfaces. Radiation

damage to both silicon and SiO_2 films (and interfaces) must be minimized to avoid degradation of capacitor storage lifetimes and shifts in the device threshold voltages. Contamination by mobile ions must also be minimized. An adequate process must also strip the photoresist which, because of exposure to plasma etching, may have been chemically or physically altered, in which case common wet stripping methods may no longer be effective. The process should be applicable, with acceptable throughputs, to the various wafer diameters needed, while simultaneously meeting all the previously mentioned requirements.

• *Process development and implementation*

The desired characteristics of a plasma resist stripping process are achieved by two approaches: 1) modification of process equipment and parameters to minimize both oxidation of the exposed silicon and infiltration of mobile ions, without seriously extending the stripping time; and 2) addition of a small amount of a selected Cl- and F-containing gas to the oxygen-stripping gas, to reduce contamination by mobile ions without attack on the exposed SiO_2, Si, or ϕSi surfaces.

The system used in these stripping experiments is a barrel-type etcher/asher [10] which has been modified as follows: The chamber coil spacings were adjusted to increase generation of oxygen atoms and excited molecules toward the front of the reaction chamber in order to compensate for the higher wafer temperature [11] and stripping efficiency near the rear of the chamber. The Faraday cage or etching tunnel was replaced by one with greater optical transparency (*i.e.*, the ratio of the area of the perforations to the area of the tunnel was increased) depending on the relative strip rate, apparent oxide growth, and reactor temperature, as measured via the standard system thermocouple (see Fig. 2). The etching tunnel was retained to prevent or reduce energetic surface bombardment, surface oxidation, and radiation damage. Replacing the quartz wafer boats with adjustable aluminum boats permitted the stripping of at least fifty wafers (up to 125 mm in diameter) centered along the tunnel axis.

Figure 3 shows the results of an MPE evaluation of both stripping time t and reactor temperature T for a system with the modifications just described. Although stripping proceeds more rapidly as the temperature increases, a low temperature is desirable to reduce alkali metal diffusion into SiO_2 surfaces. Thus, an intermediate temperature is required for the optimal process. In this case, since there are only two responses to be optimized, process definition can be accomplished immediately with the aid of the dual contour plot in Fig. 3. The indicated operating point (shown with an asterisk on the figure) reflects the compromise made to limit the maximum temperature and minimize stripping time.

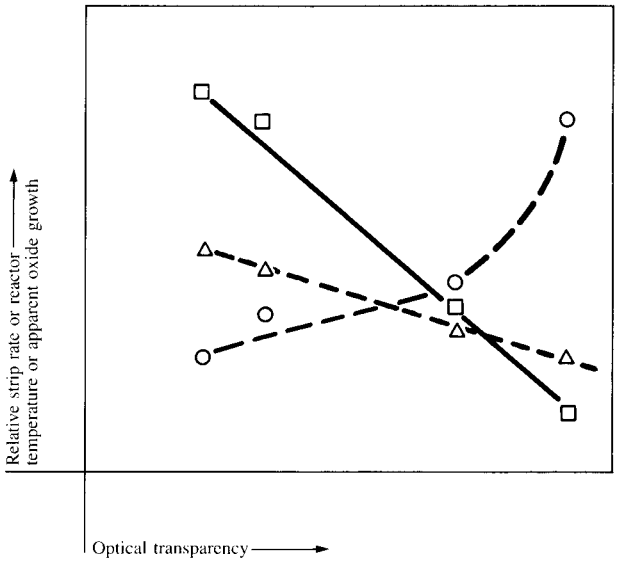


Figure 2 Relative stripping rates (○), reactor temperatures (□), and apparent oxide growth on silicon (△) as functions of the optical transparency (open area/total area) of the etching tunnel.

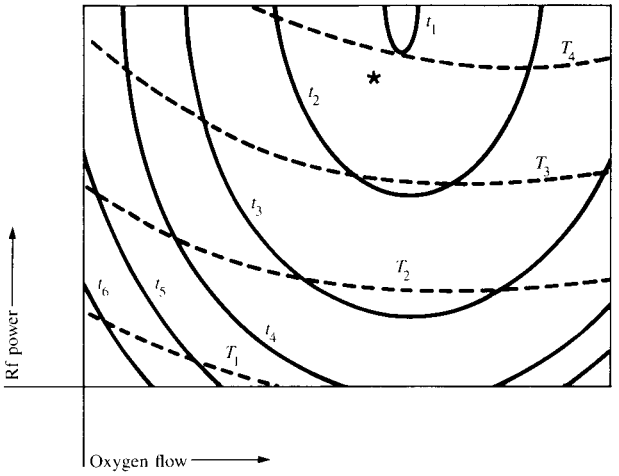


Figure 3 Multiparametric response surfaces for time (solid lines) and reactor temperature (dashed lines); $t_1 < t_2 < t_3, \cdots$ and $T_1 < T_2 < T_3, \cdots$.

The approach taken to reduce mobile ion diffusion involved the addition of trace quantities of $CHFCl_2$ to the oxygen stripping gas. The $CHFCl_2$ provides an anion which can bind mobile Na^+ ions to the surface during the stripping process, but allows subsequent removal of the sodium salts by wet processing. Since low levels of this gas in the O_2 plasma did not measurably etch silicon, ϕSi, silicon nitride, pyrolytic SiO_2, thermally grown SiO_2, or phosphosilicate glass, but did provide the required reduction in mobile ion contamination while increasing the stripping times only slightly, this method was used in subsequent processing.

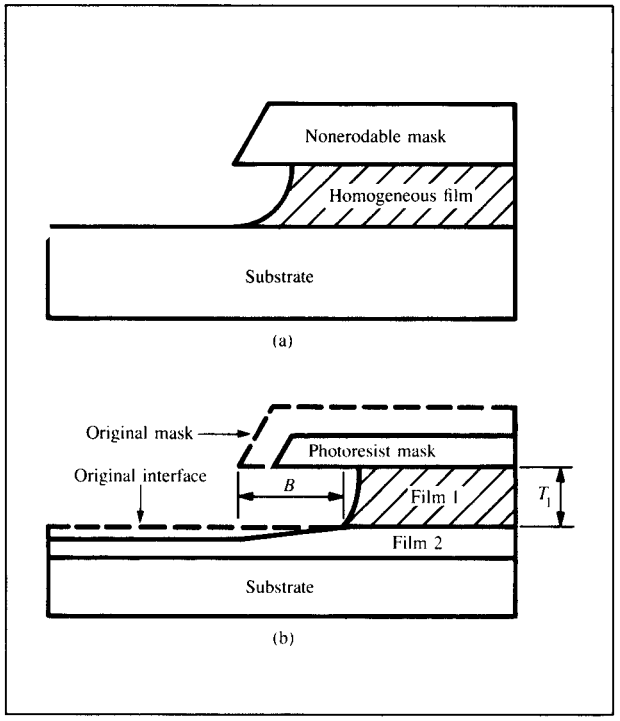


Figure 4 Isotropic etching (a) at an etching endpoint ($S_{1M} = 0$) and (b) at 100% over-etch ($S_{1M} \neq 0, S_{12} \neq 0$).

Since thin-gate dielectrics (*e.g.*, SiO_2) are most vulnerable to etching degradation, these were used to evaluate the performance of the stripping process. The observed flatband voltages, dielectric strengths, and mobile-ion concentrations were statistically equivalent for plasma-stripped, wet-stripped, and unprocessed oxide controls. Implementation of the resist stripping process involved transfer of the process to a manufacturing plasma system. This procedure was simplified through the use of an MPE evaluation in which only the most significant process parameters were investigated. In addition to simplifying the system-to-system transfer, this evaluation provided the process control and diagnostic information required for routine processing.

Plasma etching

Typical plasma etching processes needed for the manufacture of VLSI silicon-gate FET devices include 1) the definition of patterns in thin low-pressure chemical vapor-deposited (LPCVD) Si_3N_4 films over even thinner SiO_2 films; 2) the patterning of highly doped ϕSi conductors and FET gates over thin-gate SiO_2 dielectrics; and 3) the etching of vias in plasma-deposited silicon nitride insulators to contact Al-Cu-Si metallurgy. The plasma etching requirements for each of these applications are different; however, in all cases, high etching selectivity and tight linewidth control are needed. For some cases, a non-vertical etch profile is also desired to avoid reliability concerns such as degradation of sidewall dielectric integrity or inadequate step coverage in subsequent layers.

In this section the development and implementation of a polysilicon etching process is described to illustrate the optimization of *isotropic* (nondirectional) plasma etching [12]. The use of more directional (*anisotropic*) etching [13, 14] for the improvement of linewidth and profile control is addressed in a later section on processing enhancements.

• *Isotropic etching*

Isotropic etching refers to an etch rate in a homogeneous film that is independent of the etching direction (*i.e.*, horizontal and vertical etch rates are equal). Figure 4(a) presents the profile of an isotropically etched sample which is cross-sectioned at the edge of a nonerodable mask. This diagram shows the profile at *etch end point*, the point at which etching of the unmasked film has just been completed. The percent of etching time (or equivalent film removal) beyond this point is referred to as the amount of *over-etch* Θ.

The etched profile which undercuts the mask can be described at any time by a circular arc, with its center at the bottom of the mask and a radius equal to the product of the etch rate and the etch time. The situation is complicated by the simultaneous etching of the mask and/or the underlying film. These factors are normally described by an etching selectivity $S_{12} = E_1/E_2$, where the E are etch rates of films 1 and 2. Figure 4(b) indicates the resulting profile for an $\approx$100% over-etch, where the selectivities between the film to be etched (1) and the mask (M), S_{1M}, and between the film to be etched (1) and the underlying film (2), S_{12}, have finite values greater than one.

The horizontal distance between the bottom edges of the mask before etching, and of film 1 after etching, is referred to as the etch bias B. This parameter is important in characterizing the degree of linewidth control achieved by a given etching process, and may be used to illustrate the major problem encountered with isotropic etching. From geometrical considerations, B may be expressed as a function of over-etch Θ for $S_{1M} = \infty$:

$$B = T_1 \left\{ \left(1 + \frac{\Theta}{100} \right)^2 - 1 \right\}^{1/2}, \qquad (2)$$

where T_1 is the thickness of film 1. It can be readily determined from Eq. (2) that during isotropic etching the etch bias increases rapidly with over-etch. Since some amount of over-etch is required to compensate for variations in the film thickness and etch rate, the usefulness of isotropic etching diminishes as the minimum dimensions of the device structures approach $\approx 4\times$ the film thickness.

• *Process development and implementation*

The plasma etching of ϕSi is considered to be a critical step in the processing of silicon-gate FET devices. For this reason, the development and implementation of a ϕSi etching process is discussed in detail. The plasma system used in this work consists of a barrel-etch system [10] modified by the addition of a planar electrode assembly. The rf power is applied to the top electrode and the wafers are placed on the grounded, temperature-controlled lower electrode. The etchant gas is introduced to the chamber above the front edges of the electrodes and is exhausted at the back of the chamber.

The objective of the process is to uniformly etch n^+-doped ϕSi films without eroding the diazo-type positive photoresist mask or etching the underlying thin-gate SiO_2 dielectric. To avoid reliability problems arising from vertical etching profiles, the chosen process includes an isotropic $CF_4 + O_2$ plasma etch.

An MPE procedure which used a series of central-composite rotatable experimental designs was used to determine the ϕSi etch rate, the ϕSi-to-photoresist and ϕSi-to-SiO_2 selectivities, and the ϕSi etch rate uniformity $U_{\phi Si} = (3\sigma/E_{\phi Si})100$, where σ is the standard deviation of $E_{\phi Si}$. Empirical responses for these process characteristics were determined as functions of six parameters: electrode separation, chamber pressure, total gas flow, electrode temperature, rf power, and O_2 concentration. The initial experiments indicated that the electrode temperature and O_2 concentration could be fixed at relatively low values without detrimentally affecting the outcome. Analysis of the data from the subsequent experiments results in polynomials of the form of Eq. (1), with $n = 4$. For example, the normalized equation for the ϕSi etch rate uniformity is

$$\begin{aligned} U_{\phi Si} = {} & 43 - 40.8x_1 + 4.4x_2 + 27.9x_3 + 24.2x_4 \\ & + 8.1x_1^2 - 1.62x_2^2 + 12.5x_3^2 + 4.9x_4^2 \\ & + 0.3x_1x_2 - 16.8x_1x_3 - 9.5x_1x_4 \\ & + 2x_2x_3 + 3.6x_2x_4 + 6.7x_3x_4, \end{aligned} \quad (3)$$

where the x_i correspond to values of the dependent parameters; x_1 is the rf power, x_2 is the total gas flow, x_3 is the chamber pressure, and x_4 is the electrode separation. The coefficients are normalized to specified ranges of the individual parameters. It is apparent from Eq. (3) that several of the terms are not important. Standard regression analysis of the data indicates that all of the terms involving x_2 are insignificant. Consequently, it can be concluded that total gas flow does not appreciably influence the ϕSi etch rate uniformity within the investigated parameter space. This analysis is useful in the determination of those process parameters that must be controlled for each response. A similar analysis indicated that the gas flow does contribute to the ϕSi etch rate and the etching selectivity; therefore, it must be considered for the overall process optimization.

Figure 5 indicates the desirability transforms $d\{Y\}$ used for the simultaneous optimization of the process characteristics. Since the ϕSi-to-SiO_2 selectivity was found to be acceptable for all process conditions, it is not included. A maximum value for the ϕSi etch rate $E_{\phi Si}$ (1.5 nm/s) was specified in order to allow sufficient time for recognition of the end point and termination of the etching before the etch bias could become unacceptably large. A minimum value of etch rate (0.2 nm/s) was specified to ensure reasonable wafer throughput.

The contour plot of the overall process desirability D [Fig. 5(d)] shows the region of operation (shaded) which was selected after computer optimization of the responses. The values of the rf power and total gas flow were thus fixed, giving a polysilicon etch rate $E_{\phi Si}$ of 1.0 nm/s, a polysilicon etch rate uniformity $U_{\phi Si}$ of $\approx$10% and a good ϕSi-to-photoresist selectivity $S_{\phi Si\text{-}pr}$. The process defined by this procedure was then implemented for the fabrication of actual silicon-gate FET devices. Figure 6 presents electrical linewidth measurements (process bias) from more than 100 wafers. Although the variation in linewidth due to other processing steps is included in these data, the control achieved by the optimized process is apparent.

The MPE approach has also been applied to optimization of polysilicon etching in plasma systems with different gas mixtures and/or geometries (*e.g.*, barrel and radial-flow, parallel-plate systems). In the past, a fair comparison of such systems/processes has been virtually impossible. However, such comparisons can now be readily performed with the aid of desirability function analysis by specifying the same desirability criteria for each case. This approach has been found to be useful for the selection of systems and/or processes.

Process enhancements

Circuit dimensions continue to decrease to provide improved density and performance. When the required dimensional control approaches the lithographic limits, adjustments of the mask dimensions can no longer be used to compensate for etch bias. As a result, the mean value and range of etch bias must be reduced beyond those which can be routinely achieved with isotropic etching. Furthermore, the variation in isotropic etching profiles that results from the variable amounts of over-etch required by system and film nonuniformities becomes unacceptable for many processes.

A potential solution to these problems is the development of anisotropic etching processes, in which the vertical etch

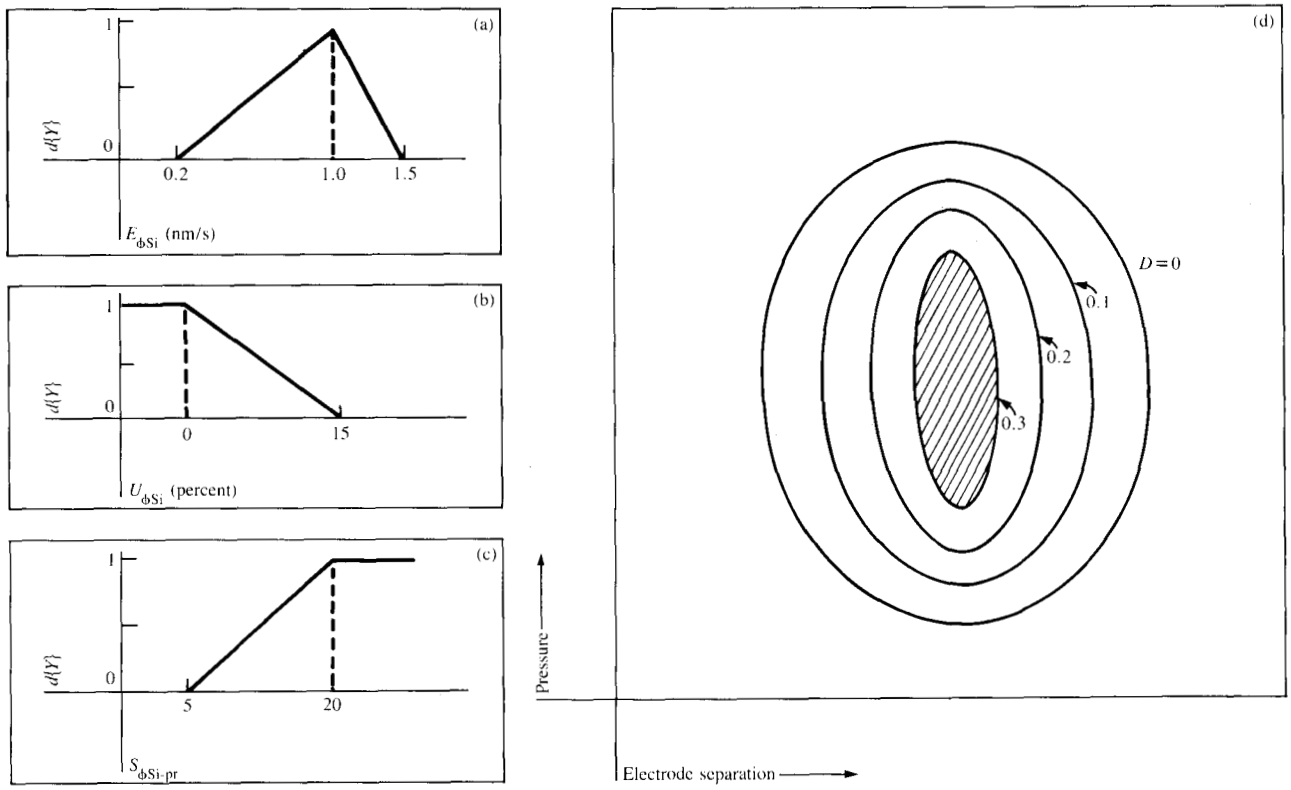


Figure 5 Desirability transforms $d\{Y\}$ for (a) ϕSi etching rate $E_{\phi Si}$, (b) ϕSi etching rate uniformity $U_{\phi Si}$, and (c) ϕSi-to-photoresist selectivity $S_{\phi Si\text{-}pr}$. (d) The total process desirability D as a function of chamber pressure and electrode separation.

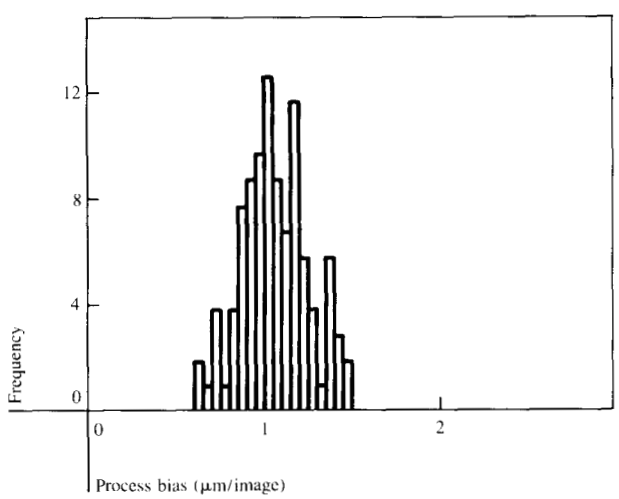


Figure 6 Electrical linewidth variation for 400-nm-thick polysilicon films.

rate E_V is greater than the horizontal etch rate E_H. Additional advantages may be obtained through the use of hybrid or multi-step etching, in which several processes, each exhibiting different degrees of anisotropy, are used in succession.

The benefits of such processes are illustrated in Fig. 7 by the variation of etch bias with over-etch for a 400-nm film. The isotropic curve, derived from the relation in (2), represents the case where $E_V = E_H$. Completely vertical etching occurs for $E_H = 0$, as indicated by the horizontal line in the figure. In both cases, a nonerodable mask is assumed. The area between these curves represents the reduction in etch bias which is potentially available with anisotropic or hybrid processing. The data points indicate the results of an actual process that is discussed in a later section of this paper. By reducing the effect of over-etch on etch bias, the range of etch bias that can be routinely produced can be decreased. This, in turn, gives improved linewidth control.

• *Anisotropic etching*

Significant progress has been made in the achievement of anisotropic etching using reactive-ion etching (RIE) [1] and chlorinated hydrocarbons [14]. The use of these techniques for the development of anisotropic processes can be simplified with the aid of MPE. The definition of anisotropy allows the etching profiles to be vertical or tapered, or to approach those of the classic isotropic case. Thus, to evaluate anisotropic etching, the systematic quantification of experimentally produced edge profiles is necessary. Since profiles are

often produced which exhibit some degree of curvature, the definition of edge slopes or angles is not appropriate. To alleviate this problem, a coefficient of directionality C_e is defined (see Fig. 8): $C_e = 1 - [(m + h)/v]$. This coefficient is an estimate of the directionality produced by an etching process, and it is determined from measurements of edge profiles and film-to-mask selectivities. A value of 0 represents an isotropic etched profile, while a value of 1 refers to a vertical etched profile (assuming that mask loss m during the etching process is much less than horizontal film loss h).

Anisotropic etching was studied using MPE for the evaluation of polysilicon etching in a radial-flow parallel-plate system [15]. The rf power was applied to the upper electrode and the etchant gas was a mixture of C_2F_5Cl and O_2. The investigated process parameters were rf power, chamber pressure, O_2 concentration, and electrode temperature. The electrode separation and total flow were held constant since the variation of these parameters was unnecessary for achieving variable anisotropy. Samples used to determine directionality coefficients were prepared by etching to endpoint, as determined by laser interferometry. Responses measured included the etch rate of polysilicon, associated selectivities to thermal oxide and resist, and the coefficient of directionality C_e.

Figure 9 depicts the observed range of C_e for various rf powers and electrode temperatures at optimized values for the chamber pressure and O_2 concentration. Also shown are SEM photographs verifying the predicted edge profiles for the process conditions indicated on the contour plot. Note that the film-to-mask selectivity must be included in the determination of C_e.

The results of this study demonstrate the ability of MPE to evaluate and model the degree of anisotropy. Thus, MPE can be used to simultaneously optimize directionality as well as other responses (etch rate, selectivities) to obtain a desired process. Since MPE provides empirical descriptions of the effects of multiple parameters on the etching process, it does not require the etching mechanism to be known. However, the data derived from MPE can be used to support mechanistic studies [16], as illustrated by the following example.

A mechanism for the observed variation in anisotropy has been previously hypothesized to be an ion-assisted phenomenon [17]. In this explanation, CF_x radicals and Cl atoms are adsorbed on the substrate surfaces. The Cl atoms are assumed to be the primary silicon-etching species, whereas the CF_x radicals presumably recombine with the Cl atoms and therefore inhibit the etching process. Ions, which are generated in the plasma, strike the substrate surface at nearly normal incidence. This bombardment dissociates the CF_x-Cl product, enhances the Cl-Si reaction, and thus

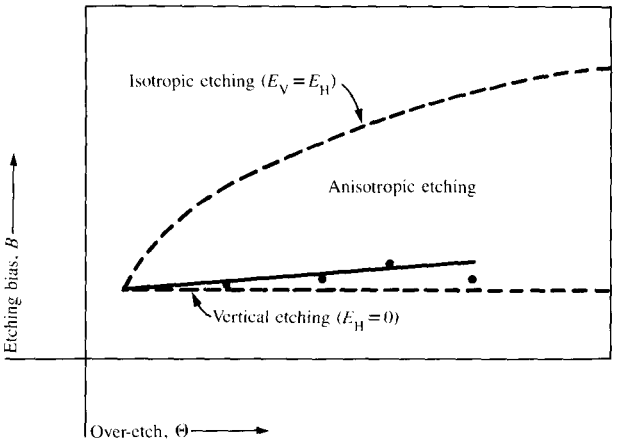


Figure 7 Etching bias B as a function of the over-etch Θ.

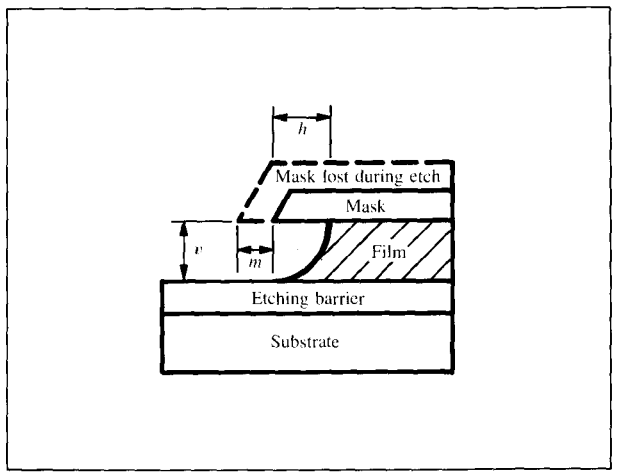


Figure 8 Definition of the estimated coefficient of directionality C_e; $C_e = 1 - [(m + h)/v]$, where h is the horizontal undercut, v is the vertically etched film thickness, and m is the horizontal mask loss.

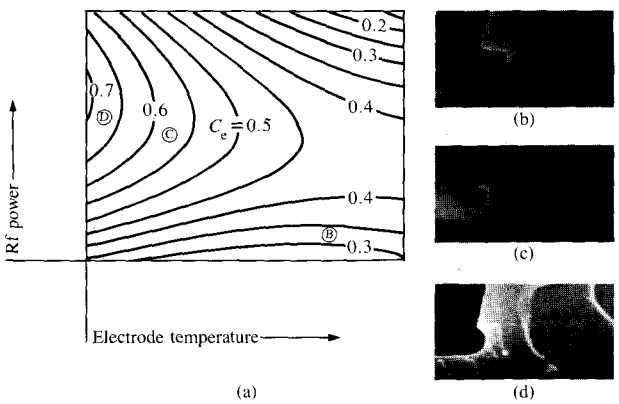


Figure 9 (a) The estimated coefficient of directionality C_e as a function of rf power and electrode temperature at a constant chamber pressure and O_2 concentration. The circled letters (B, C, D) on the plots indicate the process used for the sample edge slopes depicted in (b) $C_e = 0.30$, (c) $C_e = 0.58$, and (d) $C_e = 0.70$, respectively. Note that the apparent edge slopes in (b)–(d) have been corrected for the selectivity between the polysilicon and the resist.

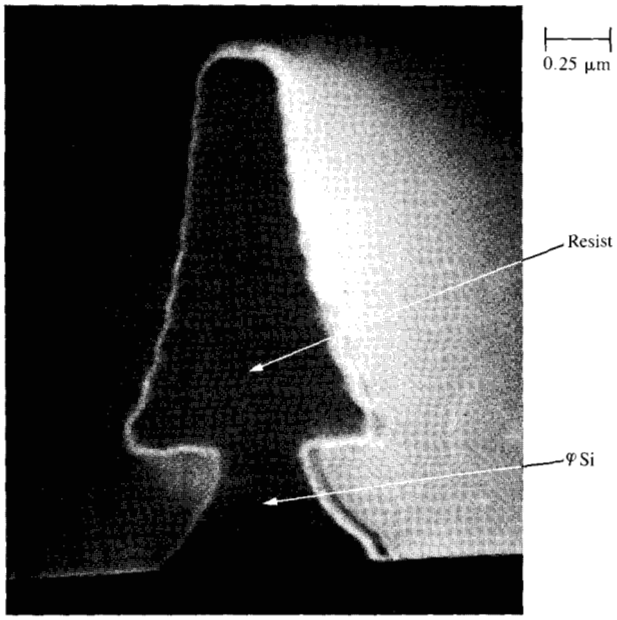


Figure 10 Edge profile of a polysilicon line produced using a two-step hybrid process. (The unsymmetrical appearance of the profile is an artifact of the sample cleavage obtained in this SEM.)

accelerates the etching process. However, those surfaces that see less ion bombardment (*i.e.*, the surfaces below the edge of a mask) are protected by the adsorbed CF_x radicals and are etched more slowly.

The use of ridge analysis in the multiparametric evaluation of anisotropy revealed that temperature was the most important contributor to the degree of directionality. It is conjectured, within the framework of the previously discussed mechanism, that the rf power, pressure, and O_2 concentration determine the availability of reactive species as well as the ionic bombardment, and thus control the potential for anisotropy. However, the temperature of the substrate may control the desorption rate of the protective CF_x radicals and may therefore control the observed directionality.

• *Hybrid etching*

Although anisotropic etching reduces the increase of etch bias with over-etch, it has been observed that edge profiles steepen with over-etch for some anisotropic processes in which $C_e < 1$. If the devices being fabricated are sensitive to the edge profile of the resultant structure, a hybrid process may be warranted.

This technique involves the optimization of multiple processes around different values of C_e. This task is relatively straightforward if an etchant system, such as the previously discussed C_2F_5Cl/O_2 system, has been characterized by MPE as exhibiting controllable anisotropy. The processing requirements, including the directionality, are specified in a desirability function which can then be systematically optimized.

Figure 10 shows an example of the results achieved for a two-step hybrid process in which approximately 85% of the film thickness was consumed by an isotropic etching step. The remainder of the film was removed with a significant over-etch by an anisotropic process in which $C_e \approx 0.95$. Other samples, prepared similarly but with less over-etch, exhibited identical profiles and equal or smaller etch biases. The measured variation of etch bias with over-etch for these samples has been shown in Fig. 7. These results indicate that hybrid etching is an effective technique for improving profile control while minimizing linewidth loss.

Summary

Statistically designed multiparametric experimentation (MPE), including response-surface analysis, has been developed for the systematic optimization of plasma processes. The effectiveness of this approach is demonstrated by its successful application to the development of plasma resist stripping and isotropic etching processes required for the manufacture of VLSI silicon-gate FET products. The capability of this approach to accurately model and optimize anisotropic etching for potential process enhancements has also been demonstrated. Finally, the use of MPE for system-to-system process transferral, process/system comparisons, and the investigation of process mechanisms is described.

Acknowledgments

The authors wish to thank J. Hamel and C. Hamel for APL programming, P. Libby for contributions relating to the evaluation of isotropic plasma etching, F. Martinet for help with chlorine-based directional etching, and B. Duncan for general technical assistance. In addition, the authors would like to acknowledge the encouragement and support of J. Wilson.

References and notes

1. G. E. P. Box and K. P. Wilson, "On the Experimental Attainment of Optimum Conditions," *J. Roy. Statist. Soc. B* **13,** 1 (1951).
2. G. E. P. Box and J. S. Hunter, "Multifactor Experimental Designs for Exploring Response Surfaces," *Ann. Math. Statist.* **28,** 195 (1957).
3. N. R. Draper, " 'Ridge Analysis' of Response Surfaces," *Technometrics* **5,** 469 (1963).
4. G. Derringer and R. Suich, "Simultaneous Optimization of Several Response Variables," *J. Quality Technol.* **12,** 214 (1980).
5. R. H. Meyers and W. H. Carter, Jr., "Response Surface Techniques for Dual Response Systems," *Technometrics* **15,** 301 (1973).
6. J. R. Hollahan and A. T. Bell, *Techniques and Applications of Plasma Chemistry,* John Wiley & Sons, Inc., New York, 1974.

7. H. G. Hughes, W. L. Hunter, and K. Ritchie, "Residues Remaining after RF Plasma Photoresist Removal," *J. Electrochem. Soc.* **120,** 99 (1973).
8. W. Kern and D. Puotinen, "Cleaning Solutions Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology," *RCA Rev.* **31,** 187 (1970).
9. G. Bell and R. Stokan, "Plasma Strip of Sodium-Contaminated Photoresists on Silicon Dioxide," *Proceedings of the Electrochemical Society,* Atlanta, GA, Oct. 1977, Extended Abstracts, p. 383.
10. The PFS/PDE/PDS-1002 plasma etch system, obtained from the LFE Corporation, Process Control Division, Waltham, MA.
11. Wafer temperature as a function of position in the reactor was measured by means of temperature-sensitive strips on the wafers.
12. S. M. Irving, K. E. Lemons, and G. E. Bobos, "Gas Plasma Vapor Etching Process," U. S. Patent 3,615,956, 1969.
13. L. Zielinsky and G. C. Schwartz, "Reactive Ion Etching," *Proceedings of the Electrochemical Society,* Toronto, Canada, May 1975, Extended Abstracts, p. 117.
14. H. Abe and K. Nishiolaco, "Micro-Fabrication of Photomasks by Gas Plasmas," *Proceedings of the Kodak Microelectronics Seminar,* Monterey, CA, 1976, p. 11.
15. *PK-2440PE/RIE Dual Plasma and Reactive Ion Etch System,* Plasma-Therm, Inc., Kresson, NJ.
16. G. E. P. Box and P. V. Youle, "The Exploration and Exploitation of Response Surfaces: An Example of the Link Between the Fitted Surface and the Basic Mechanism of the System," *Biometrics* **11,** 287 (1955).
17. C. J. Mogab and H. J. Levinstein, "Anisotropic Plasma Etching of Polysilicon," *J. Vac. Sci. Technol.* **17,** 721 (1980).

Received September 28, 1981; revised March 23, 1982

Albert S. Bergendahl *IBM General Technology Division, Burlington facility, Essex Junction, Vermont 05452.* Dr. Bergendahl is a senior engineer at the development laboratory in Essex Junction. He is currently a technical team leader responsible for definition and implementation of lithographic process development strategy, planning, process experimentation and definition, process transfer to manufacturing with appropriate equipment, and monitoring control measurement methods for silicon gate FET products. He joined IBM in Essex Junction in 1970. His early work in IBM included product reliability and testing studies related to understanding and modeling of atmospheric corrosion of LSI semiconductor products and packaging. Later he worked on application of surface chemistry and electrical testing and characterization techniques to solving semiconductor processing and instrumentation problems related to photolithographic, solid state diffusion, and chemical vapor deposition aspects of LSI fabrication. Dr. Bergendahl received a B.S. in electrical engineering in 1964, an M.S. in geology in 1965, and a Ph.D. in chemistry in 1970, all from the Rensselaer Polytechnic Institute, Troy, New York. From 1965 to 1967, he was a field engineer for Schlumberger Surenco, S.A., performing geophysical service to the petroleum industry. Dr. Bergendahl is a member of the American Chemical Society, the Electrochemical Society, the Institute of Electrical and Electronics Engineers, and Sigma Xi.

Steven Bergeron *IBM General Technology Division, Burlington facility, Essex Junction, Vermont 05452.* Mr. Bergeron received a B.S. in chemistry from Georgetown University, Washington, DC, in 1976 and graduated from the University of California at Santa Barbara with an M.A. in inorganic photochemistry in 1978. He joined IBM in 1978 and is currently a plasma process engineer developing dry etch processes for integrated circuits.

David L. Harmon *IBM General Technology Division, Burlington facility, Essex Junction, Vermont 05452.* Mr. Harmon is a process engineer responsible for photolithographic development at the laboratory. He received a B.S. in 1977 and an M.S. in 1979, both in electrical engineering, from the University of Maine, where he was engaged in the research of surface acoustic wave devices. Since joining IBM in 1979, he has worked in the area of plasma process development and optimization. Mr. Harmon is a member of Eta Kappa Nu, Phi Kappa Phi, Sigma Xi, and Tau Beta Pi.