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A VLSI Bipolar Metallization Design with Three-Level Wiring and Area Array Solder Connections

The ability to interconnect large numbers of integrated silicon devices on a single chip has been greatly aided by a three-level wiring capability and large numbers of solderable input/output terminals on the face of the chip. This paper describes the design and process used to fabricate the interconnections on IBM's most advanced bipolar devices. Among the subjects discussed are thin film metallurgy and contacts, e-beam lithography and associated resist technology, a high temperature lift-off stencil for metal pattern definition, planarized rf sputtered SiO_2 insulation/passivation, the "zero-overlap" via hole innovation, in situ rf sputter cleaning of vias prior to metallization, and area array solder terminals.

Introduction

The most advanced silicon bipolar chips in IBM's announced product line are those logic and memory array chips used in the thermal conduction modules (TCMs) of the IBM 3081 processors [1, 2]. Similar devices are used in the IBM 4300 and System/38, but they are joined to different substrates [3, 4]. The densest of these devices has up to 704 logic circuits or 3000 memory cells per chip. Experimental chips built with the same technology have 5000 logic circuits on a 7-mm by 7-mm square of silicon [5].

This dense chip packaging of circuits is made possible through the extensive wiring capability achievable with three levels of thin film metallurgy and insulator. To illustrate the level of development, if all of the thin film wiring on the three levels of a typical logic chip were joined continuously, a line approximately 2 meters long would be created. In earlier technology, much of the wiring now found in the thin films on the chip would have been done at the first or second level substrate package. Some of the benefits realized from this wiring migration from the package to the chip are higher reliability, better performance, more good circuits per wafer, and lower cost.

However, one of the complications resulting from denser logic chip wiring is the requirement for more input/output (I/O) connections on the chip. This need has been met in this technology by an area array of solder bumps on the face of the chip, a fully populated grid of 120 controlled collapse chip connections (C-4). The device is, in turn, "flip chip" joined to a multilayer ceramic substrate or an appropriate metallized ceramic substrate having a matching "footprint" of I/O terminals.

Three layers of wiring and a denser assembly of C-4 pads would appear to be a simple evolution from IBM's earlier integrated circuits and LSI devices. Some elements of the design are indeed old technology, such as the rf sputtered SiO_2 insulator, AlCu metal lines for electromigration resistance, and the metallurgical design of the C-4 solder bump. Yet other aspects are new and necessary deviations from the past designs, such as a contact system of PtSi plus a $Cr\text{-}Cr_xO_y$ diffusion barrier replacing the silicon doped Al of earlier products, partially planarized sputtered SiO_2 for the first interlevel insulator, new via technology, e-beam lithography, and lift-off fabrication of conductor lines on the

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first two levels of wiring. These modifications are discussed in detail in the sections that follow.

A sectional drawing of the three-level metallization with part of a C-4 pad is shown in Fig. 1. Note that the metallization gets thicker (also wider) at each successive layer. Much of this progression is to compensate for the topographic roughness which develops from replicating the profile of the silicon masterslice surface, lower level metallization, via holes, etc. The uppermost metal layers are especially thick (2.3 μm) because they also serve as power distribution buses. The actual thin film topography is shown in Fig. 2, a 90° metallographic cross section of the interconnection metal and insulator system on a typical logic chip.

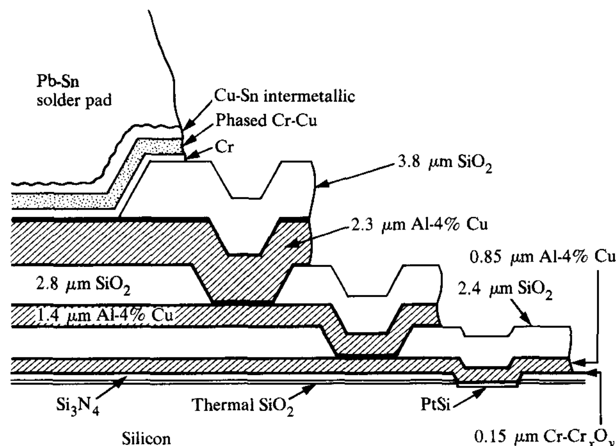

Figure 1 Sectional drawing of multilevel metallization-insulator for advanced bipolar devices.

Thin film metallurgy and contact system

In earlier IBM products the thin film metallurgy was either AlSi passivated by fired frit glass (solid logic technology), AlCu under rf sputtered SiO_2 insulator in the first integrated circuits, or AlCuSi for later shallow junction integrated circuits which were also passivated with sputtered SiO_2. In the current family of devices the contact metallization has required change. PtSi contact metallization is used on all n^+ or p^+ ohmic contacts and on n^- Schottky barrier contacts. The change resulted in part from the need for a stable, high barrier Schottky diode, but was equally necessary to make consistent low resistance ohmic contacts.

Work in the mid-1970s showed conclusively that the use of silicon doped Al or AlCu metal films would result in the solid state growth of p-doped silicon mesas or thin Si films on the single crystal ohmic contacts during process heat treatments [6]. One consequence of this growth of deposits was a high and variable contact resistance. Another consequence was the insertion of a rectifying layer between the metal and the n^+ contact. The deleterious effects worsen as the contact hole size diminishes; therefore, in the new generation of devices a change in the contact system was deemed necessary.

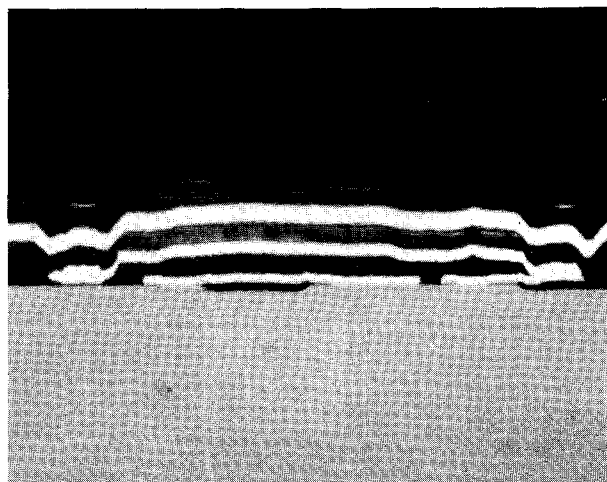

Figure 2 Metallographic cross section of three levels of metallization and SiO_2 insulation-passivation on a bipolar device (90° section, 1500×).

In order to protect PtSi contact metallurgy from alloying reactions with Al conductor metallurgy, a barrier layer was inserted between the two. Otherwise alloying would cause transformation of PtSi to Al_2Pt intermetallic compound, which would degrade the electrical behavior of the contact and permit the classical solid state diffusion of Si into Al, manifesting itself as Al alloying "penetration" [7]. The barrier selected was a Cr-Cr_xO_y cermet layer which has just enough Cr_xO_y in the grain boundaries of the Cr to serve as an effective diffusion barrier.

Aluminum alloyed with 4% Cu continues to be the principal conductor metal because it is orders of magnitude more resistant to Al electromigration than pure Al [8]. Because the Cr-Cr_xO_y diffusion barrier is present, there is no further need for Si doping of the AlCu.

The presence of the Cr-Cr_xO_y barrier layer results in additional electromigration resistance in the first level conductor relative to simple Al-Cu. It has been suggested that heat treatment of the film during wafer processing causes a transition metal enhancement of the electromigration resistance due to grain boundary formation of AlCr intermetallics [9]. Approximately an eightfold lifetime improvement over Al-4% Cu has been observed [10].

The use of the complex laminate of Cr cermet and AlCu would complicate any subtractive or etching process for

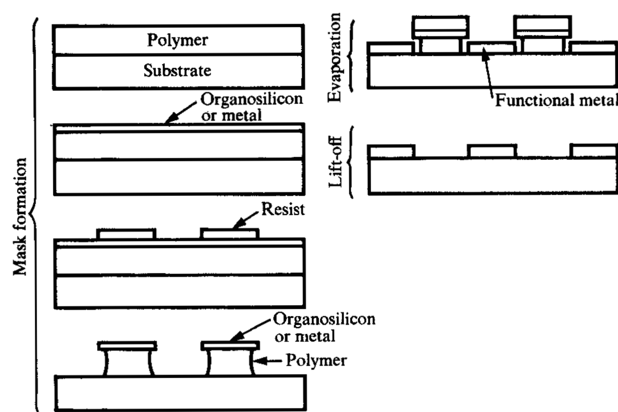

Figure 3 Lift-off sequence for bipolar VLSI circuits.

forming the wiring patterns. However, the use of a high temperature lift-off stencil for the additive formation of the first level patterns makes use of a composite metallurgy relatively simple.

E-beam lithography

The key to "personalizing" (forming conductor patterns) on large numbers of custom logic chips with a multi-level metal technology is an electron beam exposure system. Three such electron lithography (EL-1) systems [11, 12] are currently used by IBM in manufacturing to personalize the first three layers (two metal levels and the interposed SiO_2 via layer) of bipolar random logic chips [13]. These systems have been successfully used in a manufacturing environment since 1974. They provide reduced turnaround time and improved defect densities over optically exposed equivalents because of glass mask elimination. They also provide excellent resolution and overlay. In addition, the EL-1 systems have proved to be highly reliable [14].

Data describing each part number are provided from an automated design system. This system also generates printed logic diagrams and all data needed for functional testing of chips and modules, as well as the matching substrate patterns for packaging. Device part number data are post-processed to provide the numerical control data to drive either the artwork generators for 10× mask segments for optical masks or for the EL-1 systems which write the patterns directly on wafers. These data are released on tape and transferred to IBM 3330 disk files. Each pattern contains up to 250K bytes of information, and 1500 patterns are stored on a disk. Currently there are more than 9000 patterns (3000 part numbers) in a shared file equally accessible to all three user systems.

An additional advantage of the electron beam system is that each chip on a wafer can be a different part number, thereby facilitating management of an open part number set. In practice, however, only one to seven part numbers are written per wafer. Also written by e-beam are test sites, fiducials, etch end point detect sites, and e-beam alignment marks.

The lithographic films and processes used in conjunction with the EL-1 systems have evolved greatly over the past six years, from a poly (methylmethacrylate) resist process [15] to a poly (methylmethacrylate-methacrylicacid) copolymer to the presently used poly (methylmethacrylate-methacrylicacid-methacrylicacidanhydride) terpolymer. Problems such as adhesion, resist cracking during developing, low solubility ratios, and redeposition of the unexposed terpolymer gel layer were encountered and solved.

The PMMA process requires the least critical process controls; however, it requires an exposure dosage of 2×10^{-5} coulombs/cm^2. This degraded the EL-1 throughput and also resulted in charging problems because the maximum EL-1 exposure dosage is only 1×10^{-5} coulombs/cm^2; therefore two exposure passes were required per chip. Unfortunately, the charge from the first exposure deflected the beam during the second pass. Corrective registration techniques could only partially compensate for this effect [16].

The P (MMA-MA) copolymer process, although it allows a reduced exposure dose, had a significant disadvantage: A chemical conversion of the imaging resist system took place during pre-exposure baking, thus requiring extremely tight control of the prebaking temperature and time (±0.25°C, ±1 min) in order to maintain a reproducible solubility ratio of the resist.

The presently used P (MMA-MA-MAA) terpolymer system has proved to be a reliable manufacturing process, resulting in defect densities of less than one defect per cm^2. There are, however, several critical process steps requiring tight control. Stress induced cracking of the imaging layer and the formation of a potentially detrimental gel layer on the surface of the imaging layer are controlled both by maintaining a careful balance between developer composition and temperature [17] and by the use of an oxygen plasma treatment prior to development. Trace amounts of metal in the developer require careful control to maintain a reproducible solubility ratio of the resist and to control the image size. Since development is taking place above the gel temperature of the developer/resist system, an additional measure is used subsequent to development, rinsing in a solvent/nonsolvent, which has suppressed displacement of the unexposed resist penetrated by the developer.

Future e-beam exposure work is directed towards variable spot-shaped systems [18, 19] which provide greater through-

put, better resolution and overlay, as well as new e-beam resists with increased exposure sensitivity and resistance to reactive ion etching.

Lift-off process for metal wiring

The industry standard for shaping metal interconnection patterns has been wet etching, a subtractive process. This isotropic technique will not suffice in the VLSI era since it imposes severe limitations on metal line and space dimensions (resolution).

High density wiring can also be achieved by anisotropic dry etching of aluminum in plasma containing halogen species [20, 21]. However, difficulties with this dry etching process still remain, including the tendency to attack underlying substrate materials and Al corrosion problems.

Various additive or lift-off techniques [22–24] have offered significant resolution improvements compared to wet etching without suffering from the non-selectiveness of dry aluminum etching. Most, however, have drawbacks; for example, they cannot withstand higher substrate temperatures and cannot withstand ion etching, which reduces their versatility in bipolar device fabrication.

A successful metal patterning process for bipolar VLSI technology must deal with demanding fabrication requirements while retaining its high resolution capability. The current lift-off process [25–27] developed for IBM's bipolar VLSI circuits forms a stencil that

- Withstands elevated metal deposition temperatures to ensure good adhesion and appropriate grain structure,
- Permits deposition of composite metal films including some high-stress layers,
- Provides sputter cleaning or ion milling capability of via holes to ensure low interface resistance between levels of metal,
- Can be formed by either electron or optical exposure,
- Accommodates multilevel device topography, and
- Allows exposure of first level metal lines through the via holes without subsequent attack.

The stencil process is shown schematically in Fig. 3 and is carried out as follows:

Stencil fabrication begins with the spin application of a thin polysulfone release layer and a polymer, typically ®AZ-1350-type photoresist [28], of a thickness which exceeds that of the eventual metal conductor. The composite is baked in N_2 ambient at a temperature above 200°C in order to make it thermally stable at elevated metallization temperatures. The next step is the application, again by spinning, of a polysiloxane film, 200–300 nm thick. Alternatively, thin metal [29] or a different inorganic film may be substituted for polysiloxane [30].

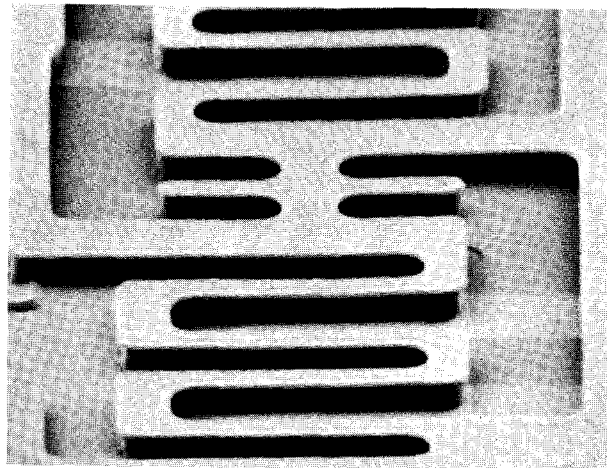

Figure 4 Scanning electron micrograph of stencil.

The imaging photo or electron resist is spun on after a baking step, again at 200°C or above. The resist is exposed, as appropriate, with uv light through an optical mask or by direct writing with a scanning electron beam, and developed. The next step, reactive ion etching (RIE), reproduces the resist pattern in the polysiloxane and the underlay polymer, thus completing the stencil. The RIE step is done sequentially in CF_4 for the polysiloxane, and then in O_2 plasma for the remainder of the composite. During oxygen etching of the underlay an overhang or ledge of the polysiloxane is created which is necessary to ensure cleanly defined metal lines. Characteristic of the process is the fact that the overhanging ledge does not begin to form until the underlay etch end point is reached; the backscattering of ions from the non-reactive substrate causes the lateral underlay etching. Consequently, resolution is little affected by film thickness; also, relatively thin imaging resist patterns can be placed on a thick underlay without resolution loss. Figure 4 is a scanning electron micrograph of the stencil. Upon completion of etching of the stencil, the wafer is cleaned and metal is evaporated. Lift-off is done by stripping the underlay and the excess metal on its surface with N-methyl pyrrolidone. This lift-off step is aided by the polysulfone release film interposed between the Si substrate and cured AZ polymer. Figure 5 is a scanning electron micrograph of a portion of the metal pattern after lift-off; the minimum spacing between lines is 2 μm, and the metal thickness is about 1 μm.

The process described above has been used to fabricate the first two levels of metallization in IBM's bipolar VLSI technology. The high resolution and versatility of the process have resulted in major performance and reliability enhancements.

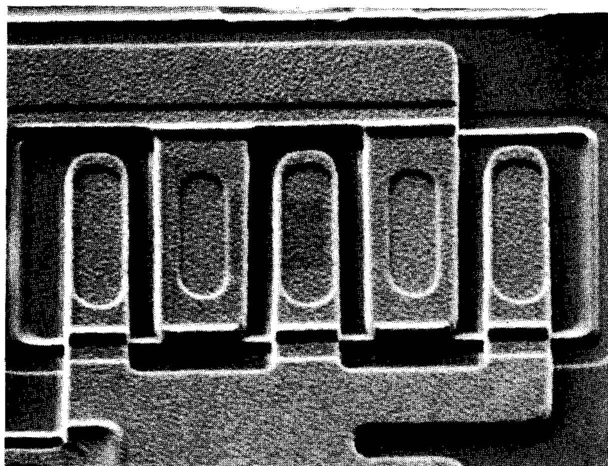

Figure 5 Scanning electron micrograph of part of metal pattern after lift-off. Minimum spacing between metal lines is 2.5 μm.

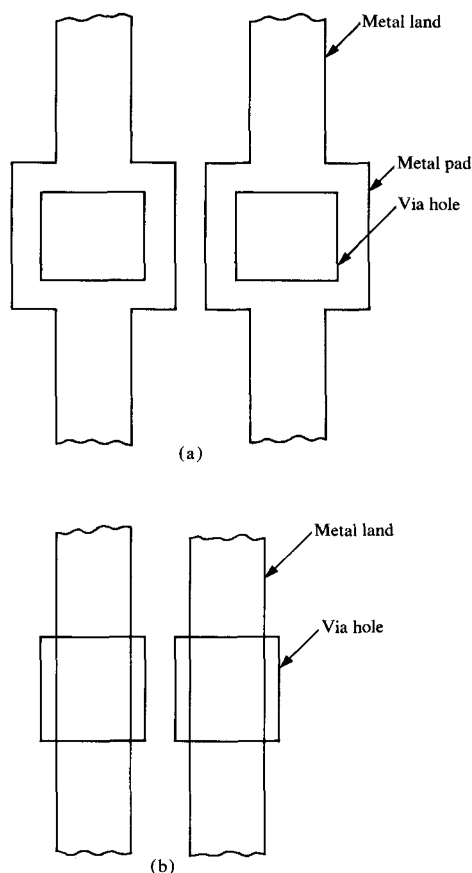

Figure 6 Conventional via hole design (a), in which first level line spacing is controlled by via pad dimensions. Zero overlap vias (b), which allow closer spacing of adjacent lines.

The third level of metallization, which has relatively coarse metal lands for power distribution buses and overflow wires, is formed by conventional techniques of blanket metal deposition and etch removal of excess metal.

Partially planar SiO_2 deposition and zero-overlap via holes

RF sputtered SiO_2 thin film is used exclusively as the interlayer insulating film among the three metallization levels of IBM's VLSI bipolar chip. The insulating layer over the first metal pattern is different from the others in that it is a partially planarized SiO_2 film, which facilitates the making of reliable "zero-overlap" via holes. The second and third levels of metal pattern are covered with less planarized, lightly biased, sputtered silicon dioxide, which conformally covers the *metal lands*. During SiO_2 sputter deposition, the negative biasing of the work causes sputter removal and redistribution of oxide on the substrate, thereby eliminating cusping or poor coverage of the oxide at the edge of the metal pattern. This reduces interlevel short circuiting and subsequent reliability problems between metal layers.

The cross section in Fig. 2 shows the profile of the SiO_2 layer over the metal patterns. Details of this latter type of conformally coated SiO_2 have been described earlier [31]. Sputtered SiO_2 has the general advantage of being deposited at a relatively low temperature (less than 400°C), yet its properties are similar to those of thermal SiO_2 [32]. An additional degree of freedom in the process is that one may control the profile of the oxide over metal patterns by varying the resputtering rate, a capability that is not typically achievable by other deposition methods. This is very useful for forming the zero-overlap via holes, a special design of via interconnection which allows space-efficient connection of two levels of wiring [33]. Conventional types of via hole structures are made in SiO_2 over metal patterns that are extended in width to form pads, so that the etched via hole is smaller than the underlying pad. In this case, the high resolution pattern density, achieved by the lift-off process, is restricted by the minimum spacing between pads. By eliminating these pads and allowing the metal pattern to be narrower than the overlying via hole, it is possible to place the underlying metal lines closer together (Fig. 6). As a consequence, reducing the center to center distance between lands by 37%, for example, results in increasing the circuit density by a factor of two.

When these types of via holes are made in conventional resputtered SiO_2, which conformally covers the metal land, it is necessary to etch the via hole all the way to the underlying Si_3N_4 coated substrate in order to completely remove the oxide on top of the metal. This leads to an undesirable condition of uncontrolled etching or tunneling along the oxide-metal interface when buffered hydrofluoric

acid is used as the etchant. Tunneling can cause reliability problems due to corrosion or interlevel short circuits. This situation is avoided by depositing partially planarized SiO_2 over narrow lands (less than 5.0 μm) using high resputtering, followed by etching the sputtered SiO_2 only about halfway down the thickness of the first level metal land. The SiO_2 deposited with high resputtering also has a much improved oxide-metal interface which resists etch tunneling. Scanning electron micrographs of this modified via hole structure (zero-overlap) are shown in Fig. 7.

A parallel plate, 13.56-MHz sputtering system is used in either of two modes to deposit partially planar oxide. In the driven substrate mode, part of the power to the target is diverted by a power splitting capacitor to the substrate electrode. A simpler alternative is the tuned substrate system, in which the bias sputtering on the substrate is controlled by a tuning circuit which is in series with the substrate electrode. In general many tuned substrate systems do not develop sufficient rf current through the substrate electrode for planar SiO_2 formation before a point of instability is reached and the rf current switches from electrode to wall. Reducing the grounded wall area can significantly increase the maximum achievable substrate bias. This is most effectively done by insulating the substrate shield from ground [34]. The high bias achievable results in resputtering sufficient to form a partially planar oxide film. The mechanism of planarization of sputtered SiO_2 over metal patterns has been described in detail [35, 36].

The slope ($\tan \phi_s$) that the glass surface assumes at a metal step for particular sputtering conditions is a function of the relative deposition and resputtering rates, which are in turn controlled by the amount of rf power or rf current at the substrate relative to cathode. Figure 8(a) shows the dependence of this angle on substrate power for the 20-inch-diameter electrode, parallel plate, driven-anode system. The inserts show the angle of the oxide over the metal land for the planar oxide (right insert) and the conventional oxide (left insert). The partial planarization of sputtered SiO_2 over narrow metal lines (less than 5 μm) results from merging of the oxide profiles at both edges of the metal land. The oxide profile over one edge of the metal land is shown in Fig. 8(b). The slope of the oxide step is only a function of the system parameters, but the peak height in the oxide over the metal land resulting from the merging edge profile is a function of the metal land width, metal thickness, and oxide thickness. For particular operating conditions (ϕ_s = 32 to 34°) the deposition of a 2.5-μm-thick oxide film over a metal land which is 1.0 μm high and 5.0 μm wide results in a peak height of approximately 350 nm (see Fig. 9). The shallow angle of the oxide step ($\approx$32°) is also beneficial for good metal edge coverage at second metal deposition, since metal lift-off at this level also requires a normal incident evaporation.

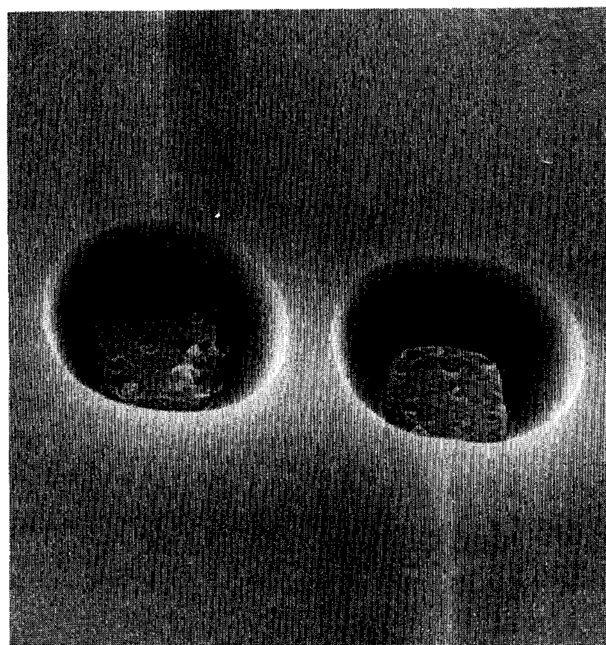

Figure 7 Adjacent via holes over metal lands (45° section, 4400×).

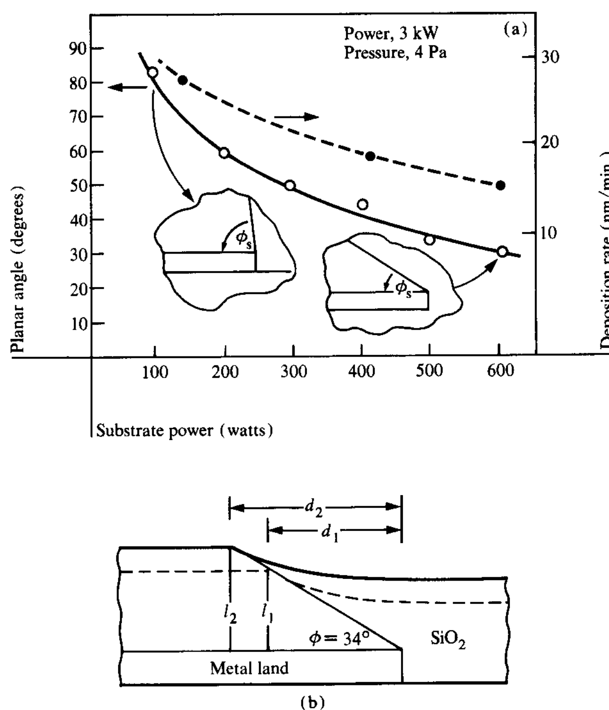

Figure 8 Dependence of planar angle on substrate power (a). Planar distance d, planar angle ϕ, and glass profile for two different oxide thicknesses, l_1 and l_2 (b).

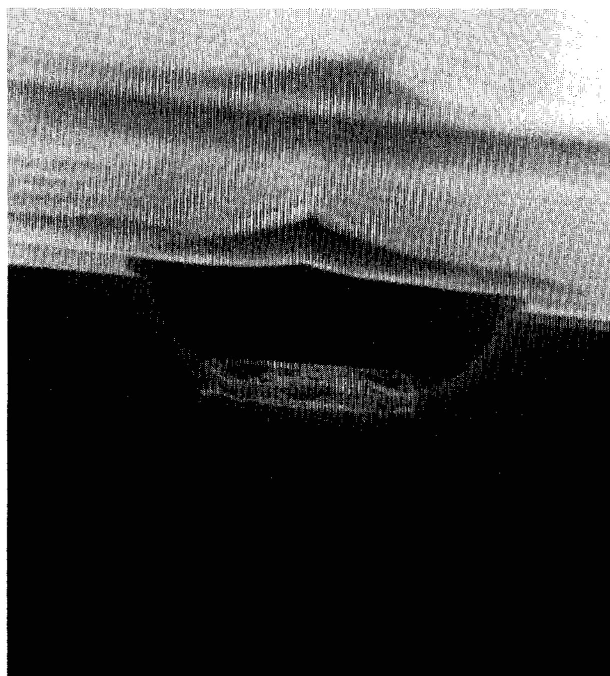

Figure 9 Cross section through via hole and metal land (90° section, 7200×).

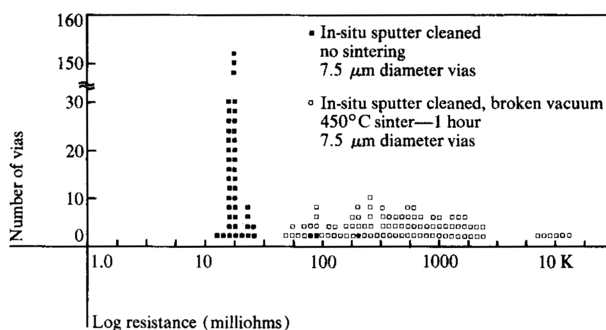

Figure 10 Kelvin probe via resistance measurement distributions of first to second level via connections.

Low resistance first to second level via connections

Making good via interconnections from one level of metallization to the next can be difficult in integrated circuit technology using aluminum conductors. Aluminum forms natural protective oxides on exposure to air. In low density integrated circuits with relatively few but large via holes the problem is solved by simply using dilute buffered HF solutions to etch a wafer just prior to depositing the next level of metallization. This results in the reformation of a thin, incomplete layer of Al_2O_3 in the hole. A post-metallization heat treatment at approximately 400°C causes Al self diffusion and recrystallization across the original metal to metal interface. The result is acceptably low interface resistances [37–38].

In VLSI, as the holes get smaller and the number of vias gets larger, the conventional precleaning procedure becomes less certain and the spread in via resistance becomes larger, to the extent of becoming marginal or unsatisfactory. For this reason a more efficient technology had to be developed to clean VLSI via holes *in situ* in the evaporator just prior to second level metal deposition.

The second metal lift-off mask is formed in the same manner as for the first metal, using the appropriate pattern. Prior to evaporation of the second metal, sputter cleaning of the first metal surface is accomplished *in situ* by applying rf voltage to the wafers in a low pressure argon atmosphere. The ionic bombardment and resultant sputter-cleaning conditions are adjusted so as to remove approximately 10 nm of aluminum or aluminum oxide. The effectiveness of this step is shown in Fig. 10, where a comparison is made of via resistance distributions with and without removal of the native oxide formed by exposure of fresh aluminum to air. The dramatic difference was observed by first sputter-cleaning a wafer in the vacuum system and then back-filling the chamber with air for several minutes, after which the chamber was evacuated and aluminum-copper evaporated. The via resistances were then compared with those for other wafers which were not exposed to air after sputter-cleaning. It can be shown that aluminum-copper oxidizes rapidly to form an oxide barrier of 1.5–2.0 nm under these conditions. Subsequent heat treatment improves the via resistance distribution if carried out at high temperatures for a sufficient length of time, but there tends always to be a "tail" to the distribution which can show up as yield loss in product. Therefore, the *in situ* sputter cleaning process [39] is used to assure high yields. *In situ* cleaning has also been accomplished by ion-milling the wafers in an appropriate evaporation apparatus [40].

Area array solder interconnections

All IBM internally fabricated silicon devices since SLT have used the "flip chip," face-down soldering method to attach passivated Si devices to thick film substrates. Initially, for the discrete transistors or diodes of SLT, copper ball standoffs were used to keep the unpassivated silicon edges of the chips from shorting to solder coated, thick film lands. Later, in the integrated circuit era, the controlled collapse chip connection (C-4) was devised, wherein a pure solder bump was restrained from collapsing or wetting out on the land by a simple glass dam which limited solder flow to the tip of the substrate metallization [7, 41, 42].

Various advantages were soon realized for C-4 connections. One example is the self-alignment capability during reflow joining. A chip which is slightly misregistered relative to the correct substrate lands will rotate and translate during solder reflow to adjust its position and self-align, a distinct reliability and manufacturing advantage. An additional benefit is the ability to make thousands of joints simultaneously in a solder reflow furnace, as opposed to most serial I/O connection techniques.

On the other hand there were also constraints and limitations in the use of C-4. One was the typical design of peripheral connections at the edges of the chip with occasional use of a staggered row of pads or a power pad inside the perimeter. This constraint was originally dictated by the practical inability to screen thick film lines and spaces on a substrate closer than 125-μm (5-mil) lines on 250-μm (10-mil) centers. Metallized ceramic technology relieved this limitation somewhat by permitting the etching of narrower lines and spaces in evaporated Cr-Cu-Cr metallization [75-μm (3-mil) lines on 150-μm (6-mil) centers and finer]. An immediate consequence was the ability to use more inboard I/O pad positions; however, a totally close-packed grid still could not be used because some space was needed between connections for the escape of wiring channels. The result was a depopulated array on logic chips of the type announced for the IBM System 38 [43]. The full array of I/O connections in a fully populated grid would have to await the more sophisticated MLC substrate in which wiring channels would be buried below the top surface [3, 44].

A second constraint has been heat dissipation. Since the chip thermal path is primarily through metal lands and via hole constrictions in glassy films, to solder joints, alumina, and beyond, the heat distribution has normally been limited to approximately 0.5 watt for a 12.5-mm-square ceramic package and 2.0 watts in a 25-mm package. The upper limit is, of course, dependent on the thermal cross section or the number of C-4 joints present.

Another constraint demanding engineering care was the maximum chip size. Due to a thermal cycling fatigue mechanism in the solder, which the outermost C-4 pads experience because of a thermal expansion mismatch between Al_2O_3 and Si (6×10^{-6} *vs* 2.8×10^{-6}), the chip size is constrained. Conservative design has forced a small enough distance to neutral point (DNP) for the most highly stressed corner pad to avoid the possibility of field failure by thermal cycling solder fatigue [45].

The combination of multilayer thin film wiring on the chip and multilayer thick film wiring in the MLC substrate and back side piston contact to remove heat directly from the Si [46] has markedly improved the capability of C-4 as a high density interconnection for VLSI.

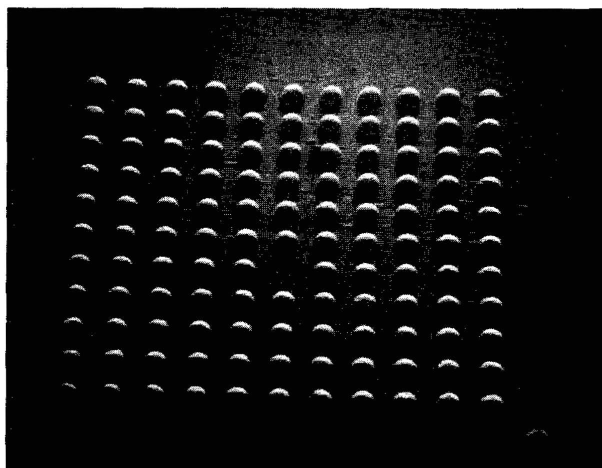

Figure 11 Area array of C-4 terminals on VLSI chip.

Three levels of aluminum wiring on the chip greatly improve the wireability of the chip (*i.e.*, the integrated silicon devices can form more circuits per unit area). Actually, only a small area of single level silicon chip is occupied by active and passive Si devices; most of the silicon chip area is occupied by aluminum thin film connections and bonding pads. As the number of levels of wiring increases, wiring which had been at a lower level is moved upward, and terminal pads are placed over wiring. Therefore, the chip becomes much more efficient in Si area utilization. One consequence of such "densification" is more chips per wafer; alternately, the efficiency can be used to get more VLSI circuitry on a larger chip. In the 3081 machine, approximately 700 logic circuits are accommodated on a chip which is approximately 4.25 by 4.25 mm square.

The I/O count on the chip has been raised to 120 C-4 terminals in a square grid array, which is 11 C-4 connections long by 11 C-4 connections wide on 250-μm (10-mil) centers. A solder bump is located at every intersection in the grid except one, which is displaced for orientation purposes (Fig. 11). Simple, single level, thick film substrate wiring would not be able to accommodate such a dense array of I/O pads. However, the buried redistribution lines in the uppermost five levels of wiring on the MLC substrate make the grid connectable to the wiring lower in the substrate (Fig. 12).

The dense and efficient grid of I/O pads also keeps the outermost pad close to the neutral point of the array; therefore, the concern about thermal cycle fatigue of solder is greatly reduced.

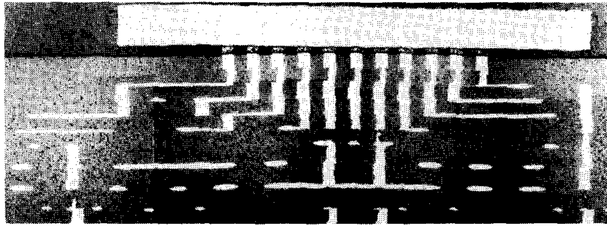

Figure 12 Cross section of MLC, C-4 area array solder connections, and silicon chip.

Finally, the TCM design of the module with individual metal pistons touching the back of each chip to lead heat directly away greatly improved the thermal capability of a dense logic chip. Three watts per chip are easily dissipated by the combination of the back side contact with a spherically tipped piston and the high thermal conductivity helium atmosphere in the enclosure.

In conclusion, the combination of multilayer chip wiring and multilayer substrate wiring has allowed C-4 connections to be used to full advantage in the format of the area array of I/O connections. When used with piston back side cooling, the total integrated VLSI packaging system becomes both efficient and extendable.

Summary

A total design for three-level metallization and supportive input/output solder connections for an advanced bipolar chip has been described. Numerous process and design changes were required to achieve the desired result. The process has been reduced to practice and is at a high level of production to make the necessary quantities of integrated circuits for IBM's most advanced computers.

A trend has begun in VLSI design to force more of the wiring at higher levels of packaging to the chip level to achieve lower cost, greater reliability, and higher performance. We expect the continuing improvement of the multilevel wiring capability (*i.e.*, process simplification, defect reduction) to become an important factor in the densification trend for tomorrow's VLSI electronic devices.

Despite what has been achieved, chip wiring still lags behind the densification of integrated silicon devices by a large factor. There is much need for further innovation and simplification of the multilevel chip wiring system if the full potential of VLSI is to be realized.

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References and note

1. B. T. Clark, "Design of the IBM Thermal Conduction Module," *IEEE Trans. Components, Hybrids, Manuf. Technol.* **CHMT-4** (1981).
2. A. J. Blodgett and D. R. Barbour, "Thermal Conduction Module: A High-Performance Multilayer Ceramic Package," *IBM J. Res. Develop.* **26,** 30 (1982).
3. A. J. Blodgett, Jr., "A Multilayer Ceramic Multichip Module," *IEEE Trans. Components, Hybrids, Manuf. Technol.* **CHMT-3,** 634 (1980).
4. D. J. Bendz, R. W. Gedney, and J. Racile, "Cost/Performance Single Chip Module," *IBM J. Res. Develop.* **26,** 278 (1982, this issue).
5. A. H. Dansky, "Bipolar Circuit Design for a 5000-Circuit VLSI Gate Array," *IBM J. Res. Develop.* **25,** 116 (1981).
6. T. M. Reith and J. D. Schick, "The Electrical Effect on Schottky Barrier Diodes of Si Crystallization from Al/Si Metal Films," *Appl. Phys. Lett.* **25,** 524 (1974).
7. P. A. Totta and R. P. Sopher, "SLT Device Metallurgy and its Monolithic Extension," *IBM J. Res. Develop.* **13,** 226 (1969).
8. I. Ames, F. M. d'Heurle, and R. E. Horstmann, "Reduction of Electromigration in Aluminum Films by Copper Doping," *IBM J. Res. Develop.* **14,** 461 (1970).
9. P. S. Ho, J. K. Howard, and J. F. White, "Intermetallic Compounds of Al and Transition Metals: Effect of Electromigration in 1–2 μm-wide Lines," *J. Appl. Phys.* **49,** 4083 (1978).
10. J. S. Jaspal and H. M. Dalal, "A Threefold Increase in Current Carrying Capability of AlCu Metallurgy by Predepositing a Suitable Underlay Material," *19th Annual Proceedings of Reliability Physics*, 1981, p. 238.
11. H. S. Yourke and E. V. Weber, "A High-Throughput Scanning-Electron-Beam Lithography System, EL1, for Semiconductor Manufacture: General Description," *IEDM Tech. Digest,* 431 (1976).
12. J. L. Mauer, H. C. Pfeiffer, and W. Stickel, "Electron Optics of the Electron-beam Lithography System, EL1," *IEDM Tech. Digest,* 434 (1976).
13. James R. Kitcher, "Application of Electron Beam Fabrication to Multilevel Metal Structures," *J. Vac. Sci. Technol.* **16,** 2030 (1979).
14. R. D. Moore, "Reliability, Availability, and Serviceability of Direct Wafer Exposure to e-beam Systems," *Proceedings International Conference on Microlithography,* Paris, Sociétè des Électriciens des Électronics et des Radio Électriciens (SCE), 1977, p. 153.
15. M. Hatzakis, "PMMA Copolymers as High Sensitivity Electron Resists," *J. Vac. Sci. Technol.* **16,** 1984 (1979).
16. D. E. Davis, R. D. Moore, M. C. Williams, and O. C. Woodard, "Automatic Registration in the Electron-Beam Exposure System, EL-1," *IEDM Tech. Digest,* 440 (1976).
17. Charles A. Cortellino, "Resist Mask Formation Process," U. S. Patent 3,987,215, October 19, 1976.
18. E. V. Weber and R. D. Moore, "Variable Spot-Shaped E-Beam Lithographic Tool," *J. Vac. Sci. Technol.* **16,** 1780 (1979).
19. E. V. Weber and R. D. Moore, "E-Beam Exposure for Semiconductor Device Lithography," *Solid State Technol.* **22,** 61 (1979).
20. N. Hosokawa, R. Matsuzaki, and T. Asamaki, "RF Sputter-Etching by Fluoro-Chloro-Hydrocarbon Gases," *Proc 6th International Vacuum Congr. 1974 (Japan J. Appl. Phys.,* Suppl. 2, Pt. 1, 1974), p. 435.
21. P. M. Schaible, W. C. Metzger, and J. P. Anderson, "Reactive Ion Etching of Aluminum and Aluminum Alloys in an RF Plasma Containing Halogen Species," *J. Vac. Sci. Technol.* **15,** 334 (1978).

22. M. Hatzakis, "Electron Resists for Microcircuit and Mask Production," *J. Electrochem. Soc.* **116,** 1033 (1969).
23. B. C. Feng, R. H. Flachbart, L. J. Fried, and H. A. Levine, "Lift-Off Method of Fabricating Thin Films and A Structure Utilizable as A Lift-Off Mask," U. S. Patent 3,982,943, Sept. 28, 1976.
24. B. J. Canavello, M. Hatzakis, and J. M. Shaw, "Process for Obtaining Undercutting of a Photoresist to Facilitate Liftoff," *IBM Tech. Disclosure Bull.* **19,** 4048 (1977).
25. J. Havas, "High Resolution, High Temperature Lift-Off Technique," *Electrochemical Society Fall Meeting, Extended Abstracts, 76-2,* 1976, p. 743.
26. J. R. Franco, J. Havas, and H. A. Levine, "Method of Depositing Thin Film Utilizing a Lift-Off Mask," U. S. Patent 3,873,361, March 25, 1975.
27. M. Hatzakis, B. J. Canavello, and J. M. Shaw, "Single-Step Optical Lift-Off Process," *IBM J. Res. Develop.* **24,** 452 (1980).
28. Produced by the Shipley Co., Newton, MA. ®AZ is a trademark of the Azoplate Division of American Hoechst Corporation, Somerville, NJ 08876.
29. J. R. Franco, J. Havas, and L. J. Rompala, "Method for Forming Patterned Films Utilizing a Transparent Lift-Off Mask," U. S. Patent 4,004,044, January 18, 1977.
30. P. Carr, J. Havas, G. Paal, and L. J. Rompala, "Stripping Promotor for Lift-Off Mask," *IBM Tech. Disclosure Bull.* **19,** 1226 (1976).
31. J. S. Logan, "Control of RF Sputtered Film Properties Through Substrate Tuning," *IBM J. Res. Develop.* **14,** 172 (1970).
32. W. A. Pliskin, "Comparison of Properties of Dielectric Films Deposited by Various Methods," *J. Vac. Sci. Technol.* **14,** 1064 (1977).
33. J. S. Lechaton, L. P. Richard, and D. C. Smith, "Partial Planarization of Electrically Insulative Films by Resputtering," U. S. Patent 3,804,738, April 16, 1974. "Integrated Circuit Structure, Accommodating Via Holes," U. S. Patent 3,868,723, February 25, 1975.
34. J. S. Lechaton and J. A. Bialko, "RF Sputtering Apparatus Having Floating Anode Shield," U. S. Patent 4,131,533, December 26, 1978.
35. P. D. Townsend, J. C. Kelly, and N. E. W. Hartley, *Ion Implantation, Sputtering and their Applications,* Academic Press, Inc., New York, 1976, p. 111.
36. C. Y. Ting, V. J. Vivaldi, and H. G. Schaefer, "Study of Planarized Sputter-Deposited SiO_2," *J. Vac. Sci. Technol.* **15,** 1105 (1978).
37. P. A. Totta and J. F. White, "Thin Film Interconnections of Etched Holes in Glass Films," *Fall Meeting of ECS, Extended Abstracts,* Abstract 190, 501 (1969).
38. G. McNeil, Symposium on Ohmic Contacts, Electrochemical Society, Montreal, 1968.
39. H. Bauer, "In-situ Sputter Cleaning of Contacts for Multilayer Chip Metallization," *Proceedings of Eighth International Vacuum Congress* **1** (Cannes, France, Sept. 22–26, 1980), p. 649.
40. S. I. Petvai, R. H. Schnitzel, and R. Frank, "Cleaning of Vias by Ion Milling," *Thin Solid Films* **53,** 111 (1978).
41. P. A. Totta, "Flip Chip Solder Terminals," *Proceedings of 21st Electronics Components Conference,* Washington, DC, 1971, p. 275.
42. L. F. Miller, "Controlled Collapse Reflow Chip Joining," *IBM J. Res. Develop.* **13,** 239 (1969).
43. A. Durniak, "System/38 Shows how IBM Aims to Keep Up with the Times," *Electronics* **52,** 102 (March 15, 1979).
44. B. T. Clark and Y. M. Hill, "IBM Multichip Multilayer Ceramic Modules for LSI Chips—Designed for Performance and Density," *IEEE Trans. Components, Hybrids, Manuf. Technol.* **CHMT-3,** 89 (1980).
45. K. C. Norris and A. H. Landzberg, "Reliability of Controlled Collapse Interconnections," *IBM J. Res. Develop.* **13,** 266 (1969).
46. R. C. Chu, U. P. Hwang, and R. E. Simons, "Conduction Cooling for an LSI Package: A One-Dimensional Approach," *IBM J. Res. Develop.* **26,** 45 (1982).

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