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High-Density Board Fabrication Techniques

A variety of construction methods can be used to form high-density printed-circuit boards. The electrical and mechanical requirements of a design strongly influence the choice of processes used to produce the finished product. The introduction of physically large high-density boards required the development of many new processes, several of which are critical to the electrical performance of the composite. In this paper the process sequence employed in the fabrication of the 3081 high-density board is described, with particular emphasis on the selection of the critical processes used in its manufacture. The 3081 registration system is also discussed, and a new method for merging through-hole location data with the data representing the location of the conducting layers is presented.

Introduction

Advanced computer systems are dependent upon very high-density circuit boards having a large number of internal planes, many conducting circuit lines, and a multitude of drilled holes in close proximity to the internal conductors. The need for very large circuit boards is caused by the increasing density of circuits packaged on semiconductor devices and modules, and has been previously discussed by Seraphim [1]. For very large modules of the type described by Blodgett and Barbour [2], one must consider the fabrication of large high-density printed-circuit boards as discussed by Seraphim [3].

In circuit packaging technology, the term *first-level package* refers to the container that houses the active semiconductor devices and is normally attached to an assembly, referred to as a *second-level package*. The second-level package provides communication channels among the various first-level packages, supplies them with power, and provides communication to external data processing equipment. Two types of second-level packages are currently in widespread use: the *card-on-board* package and the *planar* package. In the card-on-board package [4, 5], cards are used for mounting of the semiconductor devices and for providing local signal interconnections and power distribution. The card is then attached to a board (backpanel) containing most of the signal paths and the primary power distribution

sources. The planar package eliminates the card portion of the second-level package and permits all of the first-level packages to be interconnected and powered by the board. The high-density board discussed in this paper is an example of a planar package. As the level of device integration increases, improvements in system performance, cost, and reliability can be achieved with the planar second-level package design.

A cross section of the 3081 board is shown in Fig. 1. The external dimensions are $600 \times 700 \times 4.59$ mm thick. It contains 12 internal power planes, 6 internal signal planes, and 2 external planes, totaling 20 conducting layers in all. This board is larger and more complex than any multilayer printed-circuit board previously attempted at IBM.

The development of a large printed-circuit board requires an intimate knowledge of manufacturing processes. In the discussion that follows, an attempt is made to detail some of the processes used in the construction, to give some insight into why certain processes are chosen, and to show how certain critical process parameters influence the fabrication of a high-density board.

Of prime importance is the registration system used to maintain dimensional tolerances on the board during fabri-

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cation. The location of the drilled holes and the location of the internal and external conducting planes must be measured and controlled so that holes do not cause shorts or near-shorts which may later fail in service.

A new method of computerized merging of the drilled hole location data with the locations of the various conducting layers has been developed, allowing precise control of the dielectric spacing between a drilled hole and a conductor. Computer programs have been generated to allow boards to be accepted or rejected on the basis of dielectric clearance rather than absolute location. This data-merge technique has allowed yields due to registration to be in excess of 95 percent.

The electrical requirements of a high-density board dictate the geometric configuration of both the signal lines and the dielectric spacings. In addition, interconnections between the various conducting layers are required to improve wiring density and to provide external access to the internal wiring.

In this paper we first describe in some detail the methods used to register the various components utilized to fabricate a high-density board. Then we discuss the critical board fabrication processes, showing how the selection of the signal-line-circuitization process relates to the electrical performance of the board. We then describe the various copper-plating processes used in the formation of the interconnecting via holes. This is followed by a discussion of the manufacturing techniques used to construct the board; finally, we describe the board registration system and show how drilled hole location data and conductor location data are merged together to ensure that the minimum dielectric spacings required for board reliability are maintained.

High-density board construction considerations

A high-density board contains a large number of internal planes which provide the circuit paths and the power distribution system, as well as a large number of internal and external conductive holes to provide for the interconnection of signal planes and to serve as the conductor paths for signal and power to the first-level packages. The high-density board is also typically large in physical size, since it contains many internal planes and serves to interconnect multiple first-level packages having a large number of I/O pins.

The method of construction of a high-density board, which typically uses epoxy-glass as the dielectric media, is frequently segregated according to the process steps used in lamination. In one common approach, known as the *pin-parallel method*, the individual components of the composite (power cores, signal cores) are fabricated independently and then merged at the composite lamination step. The compos-

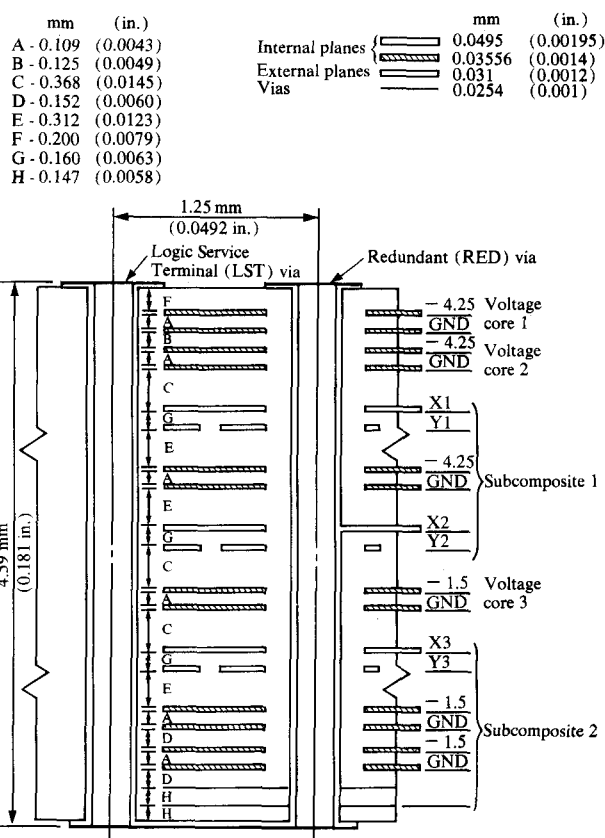


Figure 1 Cross section of the 3081 printed-circuit board.

ite lamination process must include some method for registering the internal cores with respect to each other and to the external surface of the board. Typical registration schemes employ precisely located holes on each core which have been previously used to locate the conductor pattern printed on the core. The individual cores are then "pinned" together at the composite lamination process with pins mounted on a plate in precise location, thereby aligning internal planes and also providing holes for subsequent external registration requirements (pin lamination).

A second method used in the manufacture of multilayer composite boards is known as the *sequential method*. In this approach, the starting point is usually a centrally located core which serves as the basic building block. The basic core (power core for stability) is first photoprocessed (*i.e.*, passed through a process which, through photoimaging and plating or etching, effects transfer of an artwork pattern to a conductor pattern on the part) and then subjected to several lamination and additional photoprocessing steps which sequentially add the copper circuits to the basic building block. A typical composite is made by starting with a

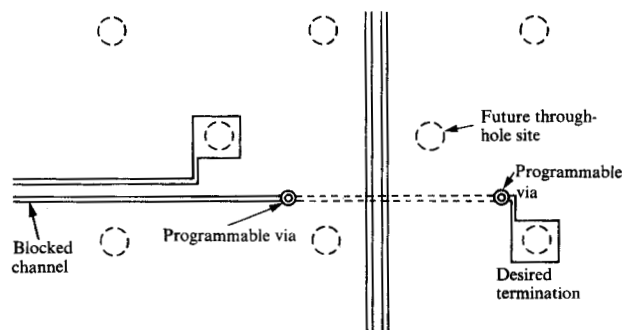


Figure 2 Illustration of programmable via concept.

finished power plane pair as the base unit, and then processing through a lamination step during which dielectric and copper foil are added to the external surfaces. The external copper is then photoprocessed to obtain a suitable signal pattern. This unit, now containing two power planes and two signal planes, can again be subjected to the lamination process, whereby another layer of dielectric and copper foil is added. After fabrication of all of the internal planes by this technique, the subcomposite is once again returned to the lamination process and made ready for hole drilling and external composite circuitization. As in the pin-parallel case, provision must be made for registering each successive layer to the internal planes. This is accomplished by pin lamination and by registering each patterned plane to the holes formed by the pins.

A third method uses a combination of both pin-parallel and sequential techniques. The advantage of this *hybrid construction technique* is that several subcomposites may be manufactured and tested independently before they are laminated together as a composite. This allows for faster manufacturing times than does the full sequential method and results in improved composite process yields compared to a pin-parallel approach. In the hybrid process, the signal planes are manufactured using sequential processing techniques. A photoprocessed power core containing two power planes is laminated into a power laminate by adding dielectric and copper foil to the base core. Signal patterns are then photoprocessed on each side of the power laminate and the subassembly is relaminated with additional dielectric and copper foil. The relaminated subcomposite can be drilled to a limited depth to fabricate connections between adjacent signal planes and then photoprocessed to produce the external signal patterns together with the plated interconnections between adjacent signal layers. These interconnections are called *interstitial vias*. The subcomposite thus fabricated contains a pair of via-interconnected signal planes on either side of the base core of two or more power planes. The multilayer composite is formed by pin-laminating two or

more subcomposites together along with an appropriate number of additional power cores. The laminate composite, which typically contains three or four pairs of signal planes and five or six power plane pairs, is drilled with through-holes which expose the internal signal and power connections. The drilled composite is photoprocessed and plated to provide access points for signal and power connections on the outside surface of the structure. [See Figs. 1 and 6 (shown later).]

The relationship between characteristic impedance, signal line width, and dielectric spacing requires that narrow line widths be used to minimize the board thickness. The minimum usable line width, however, is constrained by the electrical series resistance requirements of the board. In conventional etching technology, line widths of the order of 0.127 mm (0.005 in.) can be consistently produced in 0.035-mm (1 oz/ft²) copper, but the tolerance associated with finer lines using the conventional etching technology increases significantly as the line thickness increases. For example, a 0.127-mm (0.005-in.) line etched in copper foil 0.035 mm (0.0014 in.) thick might typically have an associated tolerance of the order of ± 0.05 mm (0.002 in.). It would be desirable to reduce the line width to improve channel wireability, but to reduce the width by 50 percent implies doubling the copper thickness in order to maintain the dc line resistance. Thus, the problem becomes one of etching a nominal 0.064-mm (0.0025-in.) circuit line in copper which has a thickness of 0.070 mm (0.0028 in.). In conventional high-volume etching operations, the condition of thickness greater than width presents a formidable tolerance problem. For additive-copper or other pattern-plating technologies, the direct dependence between line-width tolerance and plating thickness disappears. The thickness of the copper deposit is limited only by the thickness of the medium used to define the plating channel. Typically, circuit lines of the order of 0.076 mm (0.003 in.) wide by 0.05 mm (0.002 in.) thick can be routinely produced by this technology. In this case, the limits on the circuit line geometries are more a function of the properties of the material and the photoprocess used to form the line channels, rather than the ratio between line width and thickness as in the case of conventional etching technology.

Fabrication of more complex multilayer composite boards generally requires two different types of interconnections. The first type is termed an *interstitial* or *programmable via* and serves to interconnect adjacent signal planes to increase wireability. Without the *programmable via* concept illustrated in Fig. 2, wireability would be severely limited. As shown in the figure, the presence of a programmable via permits the lower circuit line to terminate at a point above the blocked wiring channel. Typical dimensions for this type of interconnection hole would be 0.125 mm (0.005 in.) to

0.25 mm (0.010 in.) in diameter, and it may be formed by a variety of methods, such as mechanical drilling, punching, or laser drilling. A variety of plating processes may be used to provide the conductive path between the two layers, and generally both the signal surface and the via hole are plated simultaneously.

The second type of interconnection is the *through-hole* connection by which signal and power connections are brought to the outside surface of the composite. Virtually all of the through-hole connections are made with high-speed mechanical drilling equipment, with hole diameters varying in size from 0.38 mm (0.015 in.) for high-density products to 1.78 mm (0.07 in.) or larger for less dense composite structures. After drilling is complete, the formed hole must be subjected to a series of processes which ensure that the internal conductors, referred to as *plated-through-hole* (PTH) lands, are sufficiently exposed so that the subsequent plating process will produce a reliable connection. In multilayer composites, the process technology involved in forming and cleaning the through-holes is usually complex due to the variety of conditions possible in any given hole. For example, a power PTH may be required to connect from one to twenty internal power planes, depending upon the internal electrical design of the composite. Similarly, a signal PTH may connect from one to ten internal lands, depending upon the complexity of the design and location of the hole. In order to maximize the wiring channel width, the diameter of the through-hole is minimized consistent with the constraints of drilled hole depth and materials used in the composite. Most of the currently used hole-cleaning processes employ mechanical abrasion, chemical solutions, plasmas, or a combination of these to remove drill debris and dielectric smeared on the inner plane connections during the drilling operation.

The plating process which forms the metallic conductor on the walls of the through-holes is dictated in part by the *aspect ratio* ($AR = \text{composite thickness/through-hole diameter}$) of the composite structure. Additive plating processes have an advantage over certain types of electrolytic plating processes in that the plating thickness inside the hole is not a function of the aspect ratio of the hole, and uniform copper deposits can be achieved with aspect ratios of the order of 12:1 or higher [6].

Critical board manufacturing processes

Because of the complexity of a high-density multilayer board, virtually all component processes are important in achieving the electrical performance and the wiring density required in a given package design. However, there are certain elements within the manufacturing sequence which are critical to the overall package reliability, performance, and cost.

Registration of the internal signal and power planes to each other and to the external planes is certainly critical and must be controlled and monitored to produce a reliable composite. Similarly, the processes which effect generation of the signal lines are of extreme importance because the line geometry, in combination with the dielectric spacings, to a large extent controls the electrical performance of the board. In addition, a reliable interconnection-producing process for both interstitial and through-hole vias is essential to achieve high wiring densities and functionality. Finally, in order to produce a board of this complexity in a manufacturing environment, it is mandatory that close process control be extended to virtually all component processes.

Primary registration is achieved by relating artwork patterns to tooling holes which have been introduced earlier into the workpiece. Artwork patterns may contain the tooling pins, or a registration fixture may be used to locate the artwork to the tooling holes in the laminate. The tooling holes are also used to pin together the individual pieces during subsequent lamination processes. In fabrication of larger boards, e.g., larger than 300 × 300 mm, the characteristic growth and shrinkage normally encountered with epoxy-glass dielectric systems can cause considerable error in the location of the internal board features after lamination. In cases where sequential lamination processes are used, the dimensional stability problem is compounded by the multiple lamination steps performed on the composite. Normally, lamination is effected by subjecting the part to a predetermined heat and pressure cycle which causes the resin in the prepreg (resin-impregnated glass fabric) to flow, bonding together all subcomposite assemblies into one composite. Since the lamination temperature is greater than that of the glass transition of the resin and the applied pressure is of the order of 1380 to 3450 kPa (200–500 psi), movement occurs in the internal signal and power planes. Therefore, not only is the system by which internal patterns are registered to the tooling holes critical, but also the methods by which internal plane movement is tracked and controlled in the manufacturing processes.

Other critical areas are the processes used to define the circuit lines and the methods used to control the dielectric spacings between circuit lines and voltage reference planes. There are several dependent parameters which ultimately determine the electrical performance of the internal signal transmission lines [7]. Characteristic impedance, series resistance, and *signal-line-to-line coupling* are three of the most important parameters and are affected by both the signal line geometry and placement and by the package dielectric spacings between signal lines and reference power planes. Triplate structures, wherein each pair of signal planes is located between two power planes, are used when control of characteristic impedance is critical. Dielectric

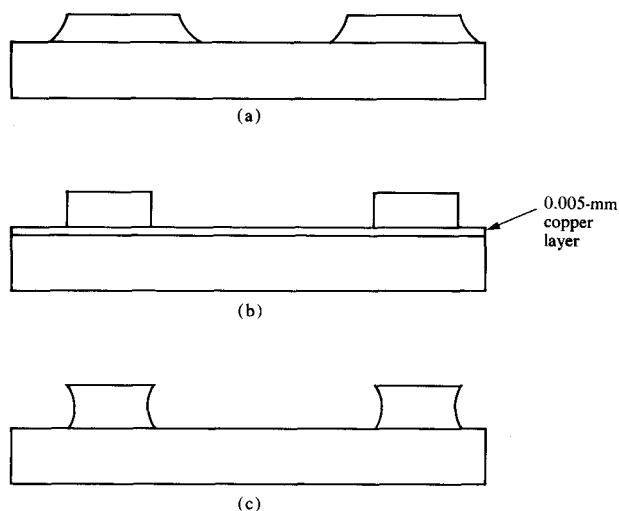


Figure 3 Typical signal line cross sections: (a) etched-circuit line, (b) additively plated lines—before etching, (c) additive line—after flash etching.

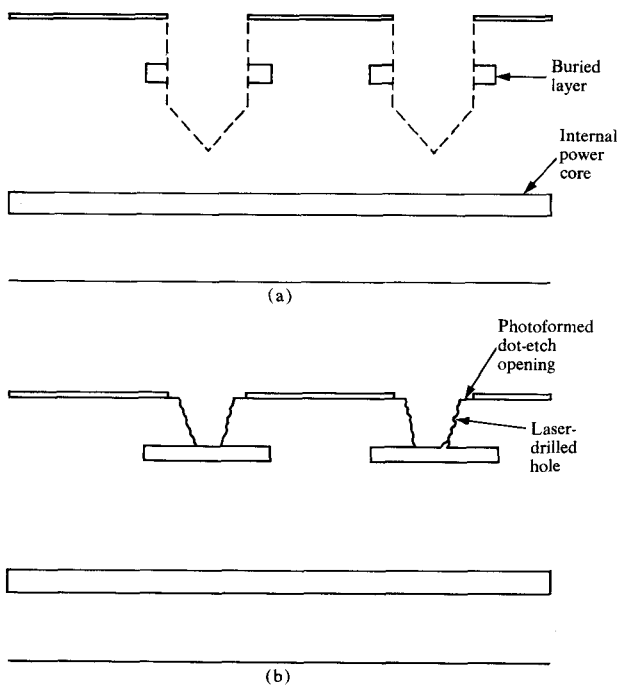


Figure 4 (a) Mechanically drilled via holes. (b) Laser-drilled via holes.

spacings are controlled by the resin and glass content of the epoxy-glass prepreg and by the lamination process used to assemble the individual components. Signal line coupling is determined by the geometry of the signal lines and their proximity to other lines, interstitial via holes, and through-holes. Series resistance is a function of the total line length, the cross-sectional area, and the resistivity of the plated

deposit. The circuit line geometry is in turn determined by the manufacturing process selected for generation. Figure 3 illustrates the effect of the various processes on the cross-sectional geometry of the signal lines. Figure 3(a) shows a typical subtractively etched circuit line with the characteristic tailing due to the etching process. The cross section of an ideal circuit line made by an additive plating process is illustrated in Fig. 3(b). In this process, the shape of the finished line is determined by the shape of the plating channel formed in the plating resist. Figure 3(c) shows the geometry of a line made by additively plating copper on a thin, previously laminated layer of copper. The side walls are straight immediately after plating, as in the case of an additively plated line. Prior to resist removal and etching, a thin layer of an etch-resistant material, such as immersion tin, may be applied to the top surface of the line to prevent line thickness erosion during the etching process. Erosion of the side wall occurs during the flash etch process, which removes the thin laminated copper and allows for circuit feature isolation. Circuit lines constructed by this technique are characterized by approximately equal widths at the top and bottom of the line but exhibit a 10–20% width reduction in the midsection.

Yet another critical process element is the method used to form and plate the interstitial and through-hole connections. Utilization of a sequential construction in forming the signal plane pairs requires the drilling, cleaning, seeding, and plating of a blind hole, *i.e.*, a hole between signal layers only and not through the entire subcomposite. The depth of a mechanically drilled hole must be precisely controlled in order to avoid plated connections to the conductor planes lying under the drilled hole. In the case of a laser-drilled hole, the buried programmable-via land acts to limit the penetration of the laser pulse. In either case, the drilled hole must be cleaned, seeded, and plated in order to ensure a reliable connection between the two signal layers. Figure 4 illustrates the differences between blind interstitial via holes formed by a mechanical drill and by a laser drill.

The final critical element in the fabrication of a high-density board is control of all manufacturing processes. This is particularly critical when one uses the sequential approach to signal plane fabrication. A pin-parallel construction approach has the inherent advantage of manufacturing each component separately and then assembling the composite in one laminating step. Sequential subcomposite manufacturing requires a longer time period because of the multiple lamination steps involved. The longer exposure to multiple processing steps requires that all processes be in control, from the time that a power core is removed from stock until all circuitization processes are completed on the subcomposite. For example, a problem with the dielectric used between a buried power core and the first signal layer would

not be detected at the completion of the subcomposite but only after that subcomposite had been laminated into a composite, drilled, plated, and electrically tested.

3081 Board construction and manufacturing processes

A cross section of the 3081 board is shown in Fig. 1. The internal signal layers contain 0.8 to 1.6 km of printed-circuit wiring smaller in cross section than a human hair. Conductive paths between adjacent signal layers are established by approximately 15 000 plated interstitial via holes 0.15 mm (0.006 in.) in diameter. Signal and power paths to the surface of the composite are formed by mechanically drilling and plating approximately 40 000 0.41-mm (0.016-in.) through-holes in the multilayer structure of epoxy-glass laminate and copper.

The dielectric used is epoxy resin reinforced with woven glass fabric. The laminate is similar to NEMA grade FR-4 commonly used in the industry for circuit boards. There are, however, some important differences. The IBM laminate utilizes a brominated epoxy based on tetrabromobisphenol A, further modified with a higher-functionality epoxy to improve heat and solvent resistance. The ratio of epoxy resin to glass is higher than that normally associated with FR-4 laminates; it was designed to achieve a lower dielectric constant at high frequencies as well as an enhanced resin flow to encapsulate dense circuitry without forming laminate voids.

The reinforcement used in all layers is Style 108 (ASTM 142) glass fabric. Woven glass is saturated with a solvent solution of the epoxy blends; the amount of resin retained is controlled by metering rolls in a conventional vertical-tower impregnator similar to that used by much of the industry.

The physical requirement of a 12:1 high-aspect-ratio plated through-hole is satisfied by the additive plating technology. The control of the copper thickness in the plated through-hole has been previously reported [6]. The additive plating technology also affords the opportunity for fabricating 0.081-mm (0.0032-in.)-wide circuit lines which are 0.05 mm (0.0019 in.) thick. Such a high-aspect-ratio line is required due to the four-ohm upper limit assigned to the dc printed-line resistance, which imposes a minimum cross-sectional area and a maximum length on any one signal line. The copper plating thickness is limited by the thickness of the photoresist used to define the circuit lines, and the top surface of the plated copper must be protected during the flash etching process in order to control circuit line thickness and width.

Selection of the board construction technique results from the dimensional instability of a thin [0.15-mm (0.006-in.)]

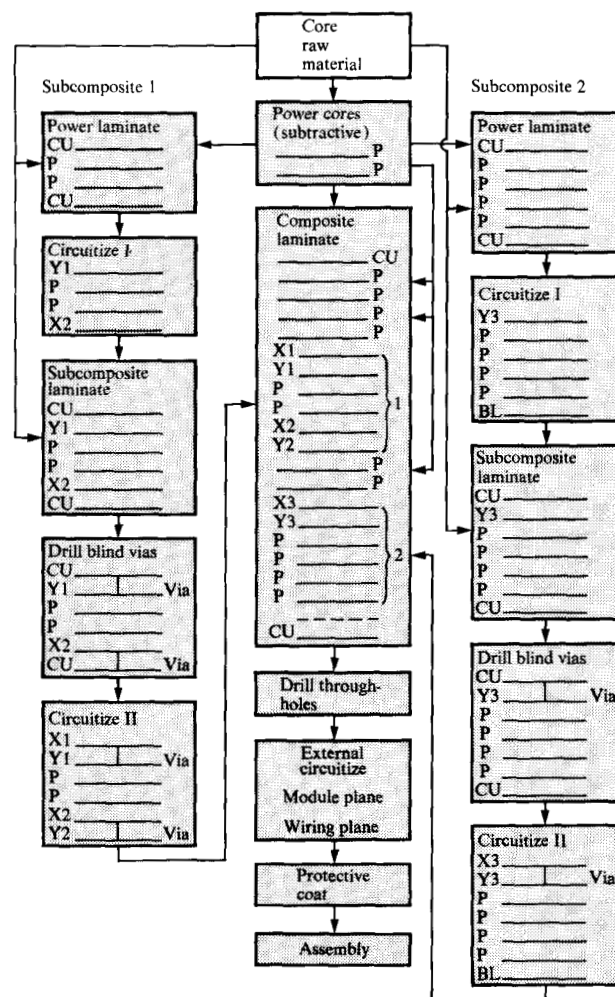


Figure 5 Process flow diagram. (Note: CU = external PAP copper, P = circuitized power plane, Xi = circuitized ith X-signal plane, Yi = circuitized ith Y-signal plane, BL = blank plane.)

signal core and the inability to process and handle a thin (610 × 710-mm) signal core in the manufacturing environment. After many early unsuccessful attempts at processing and registering thin signal cores, the sequential lamination process of fabricating signal planes was adopted. This decision affected the interstitial via hole drilling process, and subsequently a blind via hole drilling, cleaning, seeding, and plating process was developed.

The process flow diagram used to construct a 3081 board is shown in Fig. 5. Power planes used in the composite construction are manufactured in pairs by a conventional printing and etching process. Fabrication of an individual core begins with the lamination of two sheets of 0.035-mm copper foil separated by 0.109 mm (0.0043 in.) of epoxy-glass dielectric. Approximately 30 000 clearance holes rang-

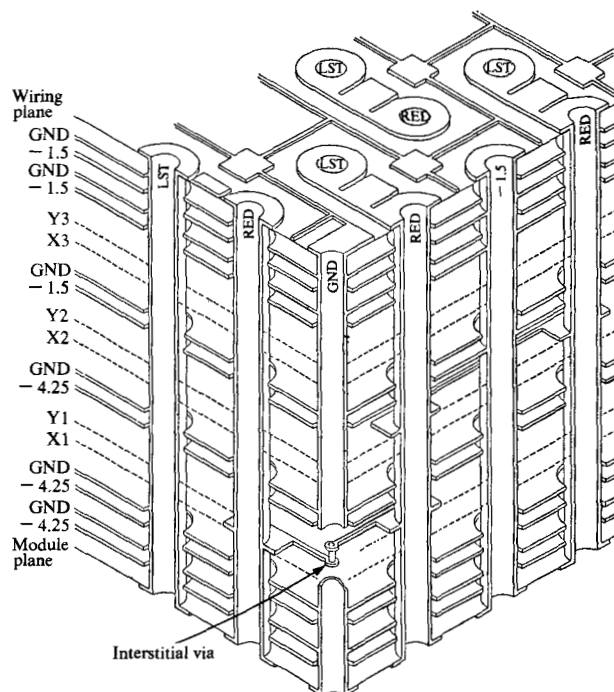


Figure 6 Composite structure of the 3081 board. (Note: LST = Logic Service Terminal via, RED = redundant via, GND = ground via, -1.5 = -1.5 V via.)

ing in size from 0.975 to 1.026 mm in diameter are etched into each copper surface by a conventional contact photo pattern printing and etching process.

All etched cores are then subjected to a noncontact test which locates residual copper projecting into the clearance-hole area. In the *hybrid sequential-pin parallel* composite construction, some of the etched power cores are used for manufacture of the subcomposite and are designated as *buried power cores*. The other power cores, designated as *free power cores*, are manufactured and stocked until the final composite lamination process.

As shown in Fig. 5, two types of subcomposites are required in the fabrication of a board. These differ in the number of buried power planes and in the number of signal plane-pairs, but each type follows an essentially identical process routing. The power laminate is made by laminating a power core with an appropriate amount of epoxy-glass dielectric and *peel-apart* (PAP) copper foil on the external surface. The primary reason for building the signal layers on a power core base lies in the fact that the power core, principally composed of copper, is dimensionally more stable, and the signal planes, containing very little copper, can thus be made more stable dimensionally by coupling them to the buried power core.

The initial step in circuitizing operations is to remove the external PAP copper foil carrier from the power laminate. PAP copper foil consists of a 0.070-mm (0.0028-in.) copper carrier to which a very thin copper layer of 0.005 mm (0.0002 in.) has been attached. One side of the thin layer of copper is loosely bonded to the carrier foil, while the other side is treated to promote adhesion to the epoxy. After lamination, removal of the carrier foil leaves behind a thin layer of copper which serves as a base for the photoprocessing and plating operations. The photoprocessing operations begin by mechanically and chemically preparing the copper surface for lamination of a vendor-supplied dry film resist. After photoforming and developing the circuit line channels, the subcomposite is subjected to an additive plating bath which deposits 0.05 mm (0.0019 in.) of copper on all exposed copper surfaces. The plated part is then immersion-tinned and the photo resist is removed from the surface. An etching operation removes the 0.005-mm (0.0002-in.)-thick background copper between the circuit lines but does not affect the upper surfaces, since they have been protected by the tin coating. After flash etching, the tin coating is removed and the two-sided circuitized laminate is ready for inspection of the Circuitize I level.

After Circuitize I operations, the subcomposite is again laminated with more epoxy-glass dielectric and PAP copper foil on the external surfaces. The PAP copper carrier is removed from the surface of the subassembly and the exposed copper surfaces are prepared for lamination of an etching resist. The part is photoprocessed to produce openings in the 0.005-mm-thick copper surface where interstitial or programmable via holes are to be formed. Formation of the via holes is accomplished with a CO₂ laser, followed by via hole cleaning prior to plating of additive copper. The etch resist is removed and the subcomposite is then re-photoprocessed in a manner identical to that previously described for the Circuitize I processes. Both interconnections between signal layers and circuit features on the surface of the subassembly are simultaneously plated in the additive copper plating bath. After completion of the remaining finishing operations, the subcomposite is now at the Circuitize II level, and signal lines can be electrically tested since all signal endpoints have been made accessible to the external surfaces. The subcomposite is then stocked after all inspections, tests, electrical characterizations, and repairs have been completed.

The composite is fabricated by laminating the 1 and 2 subcomposites together with three "free" power cores to form the structure shown in Fig. 6. After lamination and trimming, the composite is drilled and hole location measurements are made at various locations on both surfaces. The composite is then x-rayed and analyzed to assess the accuracy of the registration of the internal layers.

The x-ray data are then merged with the hole location data to determine statistically the minimum spacings between the drilled holes and the conducting planes (both power and signal) at all levels within the composite. Parts passing this merge screen are then subjected to a mechanical and chemical hole-cleaning process and a chemical seeding process which prepares the drilled hole walls for additive plating.

The circuitization process used on the composite externals is essentially the same as that used on the internal signal planes. At the completion of the through-hole seeding process, the PAP copper carrier is removed and the surface is prepared for lamination of the film plating resist. After photoprocessing operations, the composite is plated in the additive bath to a thickness of 0.036 mm (0.0014 in.) of copper in the through-holes and on the external surfaces. After the composite has been processed through the tin, resist, strip, etch, and tin-removal sequence, it is ready for inspection and electrical test.

The completed composite structure as shown in Fig. 6 is designed so that internal repairs and alterations to the internal wiring due to engineering changes can be accomplished at the composite level. All signal-carrying holes occur in pairs. One hole in the pair, termed the Logic Service Terminal (LST) hole, will eventually hold the pin which connects to the module. The other hole, termed the Redundant (RED), serves as the termination of the internal signal line. The LST and the RED are connected on the wiring surface through a specially designed pad. Repairs and engineering changes are easily made, since all that is required to effect a repair or wiring change is to sever the connection between the LST and the RED on the composite surface, thus freeing the LST and module pin from the internal wiring, and then to bond an external wire between the desired points.

The test sequence to which the finished composite is subjected is extensive. The overall purpose of all tests is to guarantee the electrical integrity of signal nets and the availability of power at the required points on the board surface. Composites are tested for signal opens, signal-to-signal shorts, signal-to-power shorts, power opens, and power-to-power shorts. All test data from both the composite and the subcomposites are analyzed at this test level, with the assistance of a specially developed, computerized analysis and repair system. All shorts, signal-to-signal, signal-to-power, and power-to-power, are removed from the boards during this phase of the board test. Repair of opens occurs at a later time during the board assembly operations.

The final operation in the fabrication of the board composite is the addition of a protective coating which also serves as a solder mask for precisely defining areas requiring

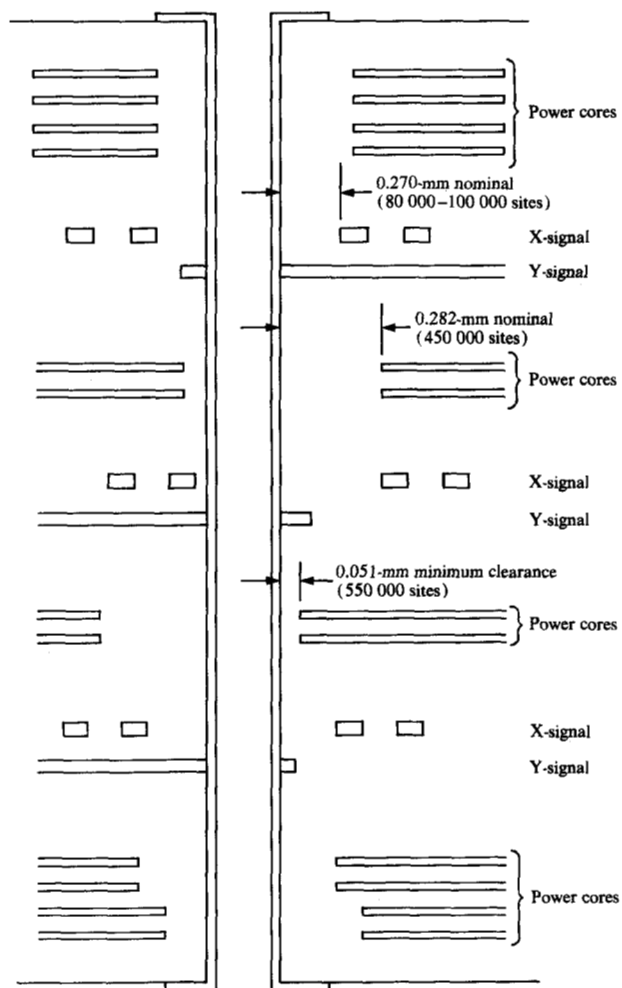


Figure 7 Section of 3081 board illustrating registration problem. The available clearances must accommodate dimensional-stability, drill-wander, drill-machine, registration-system, artwork-generation, expose-machine, hole-diameter, and pattern-etching errors.

solder on the composite surfaces. The material used in this operation was developed by IBM and is designated as PSD (photosensitive dielectric); it is capable of being coated and photoprocessed in the same way one would process a plating or etching resist. The significant difference is that PSD, once fully cured, possesses the required dielectric properties and remains as a permanent feature on the composite surface.

Registration system

The central problem of registration in a high-density multi-layer circuit board, as indicated in Fig. 7, is that of drilling holes through the various conducting layers without causing shorts or near-shorts that will later fail in service. The solution of this problem requires attention to the accuracy of the drilled holes, the stability of the dielectrics, accuracy of

Table 1 Summary of registration errors.

	3081 board experience (mm, approx.)
Drilled hole	
Machine accuracy	0.025
Drill wander	0.051
Hole diameter	0.013
Conductor size	
Etched pattern	0.038
Additive pattern	0.013
Registration system	0.013
Artwork	0.015
Lamination	
Shrinkage	0.038
Translation	0.025
Other errors	0.025
(Lamination error is for each cycle. Buried power planes experience three cycles, Circuitize I—two cycles, and free power cores and Circuitize II—one cycle.)	
Available clearance	
Signal planes	0.282
Power distribution planes	0.270

the artwork, and methods of registration. Precise control requirements are maintained by computer monitoring and computerized accept/reject decisions. The total system of improved processes and associated controls has demonstrated high yields and reliable performance over several years of pilot-line operation.

• Equipment

Locations of holes and conductor patterns are initially defined by two numerically controlled machines: the drilling machine and the artwork generator. Both rely on massive granite supports and air bearings. Basic table accuracies are better than 5 μ m, giving the precise fundamental locations necessary (see Table 1).

• Drill process

The accuracy of drilled-hole location is dependent on the performance of the drilling operation. Small-diameter drills are readily deflected and can produce holes that deviate greatly from correct location even with precise table accuracy. The error is caused largely by the drills striking glass yarns near the surface of the board. This bends the drill and starts the holes at an angle, resulting in an error at the top and a larger error at the bottom. Further bending below the surface apparently does not occur. The top deflection can be used to calculate the entrance angle by the simple beam theory equation

$$\theta = \frac{3\delta}{2L},$$

where δ = drill deflection, L = drill length, and θ = the angle of the drill tip as it penetrates the surface. The bottom error is obtained by multiplying the angle by the board thickness and adding the top error. Bottom error is then given by

$$\epsilon = \delta \left(1 + \frac{3T}{2L} \right),$$

where T is the board thickness. This was tested experimentally with a board of 3.81-mm (0.150-in.) thickness and drills of length 6.35 mm (0.250 in.), which gives $\epsilon = 1.9 \delta$ according to the previously defined equation. The experimental result was $\epsilon = 2.0 \delta$, with a correlation coefficient of 0.975, which is in excellent agreement.

The foregoing analysis indicates that the primary factor in hole location error is the bending of the drills at the surface, and that accuracy should be improved with a reduction in bending. This is obtainable by employing a shorter, stiffer drill for starting the holes and a longer one for finishing them. The initial drill location is improved because of the stiffer drill, and little additional deflection occurs when finishing with a longer drill. The standard deviation of hole location was reduced from 0.0356 mm to 0.0127 mm by starting holes with 3.175-mm (0.125-in.) drills and finishing them with 6.35-mm (0.250-in.) drills. This process has proved highly effective in yield enhancement and is used for all high-performance product.

• Lamination process

The major effect of lamination and, in fact, the largest single error in the process is a shrinkage of about 270 ppm. This occurs in the "warp" direction of the glass fabric during each lamination process. Smaller errors occur in the "fill" direction. Fortunately, this shrinkage is fairly repeatable, and compensation can be introduced in the original artworks. The net effect is to reduce maximum error from this source to about 0.076 mm (0.003 in.) after three sequential laminating steps. The basic material shrinkage is compounded by other factors that affect pattern dimensions and cause shifting of patterns. Various errors of this kind result in a total mislocation of conductor patterns of up to 0.178 mm (0.007 in.). The largest of these is a translation or overall shift relative to the registration points. The primary cause of translation is temperature nonuniformity during lamination heatup. As temperature rises, resin begins to flow and cores can expand thermally. If the temperature is low at one point, there is no flow, friction prevents motion, and expansion occurs from this cold spot. This results in deformation of the locating slots and consequent loss in registration. This error has amounted to over 0.25 mm (0.010 in.) with an out-of-control (54°C) temperature difference from one end of the press platen to the other. With proper control of temperatures, this error averages about 0.025 mm (0.001 in.).

• Moisture content

Epoxy-glass laminate absorbs and retains moisture for long periods, and the moisture can affect board size and consequently registration. The various cycles of immersion, baking, and drying are, therefore, extremely critical and must be precisely controlled. Process effects can be extremely subtle because the board dimensions at any time are the cumulative effect of all prior history. Alterations in any process step may have an impact on operations occurring much later in the process. Figure 8 indicates an initial effect of about 200 ppm after a 140°C bake. This effect is present after lamination and persists after the subsequent copper peeling and etching operations, although it is reduced by about one-half. The information of Fig. 8 was taken from one point in the process sequence, but similar phenomena apply to the entire manufacturing system. For this reason it is essential that precise repeatability be maintained in all peripheral chemical processes, even though apparently unrelated to stability.

• Mechanical surface treatment

Additional alterations in dimensions may also result from mechanical surface treatment. The effect is simply one of cold-working or compressing the surface, which results in an expansion of the assembly. The effect occurs on copper surfaces and has resulted in observed changes of over 100 ppm. Brittle materials such as epoxy-glass should not exhibit this effect and, in fact, no dimensional changes are observed unless the exterior surface is largely copper.

• Data analysis

Registration data are collected on all boards. Drilled-hole locations are measured on a jig borer, while internal conductor locations are determined via x-ray techniques. The jig borer has an inherent accuracy of ± 0.005 mm. Comparable accuracy is obtained from the x-rays by providing special dots on each conductor plane and x-raying them through a precision mask. Error is then measured by the relation between the dot and the mask pattern. Thick boards are subject to a parallax error, but this problem can be controlled by providing an X-Y table to move each x-ray site precisely beneath the source. An additional refinement includes a special x-ray site having two precisely concentric, widely spaced discs. Parallax is determined by measuring the eccentricity of these discs. This is used to set up and control the X-Y table position, and can also be applied to the data to correct errors.

Data are analyzed by least-squares fitting to a mathematical model having various parameters according to the following equations:

$$X_i = T_x + a_i S_x + b_i (\phi/2) - b_i \theta + a_i^2 \alpha_x + b_i^2 C_x + a_i b_i \lambda_x + a_i b_i^2 D_x,$$

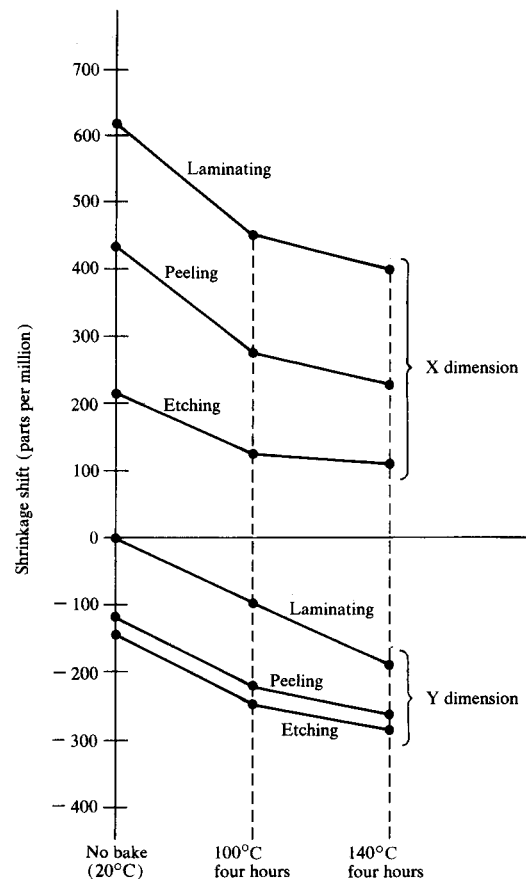


Figure 8 Effect of bake on signal plane scale factor at various process steps.

$$Y_i = T_y + b_i S_y + a_i (\phi/2) + a_i \theta + b_i^2 \alpha_y + a_i^2 C_y + a_i b_i \lambda_y + a_i^2 b_i D_y,$$

where

X_i, Y_i are the observed X and Y errors, and a_i, b_i are the coordinate positions of the data points.

The parameters represent error sources which can be present and have been incorporated into the model. Specifically,

T_x, T_y - translation,

S_x, S_y - scale,

ϕ - squareness,

θ - rotation,

α_x, α_y - asymmetry,

C_x, C_y - curvature,

λ_x, λ_y - keystone,

D_x, D_y - distortion.

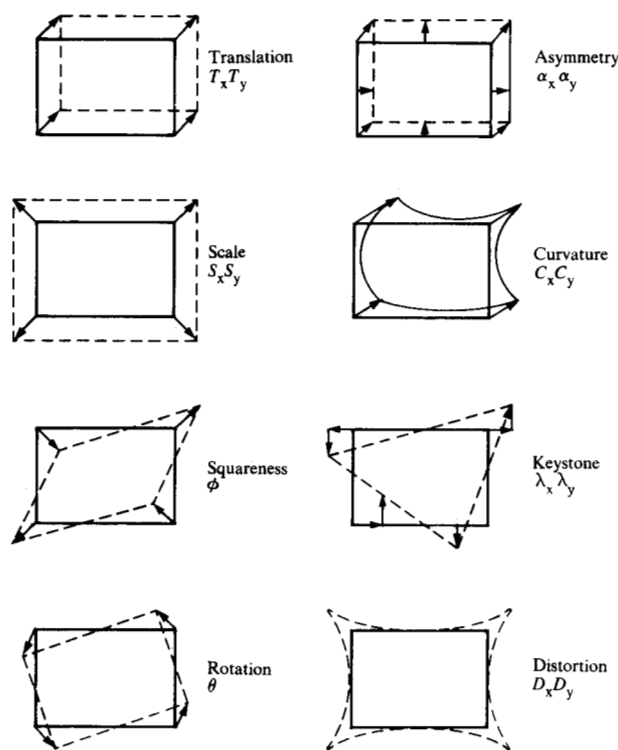


Figure 9 Graphical definition of error parameters.

Table 2 Possible causes of location errors in circuit board manufacture.

- | |
|--|
| <ul style="list-style-type: none"> Location points off Locating slots damage Slippage in lamination |
| <ul style="list-style-type: none"> Temperature Laminating shrinkage Machine ways not straight (pitch error) |
| <ul style="list-style-type: none"> Machine ways not square Lamination distortion |
| <ul style="list-style-type: none"> Process camera artwork parallelism |

These parameters are defined graphically in Fig. 9. Acceptance and rejection data of boards are determined by subtracting the model for drilled data from the model for x-ray data, thus defining a model for total misregistration. An additional variable for drill wander is defined from top

and bottom hole locations and is interpolated through the depth of the board. To this are added allowances for various wet-process variables. This variable error is then subtracted from the nominal clearance and compared against the minimum clearance.

This method of analysis was used extensively during the process development phase. Many of the parameters are generally identified with a certain type of equipment or process failure, as indicated in Table 2. Quality control charts are also run on these parameters to identify failure mechanisms before actual scrap is generated.

The registration control data have been implemented in a large time-sharing computer which provides rapid analysis capacity and flexibility. Data input is performed indirectly through two IBM 5110 computers, one on the x-ray reader and one on the jig borer. This provides direct on-line data input onto diskettes without any keyboard input. Information is transmitted periodically to the larger system for analysis. The large system is required for performing the accept/reject analysis previously described; a similar analysis would require over an hour on the smaller system. Time-sharing systems, however, generally do not have the availability necessary for on-line production, and the 5110 computers fill this need.

Summary

A circuit board manufacturing process has been developed which provides capability for many times more interconnections than were previously available. Both density and size have been increased, giving compatibility with extremely high levels of circuit integration and at the same time allowing many elements to be simultaneously connected on a single board. Precise control of characteristic impedance is provided for long transmission lengths and for high-performance circuitry. Stringent quality control and conservative specifications provide the order of reliability demanded by the immense number of risk sites.

These features result from broad advances in all manufacturing technology areas including lamination, drilling, plating, and photo-resist processing, as well as innovative analytical and quality-control techniques. The processes developed to satisfy the design requirement of the 3081 board are extendable to a wide range of board sizes and configurations.

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Received March 18, 1981; revised December 11, 1981

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