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Advanced Printed-Circuit Board Design for High-Performance Computer Applications

A new integrated circuit packaging structure was needed to support the new 90-mm multilayer ceramic modules, known as Thermal Conduction Modules (TCMs), used in the IBM 3081 computers. The structure developed eliminates one level of packaging (the card level) and allows up to nine TCMs to be plugged directly into a large multilayer printed-circuit board using a new zero-insertion-force connector system. The board has 18 internal circuit planes for signal and power distribution and accommodates new signal cabling, power bus, terminating resistors, decoupling capacitors, and cooling hardware, forming a packaged unit of up to a quarter million logic gates and half a million bits of memory. This paper focuses on the detailed design of the printed-circuit board and on its signal and power transmission characteristics.

Introduction

With the introduction of the IBM System/360 computers in 1964, an integrated circuit packaging architecture was developed having the following unique features (see Fig. 1):

1. The integrated circuit chips diced from the silicon wafers were bonded to a ceramic substrate with the circuit side down [1]. This evolved into a technology where evaporated solder pads on the chips were reflowed on the substrate to form a Controlled Collapse Chip Connection (C-4) joint [2].
2. These "flip chip" modules had screened circuits on one surface to connect the active devices (integrated circuit chips) and passive devices (trimmed resistors) to pins attached to the other side of the module.
3. The sealed module was soldered to a printed-circuit card by inserting the pins of the module into plated through-holes in the card and passing the assembly over a solder wave.
4. The printed-circuit card as a field-replaceable unit (FRU) was plugged into a printed-circuit board by compressing connector springs on the card to reformed pins soldered into plated through-holes in the board.
5. Several printed-circuit boards with their cards, signal cables to communicate between boards, and power cables to bring power to the boards were attached to a frame (gate) in the machine.
6. These gates contained all the logic (and some memory) circuits needed to form the central processing unit (CPU) of the machine.

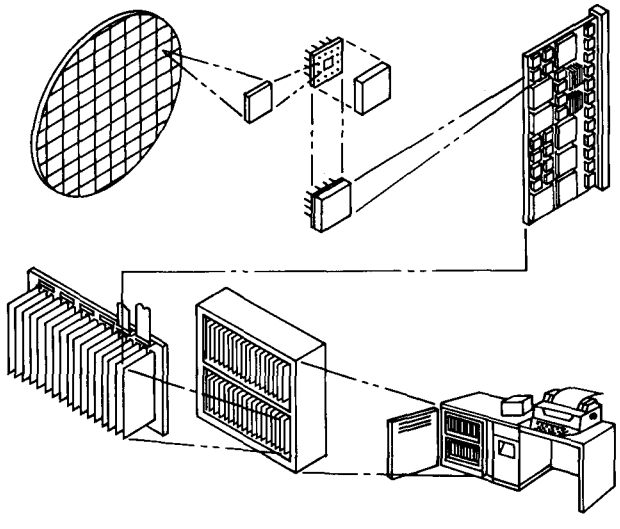


Figure 1 Conventional integrated circuit packaging: wafer to machine. Consists of dicing the integrated circuit chips from the silicon wafer, bonding the chip to a substrate, soldering the module into a card, plugging several cards into a board, cabling the boards into a gate, and attaching the gates to a machine.

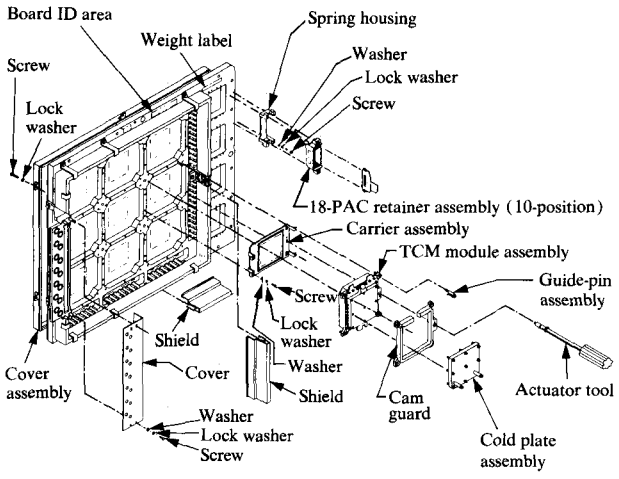


Figure 2 Nine-TCM logic board, full assembly. One level of circuit packaging has been eliminated on the 3081 Processor printed-circuit board. The 90-mm-square multilayer ceramic modules containing the LSI logic and memory chips are plugged directly into the 700 × 600-mm board.

Table 1 Complexity comparisons: High-performance *vs* ELSI board.

Factor	*ELSI board*	*High-performance board*
Size ($W \times L \times T$) (mm)	235 × 362 × 1.5	600 × 700 × 4.6
Circuitry (linear mm)	43,180	1,400,000
No. of connectors	2,384	19,200
No. of plated through-holes	8,625	41,644
Plated through-hole dia. (mm)	0.83	0.41
No. of programmable vias	—	14,400
Programmable via dia. (mm)	—	0.15
No. of card or module I/Os	1,920	16,200
No. of signal cable I/Os	288	2,160
No. of signal/power planes	2S/2P	6S/12P
Lines per channel/grid (mm)	3/3.18	4/2.5
Line width (mm)	0.20	0.08
Line thickness (mm)	0.058	0.048

As the level of integration at the chip increased, it became desirable to eliminate one of these packaging levels to reduce the number of connections (and cost) and to increase packaging density, performance, and reliability. Toward this end, an Early Large-Scale Integration (ELSI) printed-circuit planar board was developed to combine the functions of the Solid Logic Technology (SLT) printed-circuit card and board. These ELSI "planars" used soldered-in Single Chip Modules (SCMs), although the size of the ceramic substrate grew from 12.7 mm to 25.4 mm, the number of I/O pins increased from 16 to 116, and the substrate metallurgy changed from thick film (paste) to thin film (evaporated Cr-Cu-Cr). A pluggable module was also developed for the replacement of modules on the card or planar board without reflowing solder [3].

A new bifurcated spring connector system [4] appeared in the IBM 4300 processors, as well as multichip modules (up to nine chips per module) constructed with multilayer ceramic substrates [5–7]. These machines contained field-replaceable printed-circuit boards [8, 9] with 14 inner planes, and with the bifurcated connector springs soldered in the board rather than in the card, setting the stage for direct plugging of large multichip, multilayer ceramic modules into the board [10, 11]. As described previously in the literature [12], this step allows substantial increases in interconnection density in both the first level (chip, module) and the second level (card, board) of circuit packaging.

These developments paved the way for the design of the Large-Scale Integration (LSI) packaging used in the 3081 computer. Up to 118 LSI chips are mounted on a 90 × 90-mm Multilayer Ceramic (MLC) substrate [13]. The LSI logic chip is a customized 704-gate array. The water-cooled multichip Thermal Conduction Module (TCM) utilizes the MLC substrate to provide multiple layers of thick-film circuitry and each module has 1800 I/O pins brazed to its base [14].

These TCMs plug into a 700 × 600-mm printed-circuit board [15, 16], the design features of which are the subject of this paper. In the following sections, this board is described, after some complexity comparisons with an earlier technology have been noted. The module areas, signal input/output (I/O) areas, power input areas, terminating resistors, and decoupling capacitors are described in detail. These descriptions are followed by discussions of the board printed circuitry, of the signal distribution electrical characteristics, and of the power distribution system.

Complexity comparisons

The new high-performance board is considerably more complex than the ELSI board (see Table 1). The board is about five times larger in area, and about 15 times larger in volume. The four-line-per-channel board with its 2.5-mm grid, along with the larger size and increased number of signal planes, results in about a 20-times increase in the length of circuitry in a typical application. The off-grid

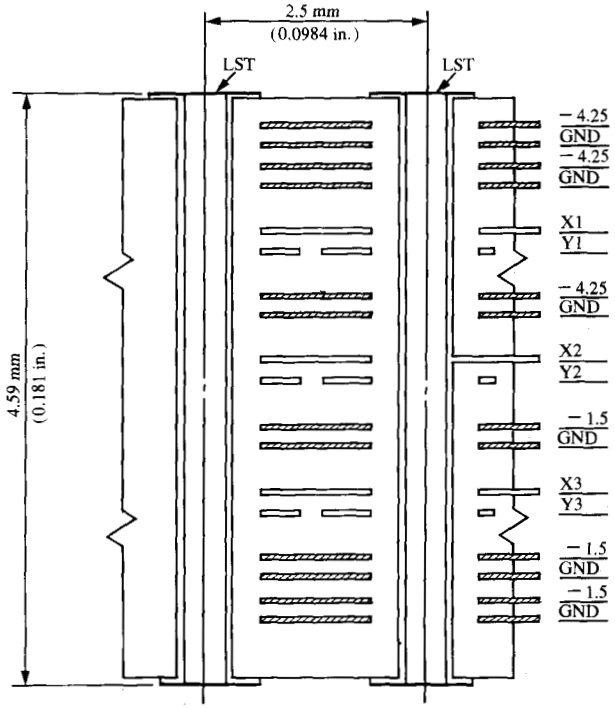


Figure 3 Logic circuit board cross section. A cross section of the 4.6-mm-thick board reveals a complex structure. Six inner signal planes, interconnected with programmable vias, and twelve power planes are combined with the outer module connector spring and engineering-change twisted-wire solder planes.

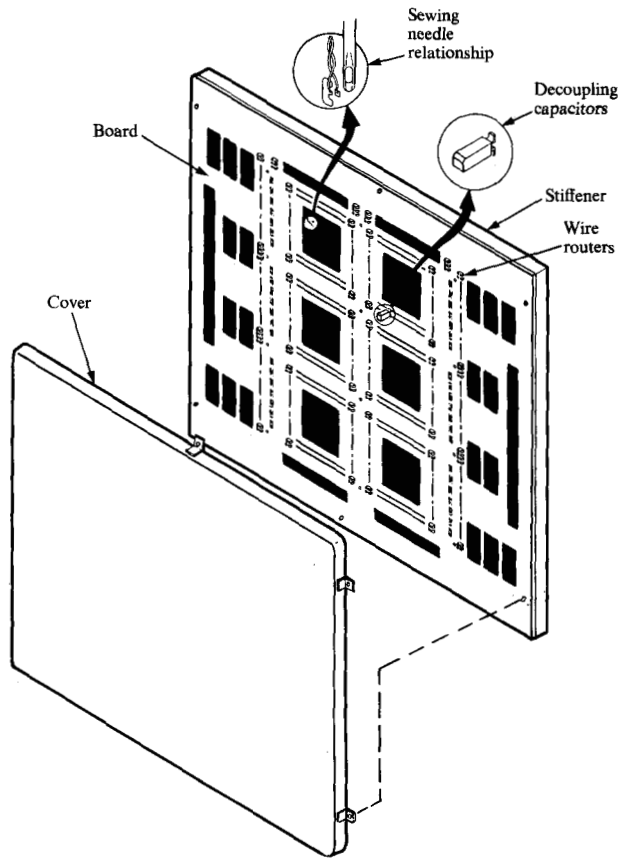


Figure 4 Wire router and cover assembly. All changes are made on this engineering change (EC) plane using twisted pairs of wires that are reflow soldered to the board. The wires are routed through the combs by a computer-directed wire-bonding machine. The decoupling capacitors are also reflow soldered to the back side of the board.

programmable vias allow better communication between signal plane pairs, since much less space is used as compared to plated through-holes (PTHs).

The board has about eight times as many connectors as the ELSI board because it is supporting nine TCMs with 1800 I/O pins each (16 200) and 12 signal cable groupers (2160) where the ELSI board contains 20 cards with 96 connectors each (1920) and 12 signal cable connectors (288). Of the ELSI board pins (2384), only 1876 are used for card and signal cable I/Os.

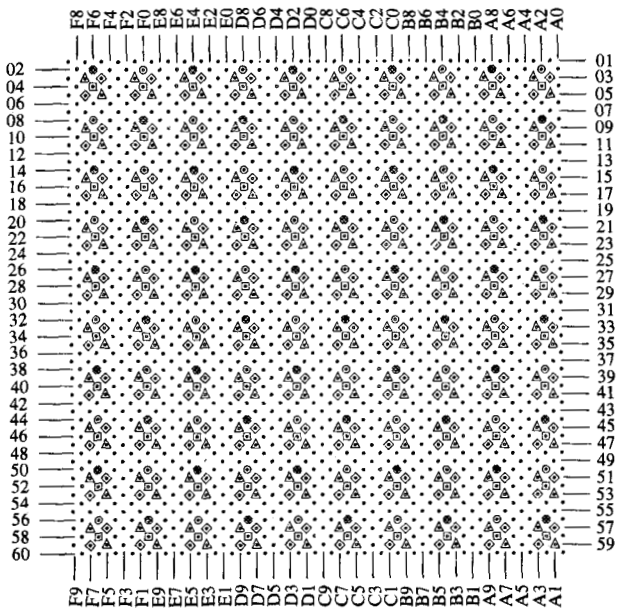
The high-performance board has six signal planes and 12 power planes arranged in plane pairs. Each signal plane pair has a ground (reference) plane on each side to control the electrical characteristics of the circuits. This type of construction (triplate), along with the dimensions and tolerances on the line width, line thickness, dielectric thickness, and dielectric constant, contribute to the high level of electrical performance of the board. The electrical characteristics of impedance, series resistance, time delay, capacitance, and inductance are held to a much tighter tolerance than on the ELSI board. The twisted-pair wire that is used to replace or augment the printed-circuit nets for engineering changes, repair, or overflow wiring also maintains a much tighter tolerance on the electrical parameters than the yellow wire that is wire wrapped on the ELSI board.

High-performance printed-circuit board

Module areas

The 700 × 600-mm (27.6 × 23.6-inch) high-performance board package was designed to support and service the 90 × 90-mm TCM (see Fig. 2). Each TCM can accommodate up to 118 of the 4.6 × 4.6-mm (0.18 × 0.18-inch) 704-logic-gate-array chips. The TCM has 1800 I/O pins brazed to one surface on a 2.5-mm (0.0984-inch) staggered grid. Of these, 1200 are signal pins; 500 are power pins at −4.25 V dc, −1.25 V dc, and ground; and 100 pins are designated as spares. The 1800 pins plug into a Zero-Insertion-Force (ZIF) connector spring soldered into each plated through-hole (PTH) in the board.

There is a Logic Service Terminal (LST) plated through-hole in the board for every signal module pin to accept the



Symbol	Legend
◬	Ground
◈	− 1.5 V
⊙	Unassigned voltage
⊡	− 4.25 V
●	Unassigned voltage
•	Logic service terminal

Figure 5 Module area signal and voltage assignments. The 1800 module pins plug into bifurcated springs soldered into the board. There are 1200 signal and 600 power connections possible in each module area.

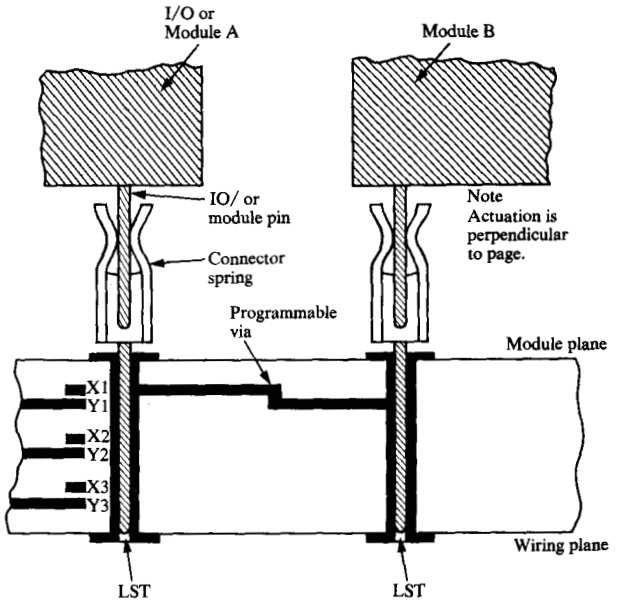


Figure 6 Via relationship and signal interconnection diagram. This cross section shows how signal pulses travel from one component to another through the printed-circuit signal planes in the board. Repairs and/or ECs are made by replacing the printed-circuit connection with a twisted pair of wires on the wiring plane.

connector spring and to make contact with one of the six signal planes (three pairs of signal planes) in the board (see Fig. 3). The LST is connected on the back (wiring) side of the board to an engineering change (EC) pad (see Fig. 4). Using this system, the printed-circuit nets in the board can be replaced or augmented by a twisted pair of wires bonded to the EC pads.

There is also a PTH in the board for every module power pin. The power PTHs connect the power planes in the board (at the same potential) and hold the connector spring for the module power pin. The power PTHs also come out to the EC pads on the back side of the board.

Every TCM requires 1800 PTHs in the board (see Fig. 5). The board is designed to accommodate a maximum of nine TCMs requiring a total of 16 200 PTHs. Communications between the TCMs use six signal planes in the board arranged in three pairs with the printed-circuit wires located between the LST PTHs.

There are lands at the LST PTHs where the circuits (nets) are to be completed. A typical module-to-module net is connected from an LST land at one signal PTH to another. As illustrated in Fig. 6, signals will be propagated from one TCM signal pin into the bifurcated spring in the LST, then to the LST PTH to the signal plane, across the signal plane to another LST, into the LST to the bifurcated spring, and then into the signal pin on the other module.

The board also has Programmable Vias (PVs) between adjacent pairs of signal planes to allow changes in line direction (see Fig. 6). The directions of the printed-circuit lines on the pairs of planes are orthogonal to each other (one vertical, one horizontal). These PVs are offset 1.25 mm (0.049 inches) from the LSTs and greatly increase the ability to wire the four-line-per-channel 2.5-mm staggered-grid board without the use of the PTHs on grid.

The module pins are inserted into the connector with zero insertion force, but the pins are actuated into the bifurcated springs with a wiping action by the use of a special tool (see Fig. 7). This wiping action between the surfaces produces a very reliable connection.

There are two basic board designs, one with nine module areas and another with six module areas. The nine-TCM board is intended for applications where a maximum

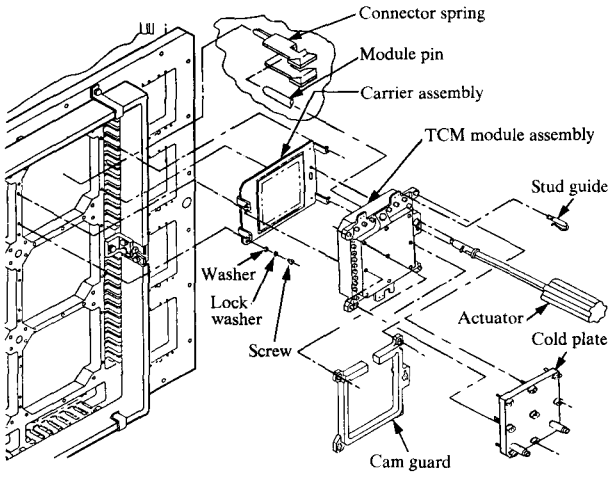


Figure 7 Module interconnection. The 1800 module pins are inserted with zero insertion force, then actuated into contact with the bifurcated spring connector using the cam tool.

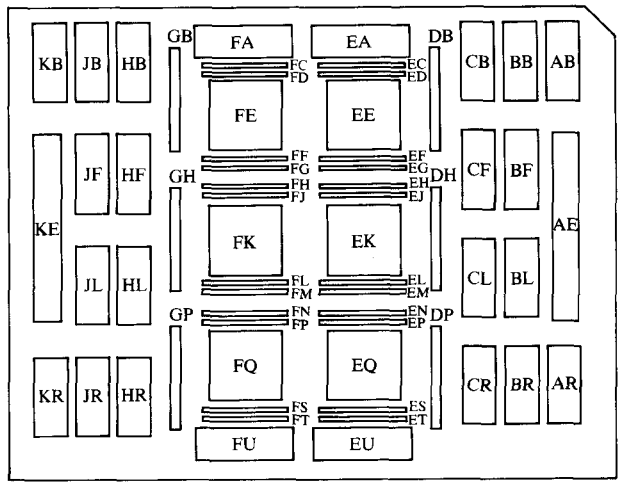


Figure 8 Nomenclature drawing showing component areas of board. The six-TCM board houses modules, terminating resistors, signal I/Os, and decoupling capacitors. Areas for soldering the power buses to the board are also indicated.

Notes:

1. Modules positioned at locations EE, FE, EK, FK, EQ, and FQ.
2. Terminators positioned at locations AE, KE, EA, FA, EU, and FU.
3. I/O locations at positions AB, BB, CB, BF, CF, BL, CL, AR, BR, CR, HB, JB, KB, HF, JF, HL, JL, HR, JR, and KR.
4. Decoupling capacitors positioned on wiring side only at locations EC, ED, EF, EG, EH, EJ, EL, EM, EN, EP, ES, ET, FC, FD, FF, FG, FH, FJ, FL, FM, FN, FP, FS, and FT.
5. Power buses at locations DB, DH, DP, GB, GH, and GP.

number of chips are needed to perform the intended function, *e.g.*, the processor board. It has sufficient signal I/Os to get on and off the board but most of its printed-circuit nets are devoted to communication between TCMs.

The six-position board was designed for machine functions which place more emphasis on communication between boards and access to the functions outside the processing unit, *e.g.*, the channel board (see Fig. 8).

The module areas were originally designed with two plated through-holes per module pin, a logic service terminal, and a redundant PTH to facilitate making repairs and/or engineering changes. The printed-circuit lines were run between redundant PTHs, and the LST and the redundant PTHs were connected on the back side of the board at the EC pad. With the bifurcated spring in the LST PTH, ECs were made by severing the connection between the redundant PTH and the LST at the EC pad and twisted-pair wire bonded to EC pads at the two ends of the net.

- *Signal I/O areas*

In addition to the areas specified for location of TCMs, there are areas in the board that are devoted to signal input and output, power input, terminating resistors and decoupling capacitors. The signals are brought onto the board from other boards and removed from the boards through special signal cables. These cables are trilead cables with 18 signal conductors and seven grounds that are soldered to a cable card. These cable cards are held together in maximum groups of ten by a retainer assembly and plugged into the board using the new bifurcated spring connector (see Fig. 9).

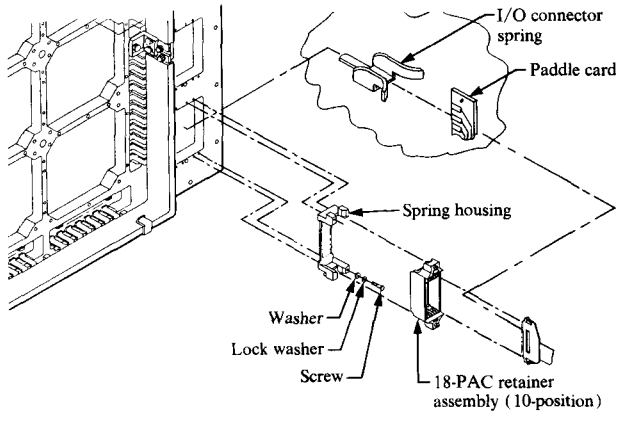


Figure 9 Interconnector assembly. The groups of paddle-card-terminated trilead signal cables plug directly into the bifurcated spring connectors. Jackscrews on both ends of the retainer assembly apply the force needed for good wiping action.

While the module pins are inserted with zero insertion force, then are locked into position to actuate the connection, the cable cards are inserted directly into the bifurcated

Table 2 Typical board designs.

Factor	*Channel board (six-position)*	*Processor board (nine-position)*
I/O-module nets	563	343
Module-module nets	301	2,593
I/O-module-terminating resistor nets	1,142	187
Module-terminating resistor nets	163	69
Total nets	2,169	3,129
Overflow wires	122	93
Line segments	14,636	15,887
Program vias	10,819	12,480
Plated through-holes used	5,944	6,600
Average line segment length (mm)	73	68
Average program vias/net	5.14	3.93
Average plated through-holes/net	2.83	2.08

springs using locking screws to complete the connections for the group of ten cable cards (Fig. 9). The signal PTHs and the ground PTHs are arranged in groups in the board with an EC pattern on the back (wiring) side of the board. These areas are similar to the module areas. ECs and repairs can thus be made in the signal I/O areas in the same way as is done in the module areas.

- *Power input areas*

Power is brought onto the board with braided copper cables attached to a laminar power bus (Fig. 2). The power bus is comprised of copper sheet stock that is laminated together with polytetrafluoroethylene dielectric between the potential levels. The tabs on the laminar bus are soldered to specific power pads on the surface of the board (Fig. 2). Power is distributed to the power planes (Fig. 3) by plated through-holes in these power pickup areas. The number and distribution of the power planes are dictated by the amount of current needed at each voltage level (-4.25 V and -1.5 V) and the need to maintain a reference plane (ground) adjacent to the signal plane pairs. The number and distribution of the power PTHs in the power pickup areas were optimized with these considerations in mind.

- *Terminating resistors*

The printed-circuit and twisted-wire nets that terminate in the board are connected to ground through pluggable 80-ohm terminating resistor packs with six signal and two ground leads. The leads of the terminating resistor packs are inserted in the bifurcated spring connectors in the appropriate areas.

The terminating resistors were originally soldered directly into the board. The design was changed to make them pluggable in order to enhance testability of the board, since the function of the resistor is to connect the net to ground through a resistance which will dissipate the signal pulse. With the nets connected to ground, it is difficult to distinguish between a high resistance open net and two nets shorted together (and then connected to ground). Also, combinations of opens and shorted nets were very difficult to detect.

By making all the terminating resistors pluggable, all the nets can be tested by probing the two ends of the nets at the PTH lands and comparing the reading to an expected value. This also eliminates the necessity for performing a resistance test on the terminating resistor in the board.

- *Decoupling capacitors*

Decoupling capacitors (decaps) are required to provide for proper power distribution and to limit noise. The capacitors are mounted around the module sites by reflowing the solder on the capacitor lands on the back (wiring) side of the board. The decap lands are connected to the power planes by PTHs. A pair of lands are connected to either -4.25 V and ground or -1.5 V and ground. The decaps thus provide an ac short between the power planes. The decaps supply the module with the transient power required by active devices switching on and off. The decoupling capacitors are put on the board in the later stages of component assembly after the power planes are tested for power-to-power shorts.

Board circuitry

The basic function of the high-performance board is to support the 90-mm modules containing the logic chips. To perform this function, the board contains conductive paths (nets) between the signal I/Os, the module sites, and the terminating resistors (Fig. 8). Typically, a net will be an I/O-to-module net, a module-to-module net, a module-to-terminating resistor net, or an I/O-to-module-to-terminating resistor (three-pin) net (Table 2). There are some unusual cases where nets connect more than one module pin to other module pins in series, several module pins to a terminating resistor, or even an I/O to an I/O, but the net counts given in Table 2 reflect two typical applications of a six-module-position (channel) and a nine-module-position (processor) board.

As can be seen from the distribution of nets by type, the channel and processor boards have different functions. The channel board is the primary interface of the CPU with the

rest of the machine. This is reflected in the high I/O usage (1705). There are relatively few module-to-module nets, indicating little communication between modules. The processor board, on the other hand, has a large number of module-to-module nets with a high level of module-module interaction. The number of nets terminated (256) and the number of I/Os used (343) imply that the chips on the processor modules are performing the mathematical operations of the CPU.

The number of overflow (twisted-pair) wires indicates either an inability of the designer to bury them as printed circuits [these nets may be of critical length (time delay)] or that there was an engineering change to the board that resulted in printed-circuit nets being stripped and twisted-wire nets added.

The line segments are sections of the printed-circuit nets that run between plated through-holes and/or programmable vias. The programmable vias (Fig. 6) form an electrical interconnection between orthogonal line segments on a signal plane pair.

Not all of the plated through-holes (41 644) in the board are used to form nets. Some are used for power distribution (4500) and the remainder are unused (33 968).

It is interesting to note that even though the channel board has fewer nets (2169), the average length of a printed-circuit wire segment (73 mm), the average number of program vias per net (5.14), and the average number of plated through-holes per net (2.83) are all higher than in the processor board. This reflects both the difference in the numbers of modules per board (six *vs* nine) and the difference in function.

The two board configurations (six and nine) thus provide sufficient module sites, I/Os, and terminating resistors for the various functions performed in a machine. These board designs can be depopulated (five or eight modules, respectively), but when used in combination can support the total number of modules in a machine.

Signal distribution electrical characteristics

A detailed definition of the electrical parameters used in the following discussion is given in the Appendix.

The impedance (Z_0) of the nominal 80-ohm board is held to a tolerance of ±10 ohms by maintaining a tight control on the printed-circuit line width, the thickness, the distance from the reference plane, and the dielectric constant of the insulator. The nominal Z_0 value assumes an average line crossing, from an adjacent orthogonal signal plane, of 35%. The series resistance (R_s) at 25°C is held to 50 ± 20 milliohms per centimeter. The time delay (t_d) is restricted to 70 ± 5 picoseconds per cm. The capacitance (C) is 0.85 picofarads per cm and the inductance (L) is 5.5 nanohenries per cm.

Since the triplate construction offers a homogeneous medium, the inductive and capacitive coupling coefficients (K_L and K_C) are equal. The near-end coupled noise (V_{qne}), in mV, is dependent on whether the printed-circuit line is in the open-channel area, the through-hole area, or in an open channel next to a through-hole area. The values are 73 mV, 189 mV, and 112 mV, respectively, when the lines are properly terminated. The far-end noise (V_{qfe}) is zero. Due to the tight coupling in the hole areas, where the printed-circuit lines are on a 0.22-mm spacing, the continuous coupled length of two parallel lines is restricted in the wiring program. Also, the continuous plane-to-plane parallel coupling between a plane pair is restricted.

The transmission line parameters for the twisted-pair cable used for engineering changes, repairs, or overflow (critical length) wires is controlled by specifying the wire diameter, insulation wall thickness, twist ratio, and insulation dielectric constant. The impedance is 80 ± 10 ohms, the dc resistance at 25°C is 31 ± 3.5 milliohms per cm, and the time delay is 53 ± 2.5 picoseconds per cm. The capacitance is either 0.64 or 0.77 picofarads per cm depending on whether the twisted-pair is isolated or bundled. The near-end coupled noise (V_{qne}) of a bundle of twisted-pair wires is designed to be 85 to 125 millivolts.

The electrical characteristics of the module pin actuated in the zero-insertion-force bifurcated-spring connector are also controlled. The series resistance is 13 milliohms, including contact resistance, the capacitance is 0.3 picofarads, with all surrounding pins and springs grounded. The time delay is 30 picoseconds, and the inductance is 2 nanohenries. The near-end connector noise depends on the number of adjacent active conductors, but is 30 to 50 millivolts with four to eight adjacent active conductors. The far-end connector noise is typically less than 20 millivolts.

The plated connections in the board are logic service terminals or engineering-change bonding pads (on the surface). The capacitances of these connectors are 1.1 and 0.3 picofarads, respectively. The series resistances are 7 and 4 milliohms maximum, respectively.

The trilead signal cables terminated to an 18-signal, 7-ground-cable card have their own unique set of electrical characteristics. Since the conductor path length on the cable card varies between 7 and 16 millimeters, the values given will have a range. The capacitance is 1.51–2.29 picofarads, the time delay is 95–152 picoseconds, and the series resist-

ance is 33–62 milliohms. The near-end coupled noise is about 80 millivolts, worst case, and the far-end coupled noise is about 60 millivolts, worst case. The worst case is found in a quiet conductor between signals.

Power distribution

The printed-circuit logic board cross section (Fig. 3) has 12 one-ounce copper power planes (six for ground, three for −1.5 V, and three for −4.25 V). The full board assembly drawing (Fig. 2) defines the location of the power bus which solders to the module side of the board. Power is distributed to the board through the power bus tabs (Fig. 2), which are connected by plated through-holes to the internal power planes. Decoupling capacitors (720 maximum per board) are soldered to the wiring side of the board (Fig. 4).

Power is distributed from the board to the module power planes through an 1800-pin connector, of which 500 pins are used for power (Fig. 5), 200 are at ground, 200 are at −1.5 V, and 100 are at −4.25 V.

The overall low-frequency electrical tolerance of the power supplied at the solder pads on the chip is +4.6% −7.4% (180 mV) or −1.5 V (−1.6 V to −1.4 V) and +4.6% −2.3% (295 mV) of −4.25 V (−4.4 V to −4.2 V). This is divided between chip dc, module and connector dc, second-level dc, second-level ac (pulse widths greater than or equal to 6 nanoseconds at 50% pulse amplitude), and regulator static and dynamic deviations.

The tight tolerance on potential differences is maintained by minimizing the resistance and inductance path from the power sources (decoupling capacitors) to the modules. These board design parameters are: board cross section (inductance), clearance hole diameter (inductance and resistance), thickness and quantity of power planes (resistance), bus design (resistance and 1 kilohertz concerns), and capacitor replacement and attachment.

The tantalum decoupling capacitor has two ribbon leads that surface solder to predesignated lands on the wiring side of the board. The electrical characteristics of these components are: 40 microfarads minimum at less than 20 kilohertz, 200 milliohms maximum between 20 kilohertz and 21 megahertz, and 1.5 nanohenries maximum above 21 megahertz. This device is used for the entire decoupling spectrum for the board and module. The quantity of capacitors required is a function of board load and module/board current changes.

The power distribution system supplies up to 600 amps of current to the nine modules on the nine-TCM board. The two potentials (−4.25 V and −1.5 V) and ground supplied to the logic (and memory) chips on the modules allow them to perform their switching function. The voltage drops are tightly controlled by a sense point on the power bus which feeds back into the power supply.

In addition, there are special voltage sense (and thermal sense) circuits in the boards to detect (and correct) the potentials at the C-4 joints on the chips.

Summary

The new logic packaging structure developed for the IBM 3081 computer features large multichip, multilayer ceramic modules plugged directly into a large multilayer printed-circuit board. The conventional scheme of soldering single-chip modules into cards and then plugging the cards into boards is thus eliminated.

By allowing up to nine of the modules to be mounted on one board, the circuit performance was greatly improved, since the active devices were moved closer together, thus reducing the delay associated with long conductive paths and connectors. Also, one level of packaging was eliminated (the card level), along with all the connectors needed to get on and off that level.

This packaging scheme permits the electrical characteristics of the multilayer printed-circuit board to be tailored to the device parameters and held to a much tighter tolerance. This results in a higher-performance system.

Appendix: Definitions of electrical parameters

- Impedance (Z_0)—impedance of a single transmission line:

  $$Z_0 = (L/C)^{1/2}.$$

- Series resistance (R_s)—dc resistance of a transmission line:

  $$R_s = \frac{\rho \ell}{A}(1 + k\Delta t),$$

  where

  ρ = conductor resistivity,
  ℓ = line length,
  A = cross-sectional area,
  k = conductor temperature coefficient of resistance,
  Δt = change in temperature from 20°C, and
  R is usually specified as a unit-length parameter.

- Time delay (t_d)—time delay of a transmission line:

  $$t_d = (LC)^{1/2},$$

  where t_d is usually specified as a unit-length parameter.
- Capacitance (C)—total capacitance of a single transmission line in its dielectric medium with all other lines floating. C is usually specified as a unit-length parameter.

- Inductance (L)—inductance of a single transmission line:

$$L = \frac{(\textit{time delay in air})^2}{C_0},$$

where C_0 = air capacitance of the transmission line, *time delay in air* = 33.37 ps/cm, and L is usually specified as a unit-length parameter.

- Capacitive coupling (K_C)—Capacitance coupling coefficient between active and quiet transmission lines.
- Inductive coupling (K_L)—Inductive coupling coefficient between active and quiet transmission lines.
- Coupled noise—The noise values presented are for matched case normalized noise. This is the noise coupled to a quiet (nonswitching) line from active line(s) assuming all lines are terminated at both ends in the Z_0 of the transmission line. "Normalized" assumes a signal amplitude (ΔV) of 1000 mV and a rise time (Δt_r) of 1 ns.
- Near-end noise [V_{qne} or $V_{qne}(\max)$]—This is the noise generated on the quiet line end nearest the switching driver(s) end of the active line(s). Near-end noise can be expressed as a unit-length parameter (V_{qne}) which is valid for coupled lengths, up to the critical coupled length. For coupled lengths greater than the critical coupled length, the noise magnitude is constant and is defined as V_{qne} (max). The critical length is for the condition when the line delay equals half the rise time.

$$V_{qne} = \frac{\Delta V}{\Delta t_r}(\epsilon_r)^{1/2}\frac{(K_c + K_L)}{59.9} \quad \text{mV/cm, and}$$

$$V_{qne}(\max) = \frac{\Delta V}{4}(K_C + K_L) \quad \text{mV,}$$

where ΔV is in mV, Δt_r is in ns, and ϵ_r is the dielectric constant.

- Far-end noise (V_{qfe})—This is the noise at the opposite end of the quiet line:

$$V_{qfe} = \frac{\Delta V}{\Delta t_r}(\epsilon_r)^{1/2}\frac{(K_C - K_L)}{59.9} \quad \text{mV/cm.}$$

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