D. J. Bendz
R. W. Gedney
J. Rasile

Cost/Performance Single-Chip Module

The introduction of the high performance T^2L device technology for the IBM 4300 Systems and the System/38 required extensions of the 24-mm metallized ceramic module used in prior IBM systems. The extension of the metallized ceramic technology into a physically larger 28-mm module, electrically enhanced with a reference plane and with fine line (0.025-mm) wiring, is described. The reliability of this module was evaluated with particular emphasis on corrosion and metal migration in humid environments and on exposure to atmospheric contaminants.

Introduction

The metallized ceramic module technology [1] is proving to be versatile and extendable as it evolves to meet chip and packaging technology needs. It was introduced into manufacturing in IBM in 1973 as a wiring vehicle supporting a 100-gate LSI bipolar chip and a 500- to 700-circuit LSI/FET logic chip. These devices required more input/output channels and greater wiring densities than could be provided by the MST technology [2] current at that time. The development of a photolithographically defined thin film metallurgy with a larger but still inexpensive 24-mm ceramic substrate provided both capabilities. In addition, the reliability of the metallized ceramic module proved to be an outstanding feature.

Later, this technology had to be extended as device technologies required additional capabilities. Improved electrical performance, greater wiring density, and more input/output channels were required to support the high speed transistor-transistor logic (T^2L) circuit chip used in the IBM System/38 and 4300 computer systems. A 28-mm-square module with 116 input/output pins was developed to satisfy these requirements.

This paper reviews the original metallized ceramic module technology and then describes how it was extended to satisfy the requirements of the high performance T^2L technology. The paper specifically deals with the physical, electrical, and reliability requirements of the module, as well as the process modifications required to build it.

Metallized ceramic technology

The basic metallized ceramic substrate process begins with a ceramic square on which metallurgical strata of chromium for adhesion, copper for conduction, and chromium for a solder flow barrier are deposited (Fig. 1). Circuitry is defined in the strata by a photolithographic process using standard resist techniques and sequential etching methods. The circuitry is point-to-point wiring that connects semiconductor device pads with input/output pin connections, which are inserted in the second level package. The pins are inserted through preformed holes in the substrate and are mechanically swaged in place. The pins and top surface are subsequently tinned to prepare the pins for connection to the second level package and to prepare the top surface of the substrate for chip attachment.

The chip is attached to the substrate using the "Controlled Collapse Chip Connection" (C-4) [3] process developed for tin-lead interconnections. A polyimide coating is applied to the top surface, an aluminum cap is placed over the assembly, and an epoxy sealant is dispensed on the underside as a liquid and cured to provide a "quasi-hermetic" seal. After it has been marked and tested, the completed module is then ready for attachment to the appropriate second level package.

Metallized ceramic technology extensions

For the T^2L module the base metallized ceramic technology had to be extended to provide increased wiring density,

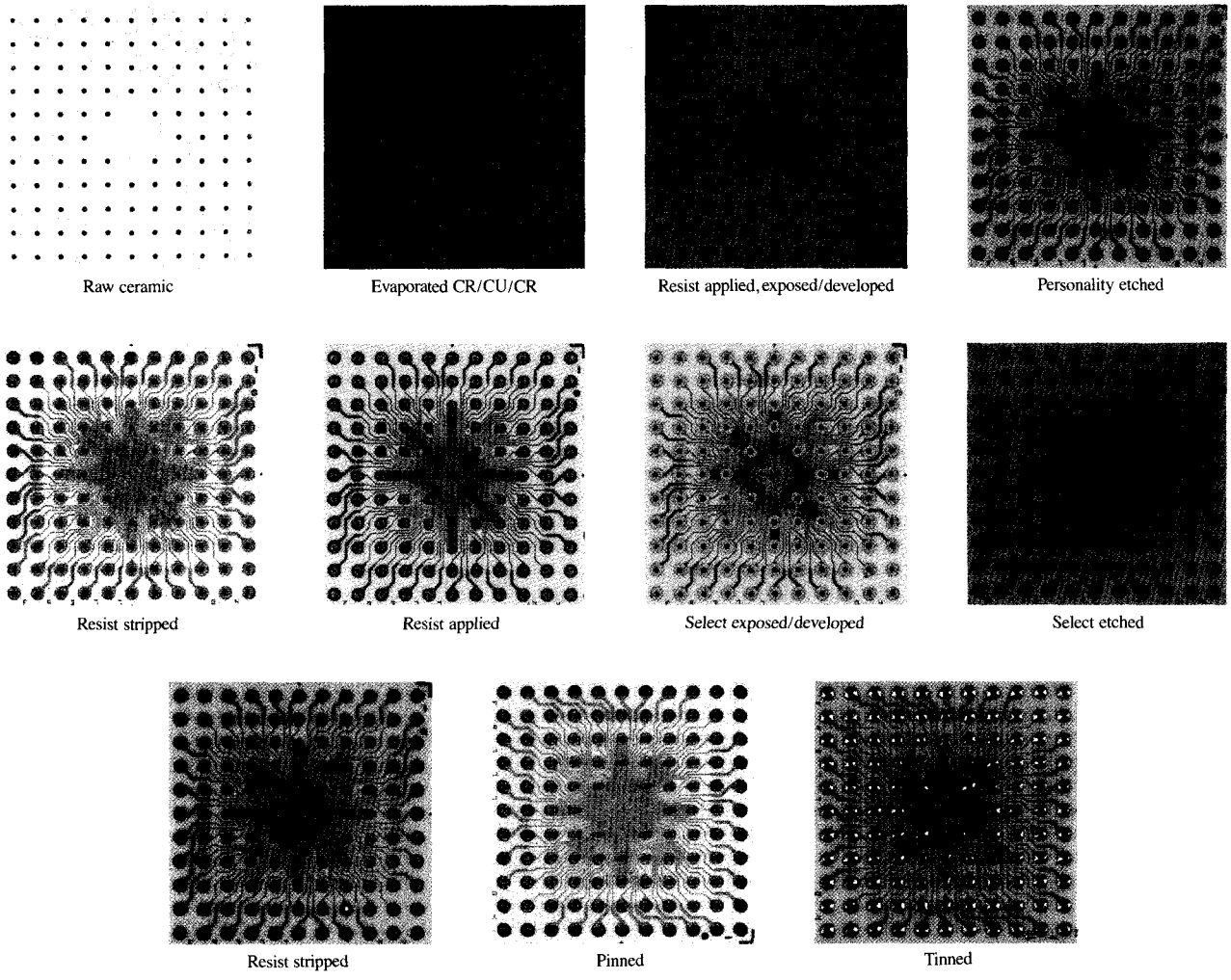

Figure 1 Substrate process steps.

especially in the device attachment area. An increase from 50 pin-to-chip connections to 132 such connections was required. After interconnecting the power pads, the module required 116 input/output pins. The 132 chip interconnection pads were arranged on 0.25-mm centers in a 17 × 17 array, which was "depopulated" to allow a greater number of wiring channels in the device area (Fig. 2). The line density in this area required a reduction in line and spacing dimensions in the wiring channels. A comparison of the standard technology dimensions with the "fine line" extensions is given in Table 1.

Improved electrical noise characteristics also had to be provided.

• *Substrate process enhancements*

The ceramic substrate we use is provided by several companies that had been supplying the 24-mm version for several years. The increase to the 28-mm size, plus the smaller photolithographic features, required less camber and closer tolerances on other dimensions. The substrate camber was reduced by a factor of two, a change that had to be closely monitored during incoming inspection.

Additional controls of the photolithographic process were required to produce the finer dimensions and tighter tolerances of Table 1.

The effects of alkaline and oxidant concentrations and temperature on the chromium etch time were investigated for substrates and for glass slides as controls.

Figure 3 shows the effect of alkaline concentration on base chromium etch time. The object was to establish process limits so as to maximize throughput while maintaining product quality. Additional increases in alkalinity produced

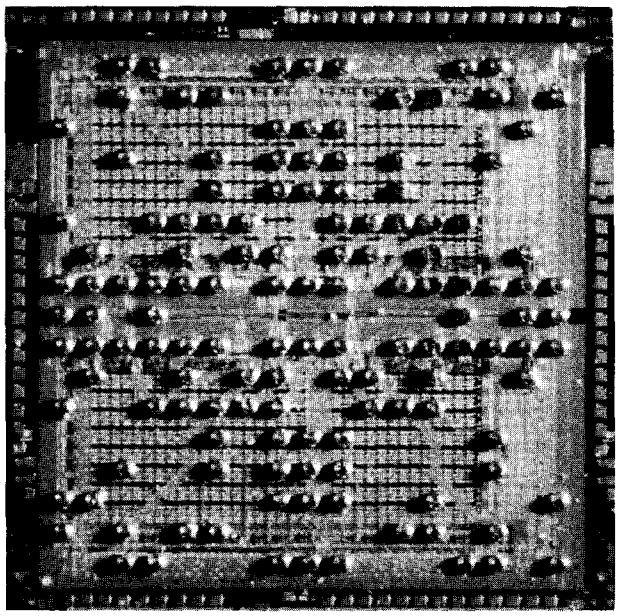

Figure 2 Chip C-4 pad arrangement and matching substrate pads.

Table 1 Comparison of pattern dimensions of original and "fine line" modules.

	Original (mm)	*Fine line* (mm)
Lines	0.125 ± 0.04	0.050 ± 0.025
Spaces	0.075 ± 0.025	0.050 ± 0.025
Chip pad (diameter)	0.125 ± 0.025	0.090 + 0.025 − 0.013
Lines (in chip area)	0.075 ± 0.025	0.020 ± 0.013
Spaces (in chip area)	0.075 ± 0.025	0.040 ± 0.013

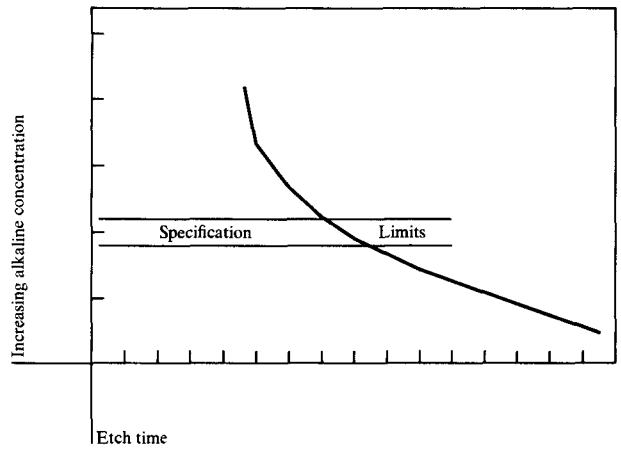

Figure 3 Effects of alkalinity on base chromium etch time.

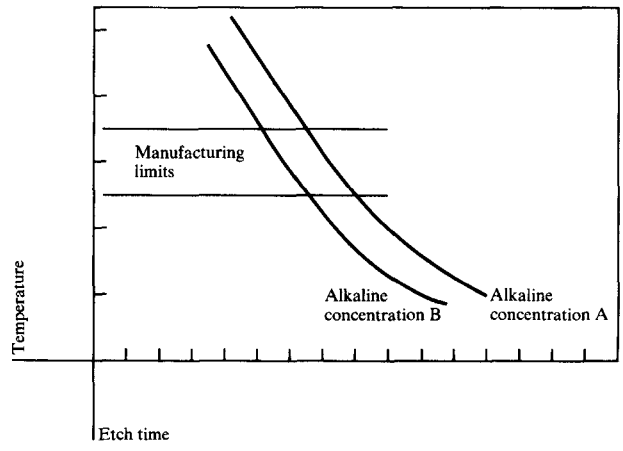

Figure 4 Effects of temperature on base chromium etch time.

rapid penetration of the etchant through the copper and unwanted attack of the base chromium layer while etching the top chromium layer. However, increasing oxidant concentration had no adverse effects and was therefore specified near its solubility saturation point for a rapid etch rate. Figure 4 illustrates the relationship between chromium etch rate and etchant temperatures. Again the process limits were determined based on maximizing throughput while this time minimizing process sensitivity.

The copper etch process limits required no concentration or temperature modifications.

To evaluate the photoresist process, five ranges of photoresist thicknesses were prepared and divided into cells with at least ten substrates per cell. All were etched simultaneously. After resist removal, all substrates were examined microscopically at 30× for line widths and defects. The photoresist thickness was established at 4.5 μm by correlating exposure time and defects with the optimized etch operation.

Prior to proceeding to the pinning operation, the personalized substrate is electrically tested for short and open circuits in the lines. Thus, defective substrates can be identified and rejected prior to final substrate processing. However, because the tinning operation has the potential of producing solder bridging, a second electrical test is done prior to shipment to the module assembly line.

- *Module processing*

As shown in Fig. 2, the design of the device interconnection is a depopulated area array of pads. This allows power to be

brought directly in to all quadrants of the device through a sufficient number of power pads to minimize inductance in the power supply path.

Unfortunately, the geometry of the device interconnections prevents visual inspection of 77% of the completed solder (C-4) joints. This, coupled with the large number of C-4 interconnections (132), meant that the new product was more vulnerable to process defects. Nevertheless, we found that careful control of the flux and solder reflow process provided adequate joining. Automation of flux dispensing and chip placement ensured that specifications were met with adequate process control margins.

We also found that tighter controls were required on the reflow of the pads on the semiconductor wafer. Fortunately, these requirements were also within the capabilities of the device process and could be satisfied with only minor changes.

After device attachment a copper reference plane [4] laminated to a Mylar film is added to the 28-mm module. Holes are punched to replicate the pin pattern, and the plane is mounted above the substrate circuitry and fits over the pin heads (Fig. 5). The Mylar provides electrical insulation and separation of the substrate circuitry and the reference plane.

Copper wires are attached at their mid-points on the copper surface of the reference plane. After the plane is positioned on the substrate, the two ends of the copper wires are attached to separate adjacent pin heads, so that the wires provide electrical connection as well as mechanical support. Wires are attached at four locations on each plane, as diagrammed in Fig. 5.

The actual bonding to the plane and pin heads is accomplished with a specially made capacitor discharge welding tool, designed for optimum yield in this application.

The encapsulation processes, which provide a polyimide top seal and an epoxy back seal, as well as the capping and marking procedures, required only minor tooling modifications to handle the larger substrate sizes.

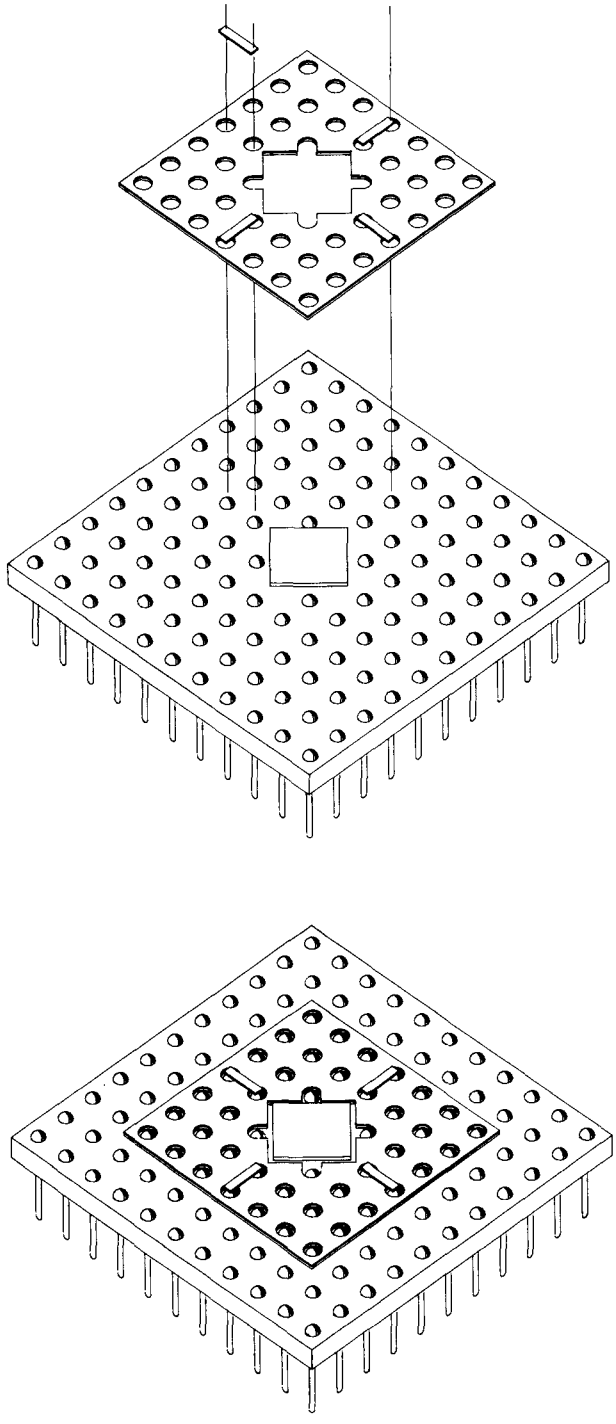

Figure 5 Voltage reference plane assembly.

Performance requirements

To connect all 132 C-4 pads, it was necessary to utilize line widths as small as 0.020 mm leading out from under the chip. As soon as possible, lines were widened to minimize dc resistance. With this technique and the high conductivity of the copper line, resistance did not play a major role in the electrical performance of the technology.

Two key electrical noise problems had to be considered seriously in this design. The first is "ΔI noise," which is developed when a large shift in current occurs across a common mode inductance in the power supply path as several drivers switch simultaneously. The second is coupled noise, which is produced when energy from a switching (or active) line is coupled into a non-switching (quiet) line.

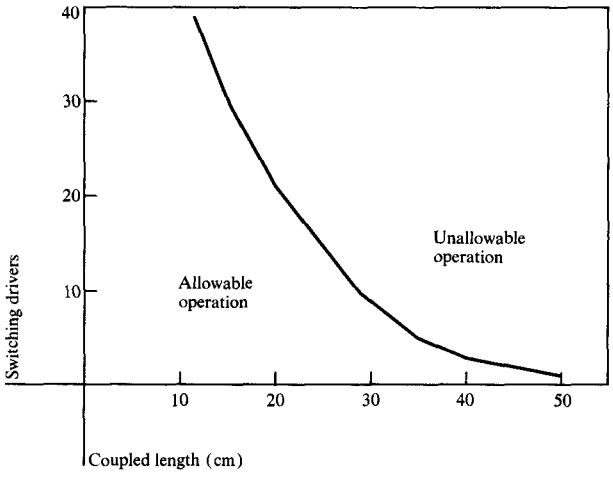

Figure 6 Allowable switching and coupling for emitter followers.

Table 2 Coupled line data for the 28-mm module.

Driver coupling	*Coupled length* (cm)		
	Average	*Maximum*	*Minimum*
Active adjacent to quiet	0.76	1.22	0.28
Active adjacent to quiet adjacent to active	0.66	0.81	0.25

Coupled noise depends on the rise time of the signal on the active line and the length of the adjacency between the lines. In a system environment, it is common to have both noise sources occurring at nearly the same time. For actual machine design, a computer program was developed to predict the overall package-related noise, as described by Davidson [5].

For the active emitter follower on the 28-mm metallized ceramic module, the ΔI noise has been found both experimentally and theoretically to depend on the near-end load capacitance and the number of pull down resistors on the active net.

The concepts of coupled noise are well understood [6]. In order to limit coupled noise occurring under worst case switching conditions, the reference voltage plane mentioned earlier was added to the module. This plane is located at a calculated optimum distance above the surface conductors. In addition to significantly reducing the coupled noise, the reflected noise is also lowered through minimizing the impedance mismatch for the conductors at the module and card package levels.

Line characterization of the 28-mm module

The characteristic impedances of the module signal lines were determined so that module coupled noise on the 28-mm module could be accurately calculated. The parameters are given in Eqs. (1) and (2) in matrix form for two typical parallel coupled lines on the substrate:

$$L = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} = \begin{bmatrix} 10.62 & 4.22 \\ 4.22 & 10.62 \end{bmatrix} \frac{\text{nH}}{\text{cm}}, \quad (1)$$

$$C = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} = \begin{bmatrix} 0.72 & 0.35 \\ 0.35 & 0.72 \end{bmatrix} \frac{\text{pF}}{\text{cm}}. \quad (2)$$

These characteristics were determined from measured data on selected typical lines on the 28-mm substrate. The coupled length statistics are summarized in Table 2.

To analyze the combined ΔI and coupled noise, the computer program alluded to earlier was made available to system designers. This program, which also includes the device model, takes account of both voltage bus transient noise and connector coupled noise.

In order to minimize the number of computer noise runs, a guideline for emitter follower nets on cards and boards has been developed. Nets that conform with this guideline do not require computer analysis. Figure 6 illustrates the guideline, which is a trade-off between the number of switching drivers and the total length of coupling.

Reliability

The program historically used to predict reliability of the 24-mm design had to be modified for the 28-mm module. The existing algorithms quantified chip-to-substrate interconnection reliability, conductor (copper) corrosion, and conductor (copper) migration. The geometrical aspects of the new design required that these algorithms be modified, or at least re-verified, and the program had to be extended to predict any change in reliability resulting from addition of the ground plane.

The susceptibility to fatigue of lead-tin solder joints between the chip and substrate is a function of the difference in the thermal expansion coefficient between the silicon device material and the alumina substrate material; this has been investigated previously [7, 8].

The essential differences introduced by the 4300 system module are the larger chip, larger device attachment radius, smaller substrate attachment radius, and higher solder volume. In considering improvement alternatives, it was obvious that certain aspects of the design could not be simply altered because of inherent design or process factors. Among

these were device size and solder volume. Solder height and solder pad cross section are dependent on the connection area between the chip and substrate. As a "rule of thumb," the optimum cross section and solder height are obtained when the solder radius on the substrate is 1.1 times the solder radius on the device. The device solder radius was set at 0.120 mm due to processing restrictions. The line density on the substrate, however, precluded a solder radius as large as 0.132 mm. Use of an "effective" radius provided a solution which could be applied to the interconnections most susceptible to fatigue failure. An elliptically shaped pad was used having an area equivalent to that of a circle of optimum radius. This design allowed sufficient area in the wiring channel for circuitry since the pads were oval instead of round.

The resistance to joint fatigue, induced by the thermal mismatch between device and substrate, was evaluated in the laboratory using an accelerated thermal cycle test. The assembled module was placed in a chamber which was cycled from 0°C to 100°C three times per hour. The electrical resistance of those joints most likely to fail was monitored using four probe points. An increase in this resistance is indicative of a fatigue crack, and the joint is considered to have failed once the change has reached 200 milliohms. A log normal plot of the failures *versus* the number of cycles to failure was generated. The median, N_{50}, and standard deviation, σ, were then used in conjunction with appropriate acceleration models to predict performance in a machine environment. Norris and Landzberg [9] have defined this relationship as

$$\frac{N_{\text{lab}}}{N_{\text{machine}}} = \left(\frac{f_l}{f_m}\right)^{1/3} \left(\frac{\Delta T_m}{\Delta T_l}\right)^2 \phi(T_{\max}) , \tag{3}$$

where

N_{lab} = number of cycles to failure during test,
N_{machine} = number of cycles to failure in the field,
f_l = cycling frequency during test,
f_m = cycling frequency in the field,
ΔT_l = thermal excursion during a test cycle,
ΔT_m = thermal excursion during a field cycle, and
$\phi T_{\max} = \dfrac{\text{Life}(T_{\max 1})}{\text{Life}(T_{\max 2})}$,

which is a ratio of life times under two temperature conditions, compensating for the temperature effects of accelerated life testing.

Analysis of the test results on 150 modules (from three product lots) yielded an N_{50} (lab) = 6307 and σ = 0.38%, close to predicted values for a round pad. Extrapolated to field conditions, a maximum of 0.01% cumulative failures over 12 years could be expected for the C-4 fatigue life

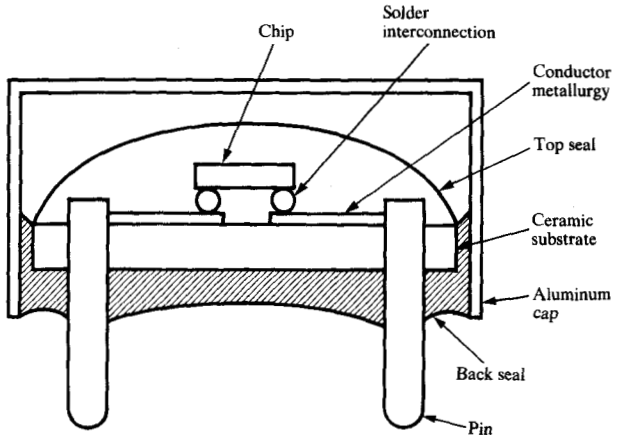

Figure 7 Cross section of encapsulated module.

parameter. This result supported the design prediction that an oval shaped pad of equal area to a round pad would be equally reliable.

The standard 24-mm module is protected by an aluminum cap and an epoxy [9] dispensed as a liquid to provide a back side coating and a seal between the aluminum can and the substrate edge, as illustrated in Fig. 7. The epoxy layer is slightly permeable to gases and moisture, and although the resulting potential of copper corrosion and/or copper migration is slight, the increase in substrate size increases the permeation area.

Surfaces that are low in ionic contamination do not readily support copper migration. However, the possible presence of such contamination from the photolithographic process, as well as from the epoxy back seal application and cure processes, had to be investigated. Standard process controls were implemented for the 24-mm module to maintain chloride levels within a module at or below 5 micrograms per unit. Testing of the 24-mm technology under accelerated temperature and relative humidity conditions (85°C, 80% RH) with and without 50-V bias had shown excellent reliability with this level of chloride.

A test vehicle for the larger substrate was designed with specific sites available to evaluate the limits of the design specification. One hundred four 0.025-mm gaps were tested under accelerated conditions (85°C, 80% RH) with a 10-V dc bias for 1000 hours; a failure was defined as insulation resistance less than 1×10^6 ohms. No failures occurred, and subsequent failure analysis revealed no observable migration across the small spaces.

Copper circuitry is known to be vulnerable to sulfide gases, particularly under humid conditions. The most

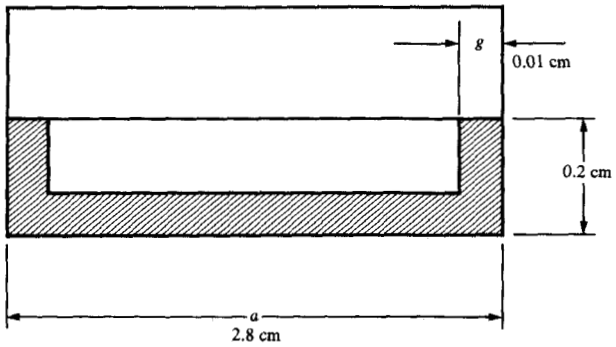

Figure 8 Module seal cross section.

common sources of sulfur in a machine environment are hydrogen sulfide (H_2S), sulfur dioxide (SO_2), and elemental sulfur (S_8). Even though the elemental form exists in the atmosphere at concentration levels one to two orders of magnitude below the other two species, the solubility of S_8 in plastic encapsulating materials is four orders of magnitude greater. (The permeability aspects of these materials have been discussed by Berry and Susko [10].) In addition, the field exposure to the sulfide gases of the metallized ceramic module configuration has been analyzed by Memis [9]. His treatment assumes that corrosion is a result of the gas diffusing through the epoxy seal and nucleating on a conductor, with corrosion progressing until the full conductor width has been converted to non-conducting copper sulfide (Cu_2S). This analysis was made for the original conductor width and the diffusion area of the 24-mm module. Both of these factors changed for the worse in the new design, and its reliability in terms of corrosion had to be reassessed. Using Memis' calculations [10] for this assessment,

$$V = \frac{\pi W^2 h}{4}, \tag{4}$$

$$W_c = VP_c = \frac{\pi W^2 h P_c}{4}, \tag{5}$$

$$W_s = \frac{1}{2} W_c \times \frac{AW_s}{AW_c} = \frac{\pi W^2 h P_c AW_s}{8AW_c}, \tag{6}$$

where

V = corroded volume (cm^3),
W = line width = 2.0×10^{-3} cm,
h = line height = 8.0×10^{-4} cm,
W_c = weight of copper consumed (g),
P_c = copper density = 8.9 g/cm^3,
W_s = weight of sulfur consumed (g),
AW_s = atomic weight of sulfur = 32.06, and
AW_c = atomic weight of copper = 63.54.

Solving this series of equations for the 28-mm module yields

$$V = 2.51 \times 10^{-9}\ cm^3, \tag{7}$$

$$W_c = 2.23 \times 10^{-8}\ (g), \text{ and} \tag{8}$$

$$W_s = 5.63 \times 10^{-9}\ (g). \tag{9}$$

Once the amount of sulfur required to consume copper to the point of failure is determined, the time required for that amount to enter the module can be calculated. Sulfur enters by bulk diffusion through the back seal, and ingress is assumed to be the rate-limiting step for the corrosion process.

The flow area (A) is described as the area of that part of the module between the substrate and the aluminum cap, as shown in Fig. 8:

$$A \approx 4ag = 1.12 \times 10^{-1}\ cm^2.$$

Assuming that there is zero concentration on the back side of the film, the diffusion is described by Crank [11] as

$$\frac{Q_t}{\ell C_2} = \frac{Dt}{\ell_2} - \frac{1}{6} - \frac{2}{\pi^2} \sum_1^\infty \frac{(-1)^n}{n^2} e^{-Dn^2\pi^2 \frac{t}{\ell^2}},$$

where

Q_t = total quantity of diffusing substance per unit area = $W_s/A = 5.03 \times 10^{-8}\ (g/cm^2)$,
C_2 = concentration of diffusing substance at entrance face (g/cm^3),
D = diffusion coefficient (cm^2/s),
t = time (seconds), and
ℓ = seal thickness = 0.20 cm.

From the work of Berry and Susko [10] on the diffusion and solubility of sulfur in polymeric materials, the remaining variables have been determined as

$C_2 = 6.04 \times 10^{-6}\ g/cm^3$,

$D = 2.0 \times 10^{-11}\ cm^2/s$, and

$$\frac{Q_t}{\ell C_2} = \frac{5.03 \times 10^{-8}\ g/cm^2}{2.0 \times 10^{-2}\ cm \times 6.04 \times 10^{-6}\ g/cm^3} = 0.042. \tag{10}$$

From Memis [10], then,

$$\frac{Dt}{\ell^2} = 0.17. \tag{11}$$

This can now be solved for t to determine the time required to diffuse the corrosive quantity of sulfur into the module:

$$t = \frac{0.17 \times 4.0 \times 10^{-2}\ cm^2}{2.0 \times 10^{-11}\ cm^2/s},$$

$$t = 0.34 \times 10^9 \text{ seconds} = 94\,444 \text{ hours}. \tag{12}$$

This analysis assumes that

1. All corrosion is concentrated at one point on the substrate, and

2. The corrosion reaction is instantaneous and directly dependent on the rate of diffusion through the back seal.

While providing a limiting value for life expectancy, this analysis presents the worst case condition. In order to demonstrate that these worst case assumptions were unlikely to occur, an accelerated test was conducted. Modules with 40 lines measuring 0.013 mm and 0.025 mm wide were exposed to an atmosphere containing 800 parts per billion sulfur, 80% relative humidity, at 70°C, and 244 meters per minute air velocity for 1000 hours. The failure criteria were that insulation resistance could not be less than 10^6 ohms and that the line resistance could not increase more than 100%.

The life expectancy was considered to be indirectly proportional to the sulfur concentration, relative humidity, and air velocity of the environment. The relative humidity and air velocity were assumed to be equivalent for test and field. The acceleration factor of the test can then be expressed as

$$A.F. = \left(\frac{RH_t}{RH_f}\right)\left(\frac{S_t}{S_f}\right)\left(\frac{V_t}{V_f}\right)^{0.42}, \quad (13)$$

where

$RH_t = RH_f$ = relative humidity of the test and in the field = 80%,
S_t = sulfur concentration of test = 250 ppb,
S_f = sulfur concentration in the field = 0.1 ppb,
$V_t = V_f$ = velocity = 244 meters/min.

Thus,

$$A.F. = \left(\frac{80\%}{80\%}\right)\left(\frac{250\text{ ppb}}{0.1\text{ ppb}}\right)\left(\frac{244\text{ meters/min}}{244\text{ meters/min}}\right)^{0.42} = 2500.$$

There were no failures, and subsequent failure analysis revealed no observable corrosion. The design was deemed to be extremely reliable in terms of resistance to substrate corrosion.

Conclusion

Successful development of a high performance, fine line, 28-mm metallized ceramic module has demonstrated that the basic 24-mm technology could be extended from a simple wiring vehicle to a sophisticated package with the same advantages of cost, reliability, and ease of manufacture. While process refinements were required to reach the 28-mm module's high circuit density, the basic process remained suitable for volume production.

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D. J. Bendz and J. Rasile are located at the IBM General Technology Division plant, Endicott, New York 13760. R. W. Gedney is on international assignment at P.O. Box 6, Langstone Road, Havant, Hampshire PO9 1SA, England.