## Preface

Among computer designers the term "package" now generally implies all of the hardware used to provide physical support for and electrical interconnection of integrated circuit chips. Thus the computer package includes chip modules, cards, circuit boards, electrical connectors, cables, and frames. The design of a computer package involves both electrical and mechanical considerations, and package designers must also consider heat dissipation. The materials used in computer packages must meet a variety of physical, electrical, and environmental requirements, and the combinations of materials used strongly affect reliability.

Electronic packaging has always been important in the advances made in integrated circuits. But as devices get faster and circuit densities increase, the package has become a major factor in the performance of computer systems as well as in their cost and reliability. For example, IBM has had to develop new packaging technologies for its 4300 Series computers and for the 3081 Processor Unit. This entire issue is devoted to previously unreported IBM work in computer packaging.

Several papers on packaging by IBM authors have recently been published both in the *IBM Journal of Research and Development* and elsewhere. A paper by Seraphim and Feinberg, which reviews the progress in electronic packaging in IBM for the past 25 years, appeared in the September 1981 issue. Two papers reporting aspects of the new IBM technologies appeared in the January 1982 issue: "Thermal Conduction Module: A High-Performance Multilayer Ceramic Package" and "A New Set of Printed-Circuit Technologies for the IBM 3081 Processor Unit." Two closely related papers are "A Multilayer Ceramic Multichip Module" and "IBM Multichip Multilayer Ceramic Modules for LSI Chips—Design for Performance and Density"; both appeared in the *IEEE Transactions on Components, Hybrids, and Manufacturing Technology* in 1980, the former on page 634 in the December issue, the latter on page 89 in the March issue.

Enhanced computer performance cannot be achieved without increased circuit density, which, in turn, requires greater connector density. The IBM approach to chip-to-substrate attachment, the C-4 (controlled collapse chip connections), introduced in 1964, was a departure from that taken by the rest of the industry in that it provided an area array of terminals. Its advantages are increased terminal density and exceptionally high reliability, but it limits thermal dissipation since in the majority of designs most of the heat generated by the chip must pass through the C-4 connections to the substrate. Thus, great demands are placed on cooling techniques for these packages. Two papers in the January 1982 issue of the *Journal*, devoted to the 3081 Processor Unit, reported advances made in heat transfer technology for enhanced cooling of LSI packages: "A Conduction-Cooled Module for High-Performance LSI Devices" and "Conduction Cooling for an LSI Package: A One-Dimensional Approach."

This issue of the *Journal* includes papers on IBM packaging technologies as well as papers describing original solutions to packaging problems common to all technologies. The issue is intended to complement the recent papers and with them to provide a comprehensive picture of electronic packaging in IBM at this time.

The first two papers in this issue describe approaches to the design and manufacture of chip-supporting modules for complete high-performance LSI packages.

The paper "Cost/Performance Single-Chip Module" describes the processes used in the manufacture of the module and how its electrical performance and reliability were assessed. The Metallized Ceramic (MC) technology used for substrate fabrication is one of the two basic substrate manufacturing technologies widely used in IBM. The other is the Multilayer Ceramic (MLC) technology used in the Thermal Conduction Module (TCM) and described in the recently published papers mentioned previously.

As device characteristics improve, many of the benefits of Very Large Scale Integration (VLSI) will be lost without significant accompanying advances in chip packaging techniques. In the second paper, "The Thin-Film Module as a High-Performance Semiconductor Package," the authors identify two key requirements for future semiconductor packages: significantly higher wiring capacity and containment of simultaneous switching noise. The authors present a novel packaging approach, which represents an alternative to rather than an extension of the present approaches, to meet future requirements.

The increasing density of circuits on the chips and of chips on the modules generates the need for very high density cards and boards, the next level of package to which the modules are attached. The next three papers treat different aspects of IBM's printed circuit board technology.

The new logic circuit packaging structure introduced in the 3081 eliminates one level of packaging, the card, by allowing the TCMs to be mounted directly on the TCM board, which results in improved circuit performance and higher system reliability. The paper "Advanced Printed-Circuit Board Design for High-Performance Computer Applications" describes the design of this board, including the printed circuitry, the signal distribution characteristics, and the power distribution system.

The TCM board is larger and more complex than any previous multilayer printed circuit board. The manufacturing processes for this board, which feature computer control of hole drilling for enhanced yield, are presented in the paper "High-Density Board Fabrication Techniques." The TCM has 1800 pluggable connectors packed in a dense array. The stringent mechanical, electrical, and reliability requirements imposed on these connectors could not be met with previous designs.

The final paper in this group, entitled "Development of Interconnection Technology for Large-Scale Integrated Circuits," describes the design features of the critical interconnections for the 3081 in the context of their interactions with other system components and the constraints imposed on them by manufacturing processes and environmental factors.

Each of the remaining papers in this issue deals with a particular aspect of LSI packaging that cuts across all packaging technologies.

Certainly one of the most important aspects of packaging is wireability, since increasing levels of integration put the greatest demand for technological improvement on wiring in an LSI package, even over that of devices or interconnection methods. In the paper "Influence on LSI Package Wireability of Via Availability and Wiring Track Accessibility," the authors compare the effectiveness of fixed *versus* "programmable" vias in packages where wires must pass from one package plane to another. Their experimental results provide insight into ways of improving the wireability of subpackages at packaging levels above that of the chip.

Logic partitioning is related to wireability and packaging efficiency. LSI chips have not yet reached a level of integration which allows a complete large processor to be implemented on a single chip. Therefore, system design still requires the interconnection of modular parts. In the paper "Lead Reduction Among Combinatorial Logic Circuits" statistical methods are described that answer such questions as what distributions of possible modular partitions are available within a system and what is a suitable maximum number of circuits for a part limited by the number of input/output terminals.

The package is also becoming the focus of attention in the drive for higher system performance. Higher densities of faster devices, for example, transfer the problem of system delay to the package. Thus the package must be an integral part of the electrical design of a system. The paper "Electrical Design of a High Speed Computer Package" describes a systematic approach for optimizing the electrical design of a packaging system.

The very high circuit densities achieved in some of the IBM packages described in this issue and in earlier papers are made possible in part by our ability to interconnect large numbers of devices on a single chip. This capability results from the use of three levels of metallurgy combined with area array solder terminals. The design and process enhancements used to fabricate IBM's most advanced bipolar chips are described in the paper "A VLSI Bipolar Metallization Design with Three-Level Wiring and Area Array Solder Connections."

The next paper, "Optimization of Indium-Lead Alloys for Controlled Collapse Chip Connection Application," presents the results of a study of the proper indium-lead composition to maintain fatigue resistance for more demanding extensions of the C-4 interconnections between chips and substrates.

The final paper, "Immersion Wave Soldering Process," describes a new soldering technique for advanced printed circuit boards which has several advantages over conventional soldering processes.