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Electronic Packaging Evolution in IBM

A quarter century of innovation in the development of packaging for semiconductors has culminated in the announcement of the IBM 4300 Series of computers and the IBM 3081. This technology has been built on a broad and expanding base starting with packaging for the 1400 Series in the late 1950s. In the next series, System/360, IBM chose to follow a unique approach which employed solder joints for the semiconductor connections, allowing ultimately a higher density and total number of interconnections compared to the rest of the industry. This has driven the packaging at the module level to achieve extremely high density and has led to multichip interconnections and multilayers on this first level of package. The dramatically increasing circuit function at the module level requires area arrays of pins to be able to get enough of them in a small area. Thus the next level (second level) of packaging has likewise been driven to provide many layers of dense interconnections to link to the module pins. New types of plated through holes join the many layers of interconnection. The highlights of the technical approaches which have been developed over the twenty-five-year period are discussed briefly in this paper.

Introduction

The increasing complexity of electronic packaging in IBM in this last quarter century has been driven by increasing integration on the semiconductor chip and the growth of computing power and performance in systems.

Projection of wiring and wiring density for circuits has been treated at various levels of sophistication [1–3] for chips and for packages. The initial empirical approach began in the early 1960s based on the systems that had been built by then. It was shown by Rent [1] that the number of terminals T supplying the input and output to a set of circuit functions was exponentially dependent on the total number of circuits C,

$$T = AC^p,$$

where A and p are constants. In the original evaluation by Rent, A was 4 while p was near 2/3. By using this relationship, it is possible to break up the entire packaging interconnection system into clusters of circuits and into sets of connected interfaces, some of which are pluggable. These are the chips, the modules which may contain one or more chips, the cards, and the back panels (or boards), each of which contains a function or functions. The Rent-like trend line is illustrated in Fig. 1 for input/output terminals *versus* maximum circuits per component.

The length of wire interconnection within these packaging levels increases as the product of the number of terminals of the subsets within the function, the number of interconnections per terminal, and the average length. For example, the interconnection length required on a module is proportional to the product of the number of chips and the number of terminals per chip. One interconnection obviously has two terminals but quite often a terminal can be common to several interconnections. Likewise, several inputs can be connected in common to a transistor. Using these considerations, a statistical interconnection length has been devised which includes the global wiring.

The increasing size of the system causes the global wiring to increase. These global wires are the controls for the functions, data flow for the system, instruction data path, and memory data path.

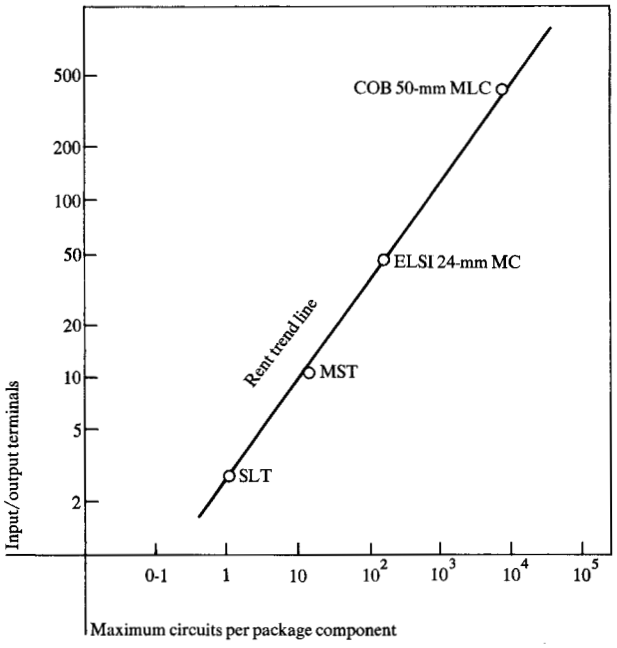


Figure 1 Trend of input/output terminals *versus* circuits on modules.

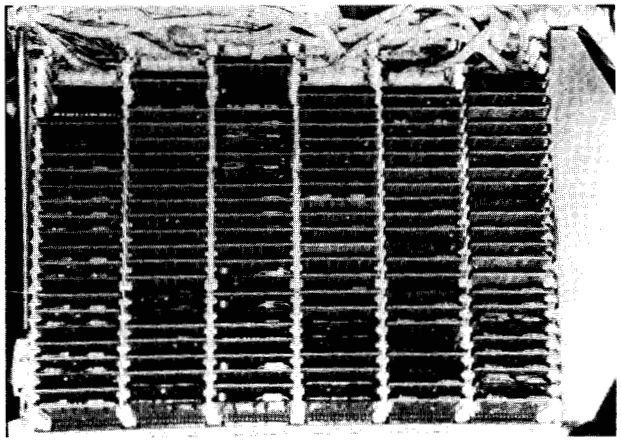


Figure 2 The 1401 System SMS electronic package. Printed circuit cards which are field-replaceable units are plugged into a back panel. The back panel is wire wrap technology.

The thrust for high performance drives the package designer to eliminate factors which delay time of signal propagation or cause excessive capacitive or inductive loading on the circuits. The performance is increased by decreasing the spacing between the components. Indeed, what used to be accomplished on the second level of packaging and in cabling is now better accomplished on the chip or module while the package itself with its dense multilayer interconnection largely replaces the cabling.

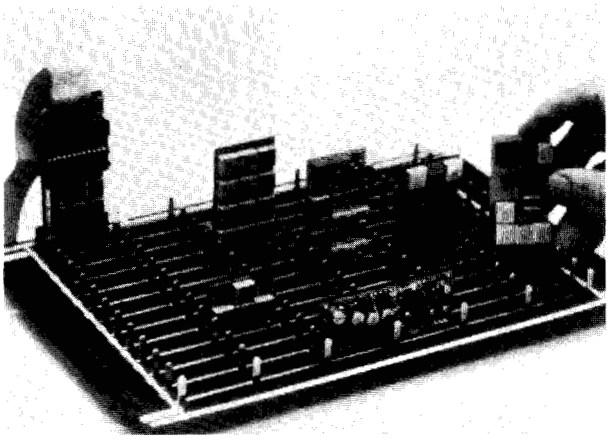


Figure 3 The System/360 Model 30 SLT electronic package. Printed circuit cards plug into a printed circuit back panel. One card can be seen to contain as many as 12 SLT modules.

Over the past few decades the dominant packaging materials have been ceramic with screened noble fritted metal interconnections for the first-level packages (chip carriers) and epoxy-glass composite dielectric with copper interconnections for the second-level packages (the printed circuit cards and boards).

Signal and power grids and interconnections have been greatly increased through the migration of printed circuits from structures which provided one signal plane prior to 1960, two signal planes with one or two embedded power planes in the early 1960s, to today's packaging environment [4–9] where 10 to 20 multilayer designs are commonplace. Accompanying this evolution was the ability to manufacture carriers with increasingly smaller line widths, closer spacings, smaller hole sizes, and greater aspect ratios (aspect ratio equals thickness divided by hole diameter). This has resulted in the use of fewer components and has reduced total packaging costs per circuit in systems.

Cooling the circuits also increases in difficulty as circuits are packaged more densely. The good heat transfer characteristics of silicon in the chips, ceramic in the modules, and copper inner planes in the second-level package, along with a trend toward higher junction temperatures, provided an evolutionary solution to this problem. However, in the latest generation (3081 system) more dramatic innovations, including heat sinks and conduction cooling from the back of chips, have been required [9].

The packaging failure rates have been decreasing by orders of magnitude on a per-circuit basis. The reliability improvement has been made possible through use of

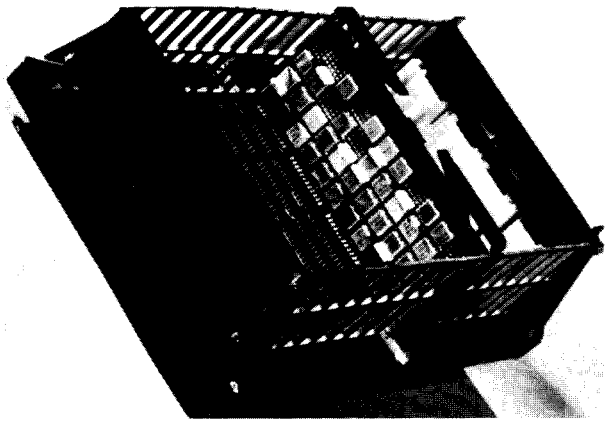


Figure 4 The System/370 Model 148 MST electronic package. Up to 60 modules are mounted on printed circuit cards plugged into a printed circuit back panel.

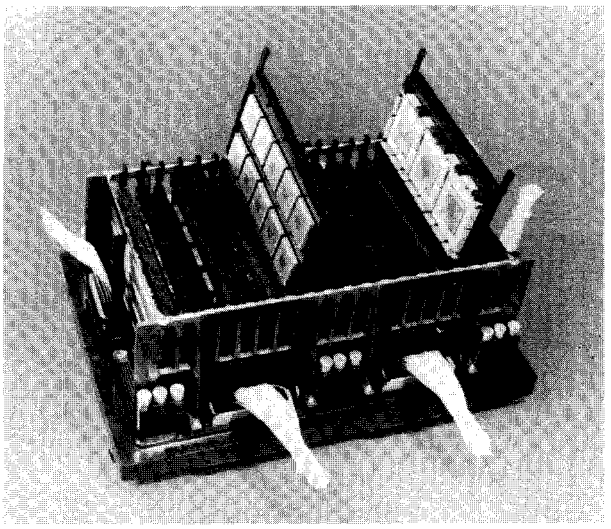


Figure 5 The 4300 Series COB electronic package. Multilayer ceramic modules containing up to nine chips are soldered into printed circuit cards. The cards are plugged into printed circuit back panels.

fewer components and a reduction in the total number of contacts between components. Because of this trend, field maintenance strategy has evolved to handle larger field-replaceable units (FRUs). Thus, quite large systems like the 4300 Series, announced by IBM in 1979 [6], provide all interconnection on one printed circuit back panel containing 16 planes. This entire back panel is a FRU, as are the printed circuit cards.

In this paper we describe the progress in IBM in developing the chip carriers, show the progress in construction of printed-circuit back panels, and discuss the innovation in pluggable contact systems. From time to time we will reference the industry as a benchmark. This era covers computer systems from the IBM 1401 Series through IBM System/360, System/370, 4300 Series, up to the 3081. The overall systems packaging concepts are shown in Figs. 2 through 6.

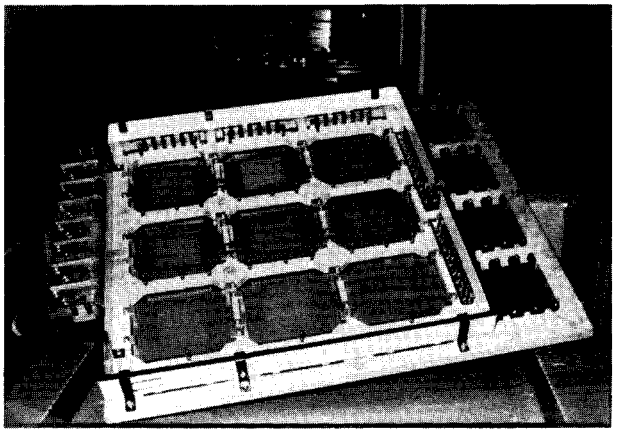


Figure 6 The 3081 System large planar board. Large Thermal Conduction Modules (TCMs) plug directly into the printed circuit back panel.

First-level packaging

- *Chip carriers for single devices*

The functions of the first-level package (or module) as a chip carrier are to provide the proper mechanical, thermal, and electrical environment while interconnecting the chip terminals and providing pins as a means of interfacing to the next level of package.

The first chip carriers were small single-device carriers, hermetically sealed metal cans with chips wire-bonded to a ceramic base, glass-sealed, TO-5 or the like, and these were inserted and soldered directly into the next card level of package, as were the resistors, capacitors, and other discrete components. The next level of package integrated these into a pluggable functional circuit containing 6 to 15 transistors and as many resistors. This first- and second-level package [10] in IBM in the late 1950s was called the Standard Modular System (SMS) and was made from paper epoxy containing etched copper circuitry on one side.

- *Carriers for single circuits*

In 1964 IBM introduced Solid Logic Technology (SLT) [11], which integrated the semiconductor and resistor

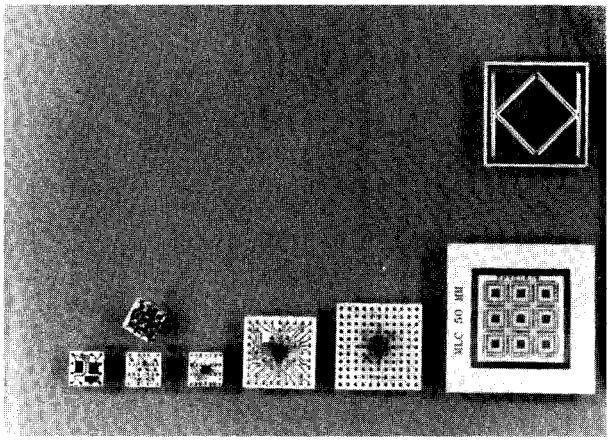


Figure 7 Progress of chip carriers developed by IBM in 1960 to 1980: chip devices per carrier increased from one to nine, pins per carrier increased from several to hundreds, circuits from less than one to thousands.

Table 1 Chip packaging: SMS compared to SLT.

SMS	*SLT*
Chip face up	Chip face down
Wire bond interconnection	Solder bond interconnection
Cooling through back bond	Cooling through solder interconnection bonds
Discrete resistors	Screened frit resistors
Hermetic seal	Glass seal on chip, cap crimped to module, plastic seal

components, providing the set of circuit functions desired, on a very small [12.5 × 12.5-mm (0.5 × 0.5-in.)] ceramic substrate which was exceptionally well suited for mass production. One of the main differences between SLT and its predecessor SMS was the introduction of a module to interconnect individual devices to form a circuit. These modules are called hybrid integrated circuits. The individual devices in the modules were not separately housed in their own package as were SMS devices. Thus, a comparison (shown in Table 1) of SLT chip carriers (or modules) with SMS chip carriers highlights what was new when IBM developed SLT and where IBM diverged from the approaches used by the rest of the electronics industry.

This was the beginning of a unique technology base which broadened (Fig. 7) in subsequent generations as the demand for more chip connections increased. The SLT module in effect replaced the SMS printed circuit package card noted above. The module contained one circuit, as did the SMS card.

The SLT module [11] was a pressed ceramic part with holes preformed for pins. This was a new and unique ceramic formulation with the required strength to withstand pinning operations and the surface texture to meet the requirements of screen printing. It was screened with an interconnection pattern of gold platinum paste containing a small amount of glass for adhesion. The paste formulations were designed for bond strength and electrical conductivity. The sintered paste interconnection was solderable, allowing metallic wetting to the pins and between the paste interconnection and the chip. The solder enhanced the conductivity of the interconnection and provided sufficient ductility for fatigue life of the chip joint. Gold- and nickel-plated copper balls between the chip and the module [12] created a positive stand-off to guarantee a soldered thickness for favorable fatigue behavior.

A wide range of resistor pastes were formulated to meet pretrimming ohmic requirements. They were monitored through the pins while they were automatically trimmed by removal of material to a required resistance.

The semiconductor chip devices were automatically oriented by the configuration of the terminals while they climbed a set of tracks in a vibrating bowl. They were picked up, tested, positioned, and soldered to the module interconnection patterns in one automatic machine. A solder melting point hierarchy for lands and pins was developed so that chips could be joined and modules later soldered into printed circuit cards without affecting the chip bonds.

The module was finally encapsulated with a coating of silicon gel and placed in a crimped can with a silicone rubber filler poured into the periphery as a back seal. Corner pins were swaged to provide positive and controlled stand-off when soldered into printed circuit cards.

This packaging hierarchy which built terminals and passivation into the device at the wafer level, combined with automatic chip joining to modules, resulted in a very high production capacity compared to that of conventional wire bonding techniques. The glass-passivated chip devices not only made the ultimate product reliable but also made it possible to utilize an active solder flux, and, more importantly, allowed the use of a plastic (nonhermetic) seal for the module. The designs, process, and tools achieved very high yields. For example, module yields from chip joining to shipment were greater than 95%.

• *Chip carriers for integrated circuit chips*

It was possible in 1969 to integrate up to 20 circuits on a Monolithic Systems Technology (MST) chip. Accordingly, the chips grew in size and required up to 16 terminals for an average use of 6 or 7 circuits per chip. Copper balls used in SLT as terminals for the chips were then replaced with an evaporated solder joint, controlled collapse chip contact (C-4) [13, 14], which drew the chips into place by surface tension, allowing tighter interconnection tolerances and also affording a fatigue-resistant interface to the module. The height of the C-4 solder pad (a critical parameter in the fatigue-resistant design) was controlled by the volume of solder and the pad area screened on the module [15]. This pad area was defined by the line width and a solder dam of screened and sintered glass frit crossing the interconnection line. The solder was partly supplied by wave-soldering the surface of the module, but the majority was supplied with the chips. For the first time, area array connections were made between the chip and the module to provide improved power supply to the center of the chips. The interconnection of the module was fanned out to an area array of pins.

For memory use it was possible to interconnect four chips on a substrate and stack two substrates. This provided very aggressive densities and substantial savings at the higher levels of packaging. The manufacturing techniques used for SLT were adaptable, with further developments, for MST and memory technology.

By 1973 Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and bipolar device integration on semiconductor chips had reached 100 to 200 circuits, requiring up to 76 interconnection pins on the modules. To minimize the module size, a 9 × 9 array of pins was supplied in a one-inch-square area. Center locations were left free of pins to make room for the chip site. The refined patterns and tolerances resulting from photolithographic technology (described below) allowed a double row of C-4 pads to be used around the perimeter of the chip; power distribution could also be supplied on the module to the center of the chip. This was beyond that achievable with the tolerances from one layer of screened-frit thick-film technology.

A new and extendible evaporated thin film (composite CrCuCr) on ceramic substrates was devised to supply all of the functions. The bottom layer of Cr acts as an adhesive to the ceramic while the top layer of Cr acts as a solder dam. The copper interlayer is superior in conductivity compared to its paste predecessor and is also a better base for soldering. An automatic 5× projection printer is used to define the interconnection pattern in the photoresist. A wide range of part numbers is easily adapted to the automatic exposure system. The general scheme initiated in SLT for chip orienting, locating, and joining was extended to meet mass production requirements.

A new epoxy back seal [16, 17], much less permeable than silicone rubber, was developed for the module. This seal design provides a compliant connection between the cap and the ceramic substrate, which have substantially different thermal expansion coefficients.

While IBM pursued the metallized ceramic (MC) approach, the dual in-line package (DIP) became the standard of the industry through actions taken by the Joint Electron Device Engineering Council (JEDEC). The lead frame pins along the two edges of the DIP used to package vendor chips were compatible with the standard 100-mil grid used by IBM. The DIPs were used extensively along with the MC. The DIPs were available either as plastic packages or as ceramic packages. However, while IBM was able to integrate freely to 76 and 96 pins in a less than 25 × 25-mm array, the DIPs were limited by their practical length dimensions of less than two inches, which allowed only 40 pins on the 100-mil grid on the two edges of the module. The demand for more interconnections brought on an alternative JEDEC industry standard package utilizing all four edges of the chip carrier. These packages, with large arrays of pins, are becoming available in the industry today [18].

• *Multichip-chip carriers for large-scale integration*

Integration has continued to increase, with density growing to 500–700 bipolar circuits and several thousand MOSFET circuits per chip. Thus our Rent relationship (Fig. 1) projects the need for a continued growth in terminals to several hundred. To accommodate this growth the metallized ceramic technology has been extended to 28-mm-square (Fig. 7) and later to 36-mm-square ceramic substrates with finer lines to handle the more closely spaced terminals on the chips.

Finally, the use of chip terminals surpassed the capability to interconnect them on one interconnection layer on a module. At this juncture many new developments were required and a technology change had to be made that could be extended for future generations. Therefore, multilayer module technology introduced a multichip module which reduced the total packaging cost by decreasing the use of higher levels of packaging, *i.e.*, cards, cables, and printed circuit boards. The added process steps of the multilayer technology increased the packaged cost per chip, but this cost was amortized over more than one chip, decreasing the cost per interconnection.

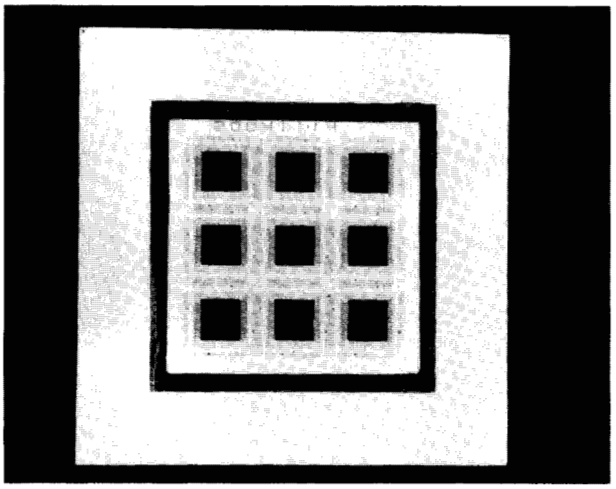


Figure 8 A 50-mm-square multichip multilayer ceramic chip carrier (module) with nine chip sites used in the 4300 Series. The module contains 361 pins solderable into a printed circuit card. This module has a circuit capacity approximately equivalent to 700 of the MST modules (16 pins) used in System/370.

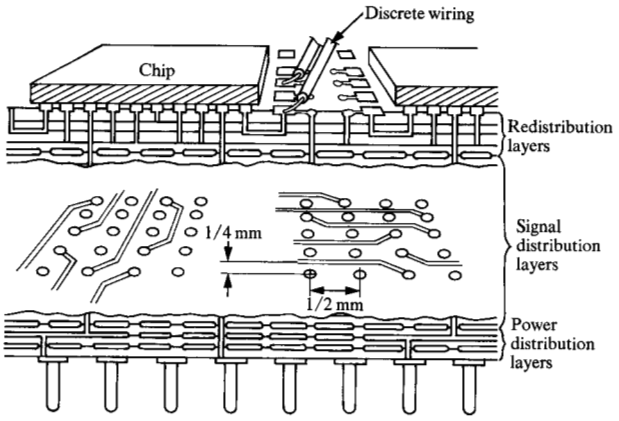


Figure 9 The 50-mm-square module has 23 alumina layers metallized with molybdenum frit. Punched via interconnections between layers are filled with molybdenum frit prior to lamination. The module contains about 500 cm of interconnections.

A 50-mm-square multichip module (MCM, Fig. 8) is used in IBM 4300 Series computers. By utilizing high-density logic devices (up to 704 circuits per device) [7, 8] and a multilayer ceramic (MLC) substrate, this module replaces approximately 700 of the System/370 modules and associated printed circuit cards and hardware.

The MLC module retains and extends the significant feature of the earlier technology, notably area array of pins (361 pins in total) and C-4 solder reflow for the 120 terminals per chip in area array. The new features [19] include the capability of mounting nine chips, a buried wiring and power distribution using screened molybdenum lines and paste-filled vias, the ability to rework or make an engineering change in the internal wiring nets, and the ability to replace chips. Still another feature is the provision of pads for probing and testing. To achieve these features a total new metallurgy structure has been developed. A sketch of the substrate showing the design features is provided in Fig. 9. The total substrate thickness is approximately 4 mm.

Recent introduction of very large systems increases the practicality of complex multichip carrier technology [9]. The trend line for circuits per square cm of ceramic for IBM products is shown in Fig. 10.

As pointed out in [7, 8] there is a 20× reduction in interlevel connections for the MCM technology compared to System/370 or MST technology. This plays a major role in improving circuit reliability. Also there is a 30× reduction in the total wiring length for the same function. This wiring length reduction is a key factor in improving machine cycle time.

- *Cooling*

The increase in integration at the module level has been accompanied by significant increases in power densities there. For example, based on chip carrier area, the power density (heat flux) in System 1401 was only 0.03 W/cm^2, while on SLT it increased to 0.1–0.3 W/cm^2. An innovative hybrid cooling system using water as secondary cooling near the back panels and a push-pull air scheme was developed for handling large-scale computers such as System/360-91/85/195 which used the SLT technology. In this case the air was cooled in the column behind the boards as heat was introduced by the components. In addition, cold plate cooling technology for power supplies was developed. Augmentative heat transfer techniques using turbulators to improve module coolability on the card level were also developed.

Present-day power densities for the 50- and 35-mm MLC modules are in the range of 0.4–0.6 W/cm^2. This has created new challenges in cooling the chip at the systems level of packaging. These challenges were met by incorporating more sophisticated heat transfer and fluid dynamics techniques in the design and detailed thermal and hydrodynamic characterizations of packaging at all levels. Air velocities higher than those previously used became possible through improved package and system hydrodynamic designs. Analytical tools were developed to predict the thermal performance of each chip in the package. Performance was specified in terms of chip

junction temperature as a function of chip technology, chip location on the substrate, substrate technology, module construction, module position on the card, card position on the board, air flow rate and distribution, packaging peripheral hardware, etc. This chip temperature mapping in a system was necessary to ensure compliance with device maximum allowable operating junction temperatures and to establish realistic circuit and system functionality and reliability projections [19].

Second-level packaging

- *Printed circuits and assembly for SMS*

The interconnection for SMS components in 1960 was created by screening resist onto and then etching patterns into a thin copper layer on paper-epoxy laminate. This highly developed art, incorporating 0.25–0.50-mm (10–20-mil) line widths, was later equaled and used in the printed circuit industry well into the 1960–1970 era.

The components were automatically inserted and soldered into place for SMS. The machine for wave soldering was the first of its kind in 1957 and was capable of soldering over 100 000 single SMS cards in one three-shift day. The high throughput of defect-free solder joints was made possible by the oxide-free wave and the cleanliness of the surfaces generated by honing with a high-pressure jet of water containing silica particles followed by proper fluxing.

- *Printed circuits for SLT*

The demand for interconnection rapidly accelerated with the introduction of Solid Logic Technology (SLT). As noted earlier, the number of interconnections is proportional to the number of pins to be interconnected, while the length per interconnection is proportional to the spacing between the modules. Thus, economy in length and total interconnection capacity is achieved by making the spacing of module centers as nearly equal to the size of the chip carrier as practical while maintaining handling and placement capability. Since handling and placing the modules in SLT was aided by the pins slipping into place in a matched grid of holes in the cards, a high packaging density was achieved by allowing (thus wasting) only one grid site (one row of holes) between modules.

Interconnection of a 12-module-card FRU, with up to 12 connections per module (including power) and external interconnections of 24 connections per card, required a multilayer printed circuit technology with two interconnection planes and two power distribution planes. A back panel (a printed circuit board) of the same construction was used to accept six of the cards with 24 contacts in the width dimension and 78 cards total (Fig. 3). Later, wider

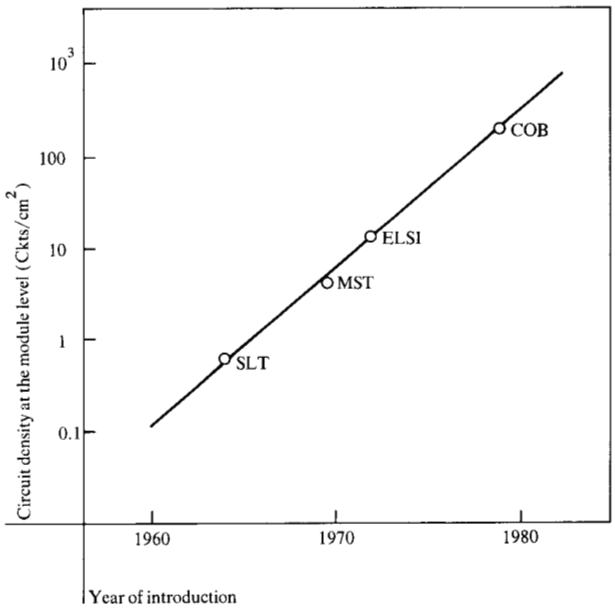


Figure 10 Circuit density trend with time.

cards with 96 terminals were developed. The gold-plated pins in the boards were square-formed to allow wire wrapping for additional wiring and engineering changes.

The material used for the insulation of the multilayers was epoxy-impregnated glass cloth. For this system the formation of a high-function resin system [20] was implemented in 1962. The resin was optimized for the rigors of a sequence of mechanical and chemical processes: lamination, drilling, stripping of photoresist, hole cleaning, etc.

The grid [all holes on a pitch of 0.125 in. (0.317 cm)] was standardized for mass production drilling. The Hydropad drilling machine developed in that era is still a standard of the industry. Here the air bearing spindles were scaled down in size and developed into a precision 24-head drill in 1962. Subsequent innovations brought this to 54 spindles.

The drill bit geometry and process was developed to minimize heat and flow of the epoxy. A drill with a very narrow cutting edge margin (2 mils) was used at 0.3 revolutions per mil of penetration. This approach to drilling minimizes the friction and heat produced and does not cause degradation of the laminate at the hole wall.

The alignment technique for automatic handling of the panels and edge location of the glass masks was established. Edge location required a non-chipping, non-wearing hard glass mask.

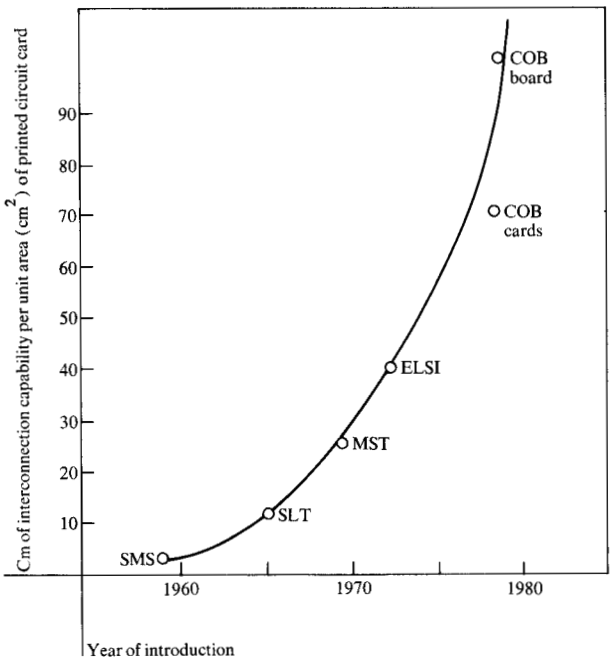


Figure 11 Growth of printed circuit density capability on the second-level package cards and boards. Actual use is limited to about 45% of the capability.

The first printed circuit line production use of photoresist was initiated in IBM in 1959. Difficulties with adhesion were overcome by an oxidizing treatment of the copper surface. This chlorite chemical treatment, which produces about 50 nm of copper oxide, is still widely used throughout the industry for adhesion of organic materials to copper.

The first printed circuit generators for fast turnaround of artwork and direct exposure of photoresist were developed in 1960.

Plated through holes were developed [21] which allowed connection between interconnection planes and/or power distribution planes. Plated through-hole quality increased dramatically with the invention of a new stable electroless copper bath in 1960. IBM engineers [22] discovered appropriate additives which initiated a thin copper deposit with good adhesion.

A new approach was developed for automatic electrolytic plating which is used to make the thick deposit after continuity is established by the thin electroless deposit. While others plated holes and circuitry into resist patterns, a process requiring varied current densities, IBM plated first and then etched the pattern. The standard pattern of holes, rapid liquid circulation, carbon treatment, the high throwing power of the pyrophosphate bath, and thieving to achieve uniform current density established a standard in the printed circuit industry for quality, ductility, and low cost.

This process in 1960 required a photoresist development in the holes to protect the copper while the circuits were etched. A mass production process was implemented using diffuse light and liquid resist which protected holes while the circuitry was being etched. This gave IBM a step up in printed circuit density and decreased the number of process steps needed to construct a printed circuit panel.

The SLT connector design [23] required pins in the boards. An automatic pinner was developed using magnetic nickel (gold-plated) pins which could be oriented vertically in a magnetic field and dropped by vibration into the holes. The use of solder rings (donuts) automatically placed over these pins allowed reflow soldering without deterioration of the gold contact coating.

An engineering change and rework capability used the gold-plated pins for wire wrapping. The printed circuit connection was deleted on the surface with a cutter guided by the pin. This could be done in the manufacturing plant or in the customer's facility.

- *Printed circuits for monolithic systems technology (MST)*

The first MST modules with 16 pins were packaged in 1969. To provide interconnections for 24 to 60 of these modules and the 96 contacts to the supporting printed circuit board required three lines per 125-mil grid and four layers of interconnection. The interconnection line dimensions were trimmed to be as narrow as 5.5 mils. These MST developments were largely refinements, a growth from four layers to six layers, including power distribution planes. This was reduced to a 100-mil grid by 1973 to accommodate the new metallized ceramic modules with 48 to 76 pins per square inch and the vendor DIPs. Full back panels (10 × 15 in.) were made this way with arrays of modules instead of cards. These are called planars. Customized planar packages essentially replaced the card-on-board packages in certain cases because of the high circuit densities that Early Large-Scale Integration (ELSI) achieved in the one-inch areas.

- *Printed circuits for multichip modules*

The increase in wiring demand for printed circuits is shown in Fig. 11. To accomplish the increased wiring for LSI modules, the cards were designed with up to three lines per 2.5-mm channel and four signal layers. Two

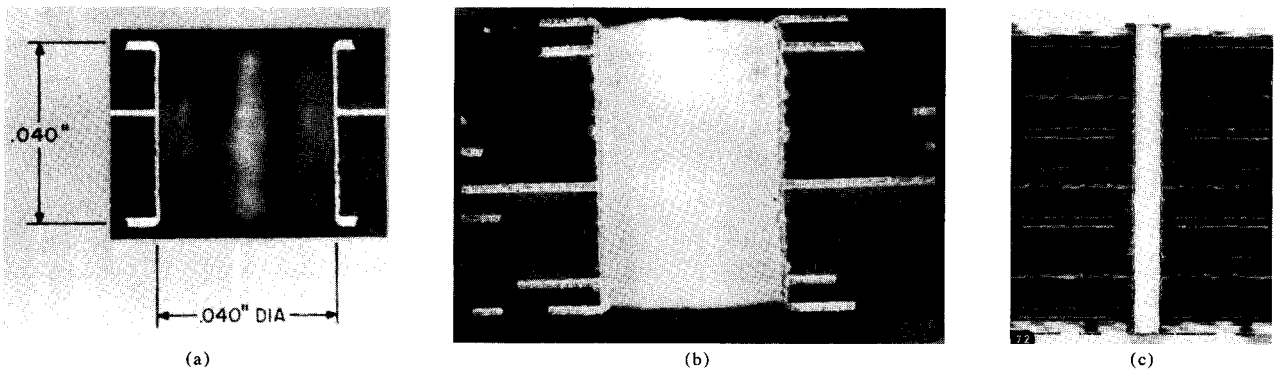


Figure 12 Plated through holes for (a) SLT, (b) MST, and (c) COB. These are 40 mils, 40 mils, and 18 mils in diameter, respectively.

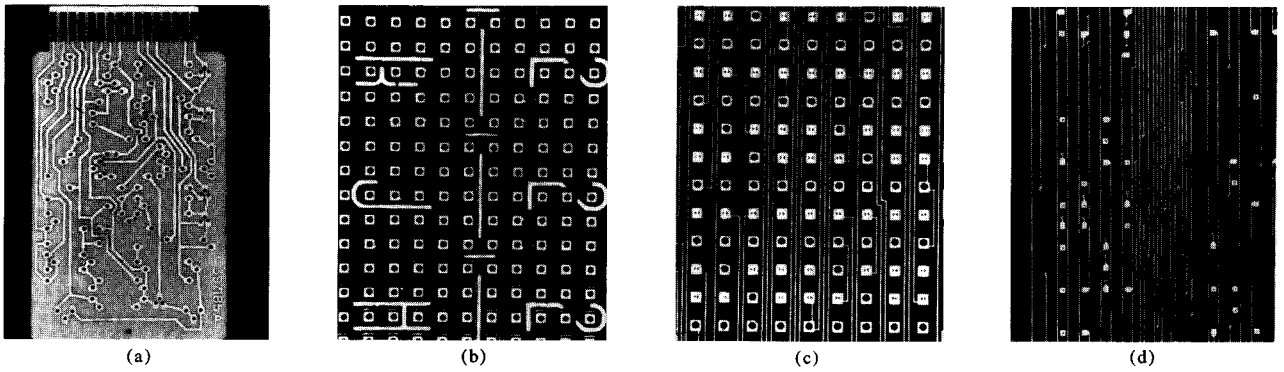


Figure 13 Interconnection line configurations for (a) SMS, (b) SLT, (c) MST, and (d) COB.

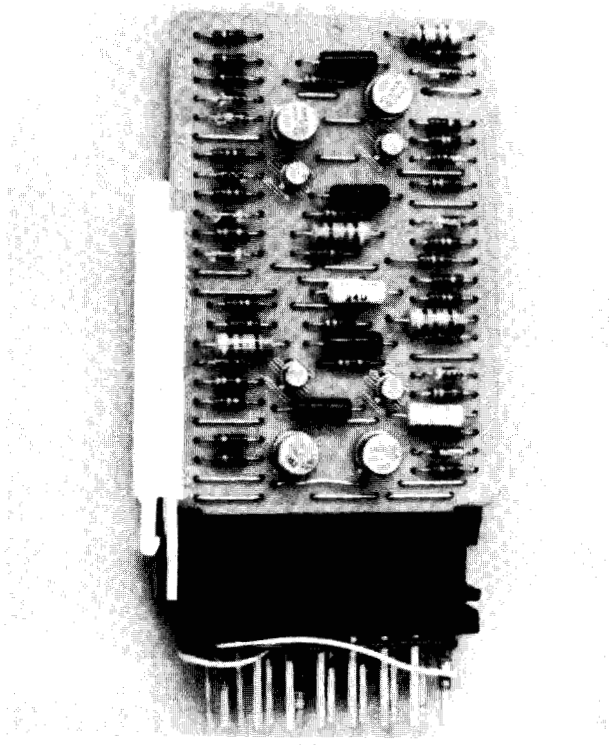
neighboring interconnection layers could be joined with a programmable via. Line widths were reduced to 4 mils.

The back panel was designed to interconnect 18 cards, or roughy 4800 contacts. This required six interconnection layers with four lines per 2.5-mm grid and programmed vias within three pairs of signal layers. The current requirements for some boards reach 200 amps; thus, to minimize voltage distribution variations, eight power planes are required. This new Card-on-Board (COB) package [5, 6] required numerous technology innovations and developments in insulation and interconnection technology.

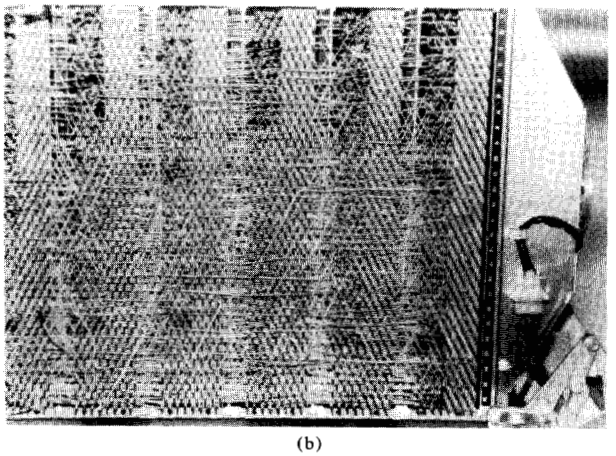
Numerous electroless plating baths have been proposed and are available in the industry, but none of these has been successful in the deposition of high-purity, high-ductility copper comparable to that achievable with electroplating. IBM engineers [24] overcame these difficulties in 1974 after several years of innovation. As a result it is possible to plate into holes ten times as deep as their diameter with constant thickness throughout. The adhesion base for the additive copper plating was developed.

Circuitry is possible with lines as narrow as 0.075 mm and 0.050 mm in thickness [25, 26]. Subsequently, printed circuit boards containing a kilometer of this type of "additive" circuitry have been built on the production line. The progress in plated through-hole technology and in interconnection density is illustrated in Figs. 12 and 13.

The cost of large printed circuit boards containing many interconnections is enough to warrant considerable rework and repair when engineering changes are necessary. Furthermore, flexibility for engineering changes is required while the machine is being brought up and for the addition of certain customer functions. The high performance of the current technology does not tolerate the significant impedance mismatches which would prevail with the use of single wires as in wire wrap technolo-



(a)



(b)

Figure 14 (a) SMS card FRU, and (b) back panel. Gold tabs on the cards mated to cantilevered pins on the back panel.

gy. Accordingly, twisted pair wire technology is used where required. The basic design brings every module connection through the printed circuit board to the opposite surface. There the choice may be made between a surface interconnection which enters a redundant hole connecting to the internal signal planes or an interconnection with twisted pair wires on the surface of the board. In the latter case the surface interconnection between the two holes is deleted.

A low-temperature-melting eutectic solder was developed for use with the larger, more complex modules on the ELSI and COB programs. The low-temperature solder was used for initial wave solder and for reworking all modules larger than one inch to maintain the module temperature as low as possible. This decreased dissolution of copper from the plated through hole and decreased the stresses from mismatch of thermal expansion coefficients of the various components in the packages.

Immersion wave soldering is a new method of soldering that submerges the board in a medium of glycerine, acting as a flux, that preheats a thick board for better through-hole solderability. The board is driven by a conveyor under the glycerine until the required temperature profile is obtained. The solder wave, which is also submerged under a glycerine envelope, prevents solder oxidation.

Connectors

The first functional printed circuits interconnecting discrete transistors, resistors, and other discrete components in IBM were introduced in 1959 as an SMS "card." This is a pluggable FRU card with 16 connector terminals. Gold-plated copper tabs on the paper epoxy served as one of the contacts while cantilevered pins on the back panel, also gold-plated, mated to the gold tabs [23]. This was the first mass-produced contact system for packaging in the industry and introduced the FRU concept along with the back panel (Fig. 14). The array of pins in the back panel, the other end of the contact system, afforded the base for wire wrap interconnection.

Semiconductor technology imposed new requirements on connector designs. Voltage and currents in the interconnections were on the way down. Circuit speeds were moving upward. Circuit elements were being forced closer and closer together. Thus, it became increasingly important to optimize connector design, the manner in which the design is integrated into the electronic package, and the method of tooling and assembly. Mass production was fast becoming a reality in the infant computer industry.

The SMS connector system consisted of a number of cantilevered spring members in the back panel pressing against printed circuit tabs along one edge of the printed circuit card, both elements being gold-plated. The design was simple but effective, although massive by today's standards. The design was successful because it accounted [27] for all the factors usually considered important in connector design.

Contact resistance is the most useful indicator of functionality for the engaged connector. Typically, this value in a gold-on-gold system may be 1 or 2 mΩ or even higher depending on how the measurement is made. Perhaps more important than the actual values are the readings, over a span of time, which measure the stability of the contact system.

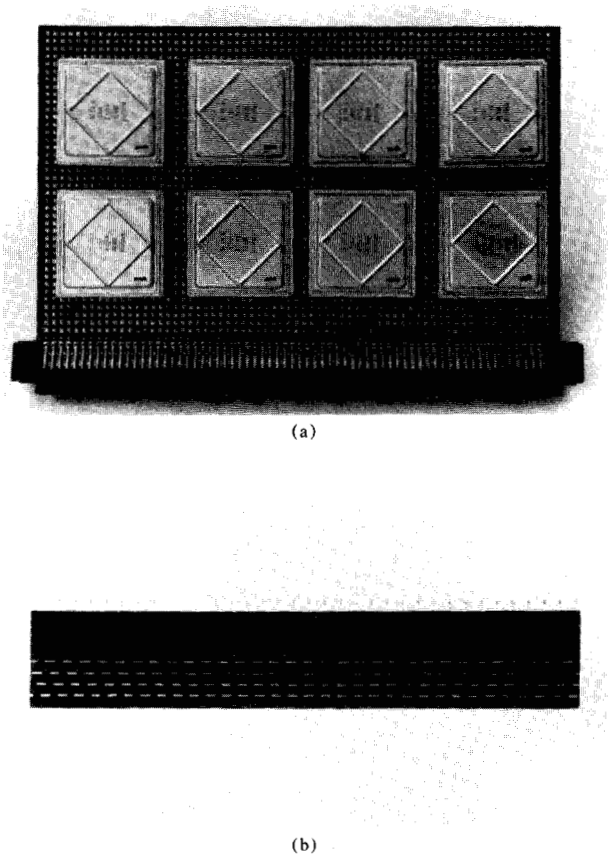
Contact wipe, the sliding movement of one contact member while in contact with its mate, is necessary to ensure clean mating surfaces at the point of contact. The movement while the contact members are under pressure must be sufficient to remove foreign particles and break through thin films of oxides, organics, sulfides, or whatever.

Contact wear or durability must be considered in any application intended for long field life. Wear is unavoidable, of course, where there is contact wipe. In new contacts, wear is of no concern but as the number of engage/disengage cycles increases, so does wear. In time, there is danger of breaking through the protective surface metallurgy to expose the less noble base metals, thus initiating corrosion leading to contact failure. The innovation needed in solving the problem is to optimize the contact geometry, the surface metallurgy, and the forces involved.

Corrosion resistance, which was evaluated for connectors [28–30], is also essential in any practical connector. Gold plating was used extensively in the SMS package beginning in 1959 and has remained a favorite ever since as a means of corrosion control. The gold-to-gold-plated connector system has had a comparatively long run in the otherwise dynamic electronic business.

In the early 1970s gold became increasingly expensive. There was increasing pressure to develop alternative plating metals without sacrificing performance and reliability. In 1973, IBM qualified a palladium-plated pin [31, 32] to be mated with a gold-plated contact. This system was used on the ELSI electronics package, and on IBM System/370 and follow-on systems. In later developments gold usage has been minimized or avoided altogether.

A new generation of the COB and planar packages was required to interconnect larger single and multichip modules in the late 1970s. By this time 28-mm metallized ceramic modules with 116 pins and 35-mm and 50-mm multilayer ceramic modules with 196 and 361 pins were being packaged on cards. This meant that over 1000 contacts had to be made for three of these units on a card and the card connector had to be expanded to 268 contacts (Fig. 15) to supply the increased number of



(a)

(b)

Figure 15 Pluggable card edge connector with 268 contacts for the 4300 Series computer: (a) top and (b) side views.

circuits. Refer also to the Rent trend line (Fig. 1) illustrating the growth of connection density as the circuits-per-package count increases.

A new connector technology [33, 34] was required to accommodate insertion of 268 blades spread over seven inches of the card edge. The tolerances of the mating parts could no longer be independently held to control the spring forces. Thus, an early decision was made to set tolerances by a bifurcated spring in a progressive die and by control of the diameter of the pin. Thus the spring was made as a bifurcated contact system shaped like a "Y." With this design the spring forces could be well controlled in a miniature contact system. Therefore, the direction of the future in low-energy connector design is an extension of reliability through bifurcated contact redundancy. Here the reliability lost in reducing the contact force and size is restored by redundancy in the contact.

Tolerance mismatches between the FRU and the back panel were compensated by the flexible tail on the spring. This system was adaptable to the small pluggable mod-

ules released in 1974 and to the cards with 268 contacts and could be extended to use the largest MLC multichip modules. In the latter case insertion guides were added and a key wrench was required to apply force for insertion.

The production volume for a given connector often plays a major role in determining the design configuration. Increasing usage of computers has pushed the production volumes of connectors (and other components) upward. At the same time, a proliferation of packaging designs has been noted. So, although the total production volume of connectors remains high, there is a continuing demand for many varieties. To offset this splintering effect, designers produce, whenever possible, multipurpose hardware. Thus, a single contact design can often be made to serve in numerous applications. For example, the IBM spring contact discussed here has been applied as a card edge connector, module connector, and cable connector.

Summary

The innovations which have led to the major advances in interconnection density at the chip carrier level of packaging are as follows:

1. Soldered pad interconnections (C-4).
2. Area array pins and area array C-4 pads.
3. Good thermal conducting ceramic substrates.
4. Dense circuit line capability.
5. Multilayer technology with dense vertical interconnection (via) capability.
6. Semihermetic sealing.
7. Engineering change capability.
8. Control of dimensional tolerances over large module areas.

The innovations which have led to the major advances in the interconnection density at the second level of package are the following:

1. Plated through-hole technology.
2. Lamination technology with epoxy-glass dielectric.
3. Photo-printed copper circuitry.
4. Field-replaceable units with connector technology.
5. Noble metal contact metallurgies.
6. Solder assembly using solder waves.
7. Automated wire bonding for reworking and engineering change.
8. Programmable via technology.
9. Control of dimensional tolerances over large panel areas.

These and other innovations described in this paper have allowed circuit densities at the back panel to grow approximately three orders of magnitude in less than three decades. This follows in fact the density growth on semiconductor chips.

Increasing circuit count and density in the semiconductor will continue to place further demands on packaging. There will be constant requirements for increased wireability, lower capacitive loading, and shorter signal propagation times. This will lead to increased densities through small grids and finer interconnection lines, more layers, and vias, and improved dielectric constant materials. The demand for improved thermal capability will follow. The System 3081 packaging concepts are a step toward the future.

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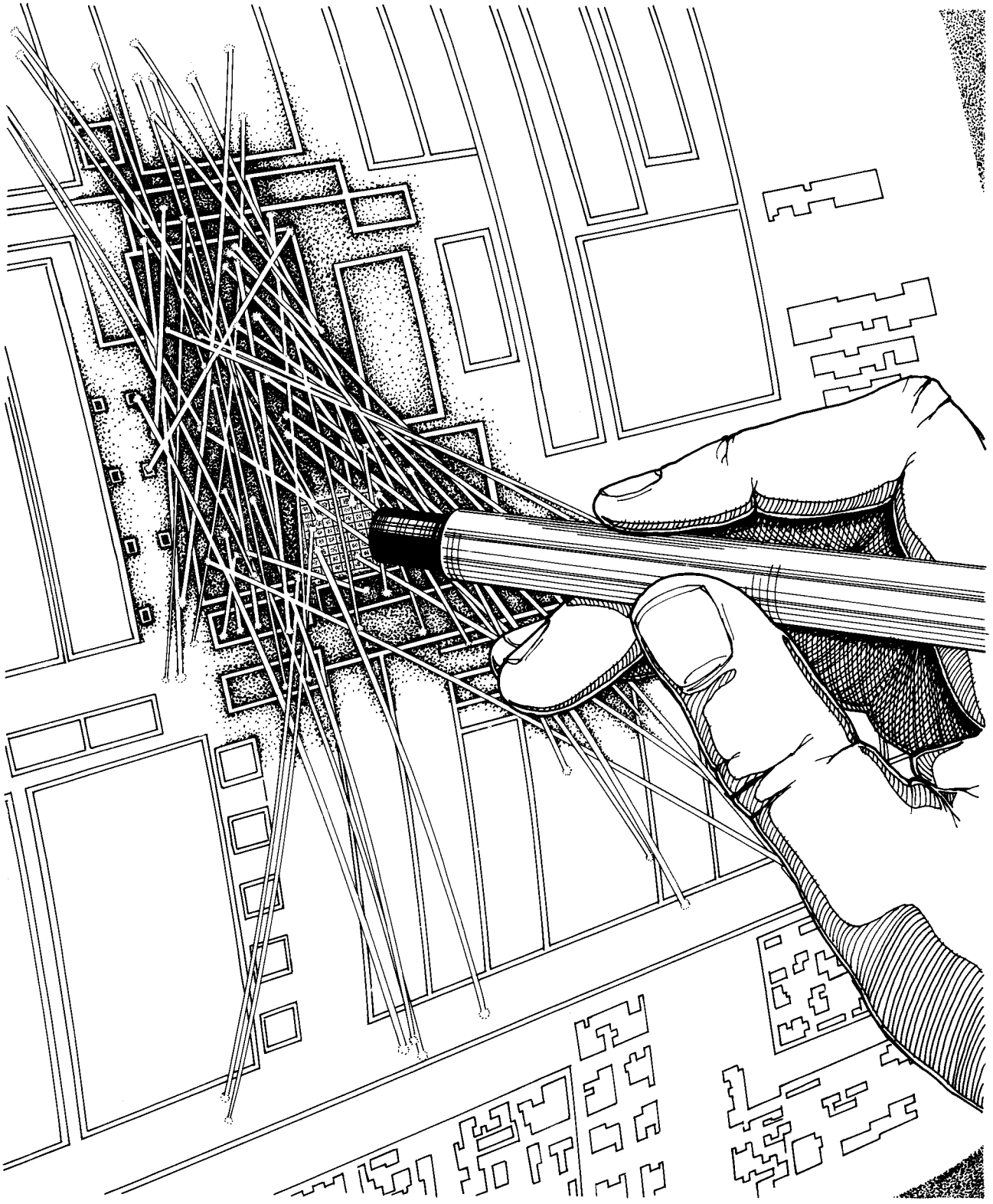

Engineering design system