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Solid State Memory Development in IBM

Memory technology in IBM processors has undergone a 280 000-fold increase in density, a 20 000 times decrease in power per bit, and a 10 to 100 times increase in speed during the last twenty-five years. These improvements have brought many advantages to users of information processing equipment, including a 650-fold reduction in the cost per bit of memory. During this period, processor memory technology evolved from cathode ray storage tubes in the early 1950s, through ferrite cores and thin magnetic films in the 1950s and 1960s, to bipolar and MOSFET semiconductor memories in the late 1960s through the 1970s. This paper describes these developments and the technical innovations that made them possible. It also describes continuing exploratory efforts, including work on magnetic bubbles—the newest solid state memory technology.

Introduction

This paper describes the rapid progress in memory technology which occurred during the last quarter-century and highlights the technical contributions of people in IBM who helped to make it possible.

The earliest device used for main memory in electronic calculating machines was a mercury sonic delay line developed in the late 1940s. This serially addressed memory, in which the contents were continuously circulated, required several milliseconds to read or write information. This was slower than desired, even for the early electronic calculators. As electronic calculators evolved toward stored-program computers in the late 1940s and early 1950s, a substantial improvement in the speed, reliability, and cost of memory technologies was essential because an increase in the speed of a stored-program computer required nearly equal increases in *both* the speed and capacity of the main memory.

A cathode-ray-tube (CRT) memory, invented by Williams [1] at the University of Manchester, England, provided much faster access to stored information. It was

termed a random access memory (RAM) because access time was independent of the memory address. The time required to write or read information was about ten μ s. CRT memories were used in early stored-program computers such as the IBM 701, first shipped in 1953.

The use of magnetic cores for a RAM in computers was independently invented about 1950 by Forrester at MIT [2] and Rajchman at RCA [3], with Forrester eventually being recognized as the earlier inventor [4]. The first main memory using ferrite cores wired in a three-dimensional array as proposed by Forrester was employed in MIT's Whirlwind computer in 1953.

At the same time, MIT and IBM cooperatively developed a core memory for SAGE (Semi-Automatic Ground Environment), a computer IBM manufactured for the U.S. Air Force. IBM also independently designed and manufactured core memories for its 704 and 705 computers, which were first delivered in December 1955 and January 1956, respectively. Whirlwind, SAGE, the ERA 1103, and the IBM 704 and 705 employed the first ferrite

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Table 1 Representative IBM processor memory technologies.

<i>Date*</i>	<i>Processor</i>	<i>Technology†</i>	<i>Cycle time (μs)</i>	<i>Volume/megabyte‡ (m³)</i>	<i>Power/megabyte (kW)</i>
1953	701	CRT (1024)	12	240	980
1955	704	Core (50-80)	12	160	340
1959	7090	Core (30-50)	2.2	13	41
1965	S/360-50	Core (19-32)	2.0	1.5	5.5
1965	S/360-65	Core (13-21)	0.75	11	48
1968	S/360-95	Thin film (4096)	0.12	8.8	23
1971	S/370-145	Bipolar (128)	0.25	0.23	9.6
1973	S/370-145	Bipolar (1024)	0.25	0.028	2.4
1973	S/370-158, 168	MOSFET (1024)	0.46	0.028	1.0
1974	S/370-158, 168	MOSFET (2048)	0.48	0.014	0.36
1979	4331	SAMOS (65 536)	0.90	0.0009	0.05

*This is the date the first processor using this memory was delivered.

†The numbers in parentheses are the number of bits per CRT, per thin film substrate, or per semiconductor chip—or the core size in thousandths of an inch.

‡This is the volume required for the memory array, support circuits, packaging, cooling space, and proportioned share of power supply, regulation, and distribution. The volume is extrapolated for memories having less than one megabyte capacity.

core memories capable of handling the large quantity of instructions and data required by stored-program computers.

Ferrite core memories were soon proven to be faster, cheaper, and more reliable than earlier technologies. By the time the first IBM System/360 computers were announced, IBM had developed advanced memory designs and automated manufacturing techniques capable of producing large quantities of memories at a very low cost.

Numerous research and development projects were undertaken by IBM during the 1960s to identify and develop promising new technologies. Work on magnetic film technology, for example, resulted in the shipment of memories on the IBM System/360 Model 95 computer in 1968 which were five to ten times faster than ferrite core memories. However, development work on ferrite core memories was stopped by IBM early in 1968, and on magnetic film memories in 1969, to permit greater focus on semiconductors. Management had gained confidence in semiconductor memories following the innovative use of a small, high-performance monolithic semiconductor memory as an automatic buffer (cache) for a large, low-cost ferrite core memory on the IBM System/360 Model 85 processor.

With its memory development resources focused on semiconductors, IBM was able to deliver the world's first commercial computer with an all-semiconductor main memory in June 1971, the IBM System/370 Model 145. This multi-megabit memory was composed of bipolar semiconductor chips less than one-eighth of an inch (3.1 mm) on a side, each with 128 bits. In April 1973 the IBM System/370 Model 158 computer was shipped with

the first main memory to use the lower-cost MOSFET devices. The first version had 1024 bits per chip and 2048 bits per module. The n-channel technology pioneered by IBM in these devices provided 50 ns access at the chip and 150 ns access to a twenty-million-bit memory system. Within a few years, monolithic semiconductor memory technology had become standard in the industry. In 1979 IBM began shipping a new semiconductor memory product with over 65 000 bits per chip—the largest number of bits per chip achieved in any system to that time.

A number of IBM processor memory product technologies are listed in Table 1 and serve to illustrate the dramatic improvements which occurred during this period. Among the many important advantages for the user was a reduction in monthly rental per bit of memory from 3.5¢ for the CRT on the IBM 701 to 0.0054¢ for the MOSFET technology on the IBM 4331.

Ferrite cores

Information in ferrite core memories is stored by the clockwise or counterclockwise direction of the magnetization around the hole of each donut-shaped ferrite core. These two magnetization states represent the logical "1" and "0" of digital computer information and can be switched by the coincidence of the currents in wires through the hole in the donut-shaped core. In three-dimensional (3D) arrays, cores are to switch only under the influence of positive polarity current pulses on the X and Y wires and the absence of a negative (inhibit) pulse on the Z wire during a write operation, and under the influence of negative current pulses on the X and Y wires during a read operation [2]. To operate reliably in this mode, the cores must switch when acted on by this combination of current pulses and must remain undis-

turbed when acted upon by a large number of current pulses of any other combination. Cores which satisfy this requirement are said to have square loops because a plot of their magnetization on the y axis and applied current pulses on the x axis has a square or rectangular shape. In early memory designs, a fourth (sense) wire through each core was used to detect the output voltage induced when a core was switched. Later designs used one of the drive wires for this function.

• Initial developments

Early successful cores used the magnesium-manganese (Mg-Mn) ferrite material invented about 1950 by Albers-Schoenberg of General Ceramics [5] or the copper-manganese (Cu-Mn) ferrite material invented by Beck and Matteson of Philips [6]. An effort directed by J. W. Gibson of IBM was successful in producing Mg-Mn cores for the SAGE, 704, and 705 memories. However, because of difficulties in acquiring a second source for cores of this composition, IBM began a cooperative effort with Philips on cores of the Cu-Mn composition. This composition was used in 98.7% of all the cores produced for IBM memories.

A major improvement in the quality and uniformity of cores was achieved by Brownlow of IBM in 1956 [7]. He achieved a specific oxidation state by rapidly quenching the cores from an elevated temperature to room temperature during the sintering cycle. Concurrently, Gibson and Schuenzel of IBM and Bleyenbergh, DeRooy, and Dam of Philips discovered that presintering of the material prior to pressing plus a two-step sintering technique in which the cores were first sintered at a high temperature and then at a temperature a few hundred degrees lower significantly improved the characteristics of Cu-Mn cores [8].

IBM and MIT jointly designed rotary press tooling to form the donut-shaped toroidal cores for the SAGE computer. In 1954 these machines were able to form cores at a rate of 30 per minute. This rate was increased to 6144 cores per minute by 1966 as the result of an evolutionary development of rotary press designs by IBM. During the same period, the outside diameter of cores used in products was reduced from 80 to 21 mil (thousandths of an inch; *i.e.*, 2 to 0.5 mm) in order to reduce drive current and power requirements.

The first of IBM's core planes were fabricated by soldering the copper wire to a steel needle which was then manually probed into a dish filled with cores to place them on the wire. These wires, loaded with cores, were soldered to terminals on a frame, and the other three groups of wires were hand-threaded. Then persons at

MIT conceived a technique that automatically positioned the cores for wiring by air flow through holes in the bottom of a matrix of cavities. Shaw and Link of IBM invented the technique of using hollow steel needles which were strong enough to be simultaneously threaded through 64 columns or rows of cores in the matrix [9]. The weaker copper wires were inserted through the hollow needles; when their ends protruded, they were grasped and the needles were withdrawn. IBM implemented this wiring concept in 1955; it reduced the time to thread the X and Y wires in a 64×64 plane from 25 hours to 12 minutes. Shaw and Judge of IBM devised a mechanism which grasped the X and Y wires after they were threaded and wrapped them around terminal posts on the plane frames [10]. The time for this operation was thus reduced from 2.5 hours to half a minute.

The generation of X, Y, and Z current pulses was a major challenge; currents of $1/4$ to $3/4$ A with rise times on the order of $0.1 \mu\text{s}$ were required. Rajchman of RCA invented a two-dimensional matrix of transformers made with rectangular hysteresis loop cores which reduced the number of vacuum tubes for generating the X and Y currents by a ratio of $2\sqrt{n}/n$, where n is the number of X or Y windings [11]. An improvement of Rajchman's concept invented by Bloch of IBM reduced the magnitude of spurious output currents [12]. Bloch's switch-core-drive matrix concept was used in many memories, including the 12- μs -cycle, 4096×36 -bit memory shipped on the IBM 704 in December 1955 [13].

Of the early IBM core memories for commercial computers, the fastest was for the 705 computer; it had a cycle time of $9 \mu\text{s}$ and a capacity of 4000×35 bit words [14]. The noncommercial 4096×33 -bit memory completed in 1955 for the SAGE system had a cycle time of only $6 \mu\text{s}$. All were made with cores of 80 mil outside diameter (OD) and 50 mil inside diameter (ID) (2 mm OD and 1.3 mm ID).

• The next generations

In 1958 IBM announced two new memory products: the 7301, for the 7070 processor, with a maximum capacity of 9990 53-bit words and a cycle time of $6 \mu\text{s}$ (later reduced to $4 \mu\text{s}$), and the 7302, for the 7030 (Stretch), 7080, and 7090 processors, with 16 384 72-bit words and a cycle time of $2.18 \mu\text{s}$ [15]. The core ID-OD was reduced from 50–80 mils (1.3–2 mm) to 30–50 mils (0.8–1.3 mm), and magnetic characteristics were changed to accomplish faster switching speed with approximately the same drive current. With the increase in speed, the drive and sense windings had to be terminated with resistors equal to their characteristic impedance of 100 to 200 Ω . The termination in characteristic impedance was needed in order to

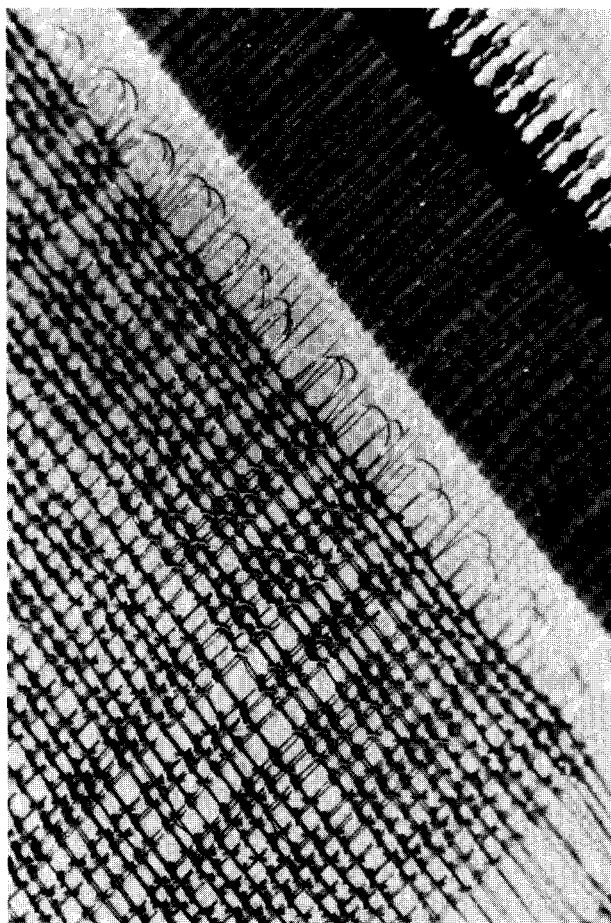


Figure 1 Photograph showing the edge of a 7302 territe core plane with 19-32-mil (0.48-0.81-mm) cores. This had a 2- μ s cycle and was used on the IBM 7094 computer.

eliminate pulse-shape distortion. This increased the X, Y, and Z drive-pulse peak power by about a factor of ten, and the rise and fall times of the drive pulses had to be reduced. To satisfy these requirements, IBM developed a medium-power, graded-based transistor which produced 60-V 0.6-A pulses with rise and fall times of 0.1 μ s [16].

With this transistor, the Z windings could be driven directly. However, this was not possible for the X and Y windings because of the opposite-polarity read and write currents. The load-sharing matrix switch, invented by Constantine of IBM, provided a very attractive solution to this problem [17]. It combined the currents of several transistors to collectively provide the drive for a single X or Y winding. A switch having n outputs requires $2n$ drive transistors as in a simple transformer drive approach; however, the power requirement of each transistor is reduced by a ratio of $1/n$.

Another improvement was the change from a diagonal sense winding to one that is parallel to the X or Y windings. This not only reduced sense-winding attenuation and delay, but it also helped lower the drive power requirements. An invention by Crawford of IBM further reduced the distortion, attenuation, and delay of sense-winding signals by dividing each winding into two halves and terminating each with resistors equal to the characteristic impedance [18]. The improvement in IBM's second-generation core memory technology can be gauged by the fact that the first 7090 memory had eight times the capacity for only three times the price of the earlier 704 memory. It was also six times faster and had approximately a tenfold improvement in density and power per bit, as revealed in Table 1.

The 7302, as initially designed, had the array immersed in transformer oil to remove heat from the cores. A new design, completed in 1962, eliminated this requirement by the use of a core with smaller ID-OD, 19-32 mils (0.48-0.81 mm); see Fig. 1. The cycle time was 2 μ s, and in 1964 that was reduced to 1.4 μ s for use with the 7094 II computer. Two special memories having 1024 72-bit words each and a cycle time of only 0.7 μ s were built in 1960 for the IBM supercomputer HARVEST. These memories used the same cores as the 7302s, but they employed a two-dimensional, two-core-per-bit, partial-switching storage array [19].

All the IBM System/360 processors benefitted from advances in core memory technology achieved in the mid-1960s. The 19-32-mil (0.48-0.81-mm) core developed for the air-cooled design of the 7302 memory was used in the moderately high-speed memories. An invention by Flaherty, Hallstead, Judge, Vaudreuil, Wyckoff, and Schug of IBM significantly reduced the problem of wiring cores into planes by permitting the same wire to be used for inhibit drive and sense output [20]. Thus, only three instead of four wires had to be threaded through each core. The resulting memories had cycle times of about 2 μ s and a maximum capacity of 1 179 684 bits per array. The same designs were also used for IBM's first System/370 processors, the Models 155 and 165.

A new 13-21-mil (0.33-0.53-mm) core was developed for the highest-speed System/360 memories. These memories also used only three wires through each core. A cycle time of 0.75 μ s was achieved. Maximum capacity memories (32 768 $\times$ 72 bits) used Constantine's load-sharing matrix switch for driving the X and Y windings. Smaller-capacity designs used "floating" transformer output windings connected to X and Y windings through semiconductor diode matrices invented by Sommerfield, Norton, and Cooper of IBM [21]. This significantly

reduced the number of drive transistors. Cycle times of memories using this drive technique were in the 0.9–1.5- μ s range.

The System/360 memory designed for maximum capacity and lowest cost per bit was the 2361, announced in 1964. It used a 2½-D concept and provided 252144 72-bit words and a cycle time of 8.0 μ s. Low cost was accomplished by the use of very large (256 $\times$ 1152-bit) core planes with only two wires threaded through each core. The invention by Thome of IBM provided the means for doing this by utilizing the same wire for both the drive and the sense functions [22].

- *Final developments*

A 110-ns-cycle memory was built by Werner, Whalen, Lockhart, and Flaker at IBM in 1966 with a capacity of 8192 72-bit words [23]. It was a 2D design employing 7.5–13.3-mil (0.19–0.34-mm) cores. This memory used the two-core-per-bit partial-switching technique previously used in the 0.7- μ s HARVEST memories. One important difference was the use of a ground plane which was placed close to the windings and thereby reduced and controlled their impedance. This memory was not placed in manufacturing because of the higher performance projected for magnetic film memories.

In the late 1960s another advanced core memory was developed for IBM's commercial computers by Councill *et al.* [24]. It had a capacity of 16 384 18-bit words and a cycle time of 275 ns. This was a 3D memory using 8–13.4-mil (0.20–0.34-mm) cores with a switching time of about 50 ns. The array and drive circuits were immersed in an inert fluorochemical liquid to prevent overheating.

The project also produced a better means of testing and wiring cores. A machine invented by Baker, Cadwalader, and Marinelli of IBM, which grasped the cores on the outside and placed them on one of twenty-five probes, was implemented in 1968 [25]. It increased the test rate to 180 cores per second. A scheme developed by Hazel and Mueller tested the cores during the wiring operation [26]. Unsatisfactory cores were broken and removed, the last wire that threaded them was withdrawn, and substitute cores were moved into the same positions. This avoided the expensive operation of cutting and splicing wires to remove faulty cores.

The 275-ns-cycle ferrite core memory developed for IBM System/370 requirements was technically successful; however, development of manufacturing tooling was stopped in January 1968 because of the expectation that semiconductor memories and magnetic film memories would soon provide superior cost and performance. Nev-

ertheless, ferrite cores had provided the most satisfactory processor memory technology for IBM over a period of nearly two decades—a period during which digital computer logic made the transition from vacuum tube to transistor to integrated circuit technologies.

Magnetic films

The first experimental magnetic core memories used ceramic bobbins about which thin metallic strips of ferromagnetic nickel-iron were wrapped. Eddy currents induced in the metal strips caused these cores to switch very slowly, so they were soon replaced by faster-switching nonconducting ferrite cores. However, Blois [27] suggested that nickel-iron films deposited on a substrate from a vapor could be made thin enough that eddy currents would not retard the magnetization switching process. He further believed that very fast memories could be built with magnetic films because of the simple, ultra-fast magnetization reversal that was theoretically predicted.

Observations in 1956–57 by Smith and by Olson and Pohm [28] showed that the magnetization reversal process in flat films was not so simple. Only by applying a field perpendicular to the magnetization direction were they able to achieve the fast magnetization reversal predicted for a single-domain rotation process. Even then, the reversal phenomenon was neither as fast nor as simple as predicted by theory. The complex mechanism of magnetization reversal in films was finally explained by Methfessel, Middelhoek, and Thomas [29] of the IBM Zurich Research Laboratory in 1961. Magnetization reversal was shown to consist of a *partial rotation* process in which the more easily rotated regions switch reversibly and the large stray fields from them tend to counter-reverse adjacent regions, which then cannot switch rotationally without the application of very much larger fields. Their results were consistent with the first high-speed sampling-oscilloscope measurements (with an overall resolution of 0.35 ns) made by Dietrich and Proebster [30] of the same laboratory. Suits and Pugh [31] in the IBM Poughkeepsie Laboratory subsequently showed that a much higher percentage of the film could be caused to switch rotationally if the drive line were sandwiched between two Permalloy™ films.

In July 1959 Raffel [32] and his group at Lincoln Laboratories placed the first thin-film memory in operation with the experimental TX-2 computer. It had a small 32 $\times$ 10-bit array, consisting of 1/16-inch (1.8-mm)-diameter, 700-Å (70-nm)-thick spots of Permalloy™ (trademark of Allegheny Ludlum Industries, Pittsburgh, PA) on a glass substrate; it was operated with a read-write cycle as short as 800 ns. At about the same time, Bradley [33] of

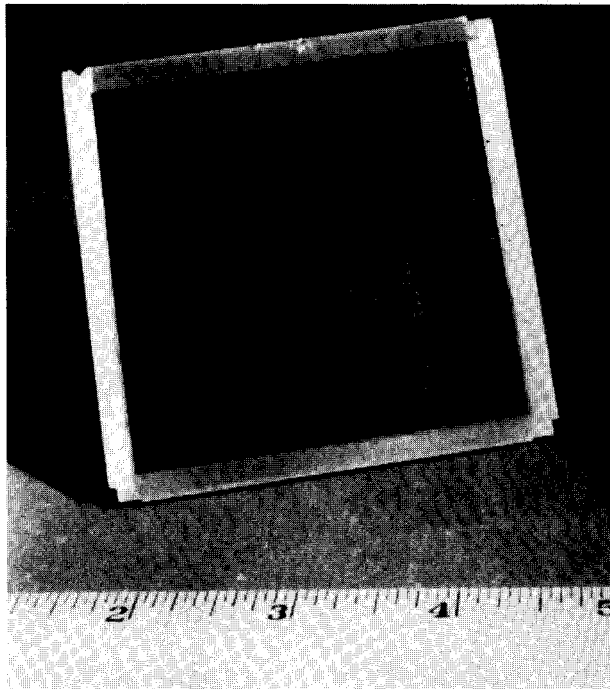


Figure 2 Photograph of a three-inch square magnetic film bit plate with 4176 bits. These were first shipped on the IBM System/360 Model 95 in February 1968.

International Computers and Tabulators operated a 50×50 -bit array of elements selected from a continuous sheet of Gyrallloy™ (trademark of Hewitt-Robins, Inc., Stamford, CT), later revealed to be NiFe with some Co. The magnetic film was deposited on aluminum substrates which served as ground planes for the drive and sense currents. Both of these approaches made use of an orthogonal drive scheme to provide nearly rotational magnetization reversal. In this scheme a large word-line current is used to drive all the films on a given line perpendicular to the "1" or "0" storage states. Positive or negative currents in the orthogonal bit lines determine whether a "1" or "0" is written as the word pulse is terminated.

Interest in thin-magnetic-film memories increased sharply in October 1961 when Rubens [34] of Univac described that company's plans to ship a 600-ns-cycle thin-magnetic-film memory with 4608 bits on the Univac 1107. In February 1962, an experimental 18 432-bit memory with a 60-ns access and a few-hundred-ns cycle was demonstrated by Proebster *et al.* [35] in the IBM Zurich Laboratory. The bits in this memory were 0.3 mm by 0.65 mm and 500 Å (50 nm) thick, and they were evapo-

rated on highly polished 2.5-cm-square coin silver substrates coated with silicon oxide. Techniques for achieving reproducible magnetic films on metallic substrates were pioneered in IBM by Bertelsen and Mohr [36].

In November 1962, a product development program was initiated which resulted in the magnetic film memory shipped in February 1968 on the IBM System/360 Model 95. The four magnetic film memory units on each Model 95 had cycle times of 120 ns and provided 60-ns access to 9.4 million bits or one million bytes of information. This was six times faster than the fastest ferrite core memory in the IBM System/360 line of computers. Each memory unit consisted of four 1024-word by 288-bit assemblies which were driven and sensed in parallel, but only 72 of the 288 bits read in parallel were gated out. Each assembly contained two arrays of 72 3-inch (7.6-cm) bit plates arranged back to back in a 6×6 configuration. An early version of this memory was described by Simkins in 1965 [37].

The memory array developed by Pugh *et al.* [38] consisted of copper bit plates on which 900 Å (90 nm) of Permalloy™ was deposited over a smoothing layer of dielectric and etched into 4176 rectangular bits 25×30 mil (0.63×0.76 mm) on a side (see Fig. 2). All bits were required to be good, but 80 were not wired and were reserved for repairs. The rectangular Permalloy™ bits were electrically switched and detected by copper conductors on Mylar® (registered trademark of E. I. du Pont de Nemours and Co., Wilmington, DE) foils placed directly over the copper bit plates. These conductor foils were backed by a flexible ferrite keeper [39] and supported by an aluminum frame which was long enough to accommodate six bit plates in a row.

Follow-on thin-film memory designs were developed in IBM which offered lower cost and higher performance than could be projected either for ferrite cores or for plated-wire memories [40], and even more advanced concepts using coupled film arrays deposited directly on silicon chips with integrated support circuits were considered [41]. However, these film memories were never manufactured. All development work on film memories was terminated in IBM by the end of 1969 due to the rapid progress in semiconductor memory technology which is described in the next two sections.

IBM's magnetic film memory was used only on the System/360 Model 95 computers. However, it provided the highest-performance megabyte memory in existence for many years. With over 4000 good bits on a single substrate, it had achieved a level of batch fabrication not reached by semiconductors until several years later.

Bipolar memory

By 1960 the semiconductor industry had started development efforts on bipolar integrated circuits. The objective was to achieve electrical isolation of the active components of a circuit [42] on a single silicon substrate. This powerful concept permitted complete circuits to be fabricated in a single semiconductor chip. The first work in IBM, which applied these integrated circuit techniques to the fabrication of memory, was started in 1963.

At this time, magnetic core memories had been very successfully applied to digital computers. They provided nonvolatile low-cost storage with cycle times as low as fractions of a microsecond. Magnetic film memories had similar attributes plus projected cycle times under 100 ns. However, the nonvolatility of these memories was achieved by the use of passive magnetic storage elements that required semiconductor devices to perform the decode, drive, and sense functions. The integration of magnetic with semiconductor components involved mechanical assemblies, and the semiconductor device requirements for the higher-speed memories were generally quite severe in terms of power, current, and voltage. Furthermore, the mechanical and electrical problems became increasingly severe as devices were miniaturized and as array capacities were increased to reduce the cost per bit.

Monolithic memories, in contrast, offered the attractive possibility of integrating the storage array with the drive, decode, and sense circuits—all on one silicon chip. Memory cost per bit was more nearly independent of memory capacity. However, the pervasive application of this technology to main memory technology was regarded by many as unlikely. The reasons cited were the relatively high cost per bit of large-capacity memories, the high power required to store information, and the poor reliability of semiconductor storage as compared with nonvolatile magnetic storage.

These presumed disadvantages stimulated a number of developments within IBM. To address the cost problem, development efforts concentrated on finding memory cells which occupied the least chip area. The power problem in memory was greatly reduced by the development of pulse power techniques as first proposed by Henle [43]. The potential reliability problem was solved by the application of error-correcting codes to the memory at the systems level. In addition, the reliability of semiconductor storage proved to be much better than was originally estimated. The volatility problem proved not to be a significant factor in most computer applications. Even magnetic memories were rarely designed to provide integrity of the stored data if power was lost.

• *Special-purpose memories*

The first monolithic memory application in IBM was for a storage-protect memory on the System/360 Models 91 and 95. This unit was to contain the code which logically prevented access to specified blocks of main memory. The ferrite core version of this unit was a 64-word, 20-bit memory with a cycle time of 350 ns, whereas the monolithic version would have a 128-word, 20-bit array and a 300-ns cycle. The project was initiated in January 1965.

The memory circuit used in this chip was conceived by Farber and Schlig, and an improved version incorporating diode loads was first published in May of 1966 [44]. The complete cell used five transistors. It was larger than other cells which were known at this time but was chosen for its high-performance, nondestructive read and its large tolerance to component variations. The first, Phase 1 version was described by Agusta, Bardell, and Castucci at the October 1965 Professional Group on Electron Devices [45]. It consisted of a 4×4 array of Farber-Schlig cells and contained no decode or drive circuits. Two of these chips were mounted on a half-inch (1.27-cm) module with six modules on a card. Total memory capacity in the application was 1024 9-bit words. The monolithic memory protect was announced on the Model 91 in January 1966, making it the first announced application of monolithic memory technology in a commercial system.

The second application of monolithic semiconductor memories was for the automatically buffered cache memory system [46] first implemented on System/360 Model 85. A cache memory is designed to hold that portion of the main memory content that is currently being used. This is accomplished by a least-recently-used (LRU) algorithm implemented in hardware. Most of the processor memory references can then be handled by the cache with its short access time. For example, in the Model 85, a 16K-byte cache of 80-ns cycle and a multimegabyte main store with a 1- μ s cycle achieved a performance 80% as good as would have been achieved by a single main memory of 80-ns cycle [47]. This resulted in a substantial improvement in the cost/performance ratio of the memory system and represented a major systems innovation on the IBM System/360 Model 85.

The requirement for a small fast memory for the cache application was well suited to the capability of a bipolar technology. The Phase 2 memory was developed with 64 bits on a 2.85-mm-square chip. The memory cell was an improved version of the one used in the Phase 1 chip. The Phase 2 chip was qualified in September 1967 and later described in two companion papers presented at the February 1969 International Solid State Circuits Confer-

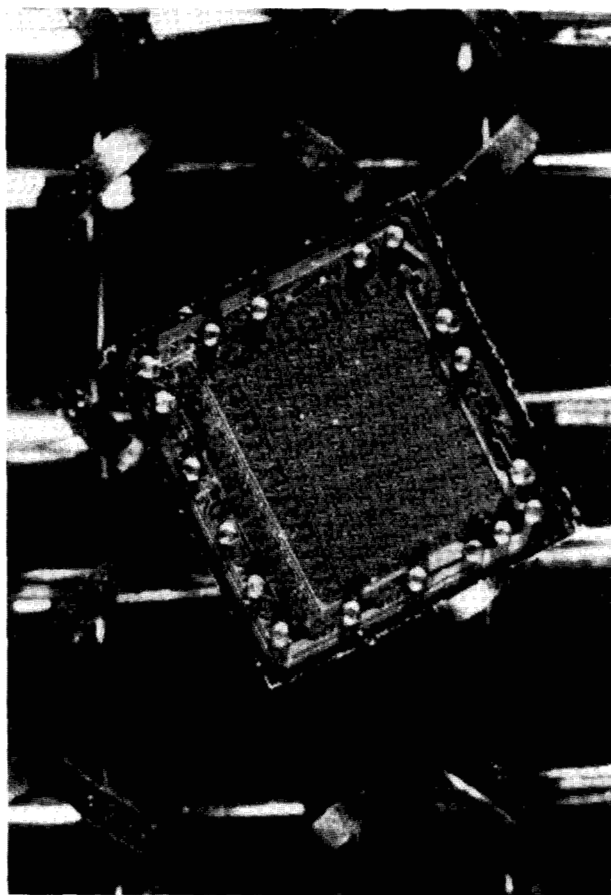


Figure 3 A 128-bit bipolar chip of the type used in the first all-semiconductor main memory which was announced on the IBM System/370 Model 145 in September 1970. The core plane supporting it has 30–50-mil cores. The smallest cores used by IBM in a product were 13–21 mil.

ence (ISSCC). The first paper, by Augusta [48], described the memory chip. The second paper, by Ayling, Moore, and Tu [49], described the memory circuits and the chip organization. Details of the memory cell were published in August 1972 by Farber and Schlig [50].

The Phase 2 chip was the first to contain on-chip driver circuits in addition to the array of storage cells. The chip had a power dissipation of 112 mW and a differential output signal of 2 mA. The X and Y access lines were brought to the terminals of the chip with a nondestructive read delay of 7 ns and a chip writing time of 12 ns. The chip was fabricated with 5- μ m minimum image lithography and a single level of aluminum interconnections. Two of these chips were mounted on a 23-pin, half-inch (1.27-cm) module. A single chip integrated the equivalent of 664 transistors, diodes, and other components. Phase 2 tech-

nology was also used for cache memories in the System/370 Models 165 and 155 with 80-ns and 115-ns access times, respectively [51].

Following the 64-bit chip development, a 32×3 -bit chip was developed. It also used a 5- μ m minimum-feature technology and was designed in the 1968–69 time period. This chip utilized a new cell configuration invented by Harper of IBM [52], having two cross-coupled double-emitter devices with resistor loads. Two of the emitters were joined to a common read line; the other two emitters each went to a separate bit line. This was the first chip to utilize full on-chip decoding. It was used for storage-protect and buffer applications on System/370 Models 158 and 168.

The 32×3 RAM chip was redesigned in an oxide-isolated 2- μ m-epitaxy technology with a modified Harper cell and was qualified for production in 1976. The cell modifications included the addition of Schottky diodes across the load resistor and two read lines from each cell which were obtained by means of emitter follower outputs on the collectors of the cell. This modified chip has been used in the cache and the channel circuits of the IBM 3030 systems.

At the 1971 ISSCC, Wiedmann and Berger of IBM described a memory cell utilizing lateral pnp loads [53]. In 1973, at the ISSCC, Wiedmann described an improved cell with lower power and better performance [54]. The cell used cross-coupled npn transistors with lateral pnp loads. It was designed into a 512×10 array (1-bit redundancy) and a number of smaller arrays, all of which are used in the IBM 4300 systems. The access times of these arrays are in the 30–40-ns region. They are packaged with logic chips on multilayer ceramic substrates.

• Main memories

In January 1968 the decision was made at IBM to stop developing ferrite-core commercial memories in order to concentrate on monolithic memories. The Phase 2I 128-bit chip had been developed. This was the first monolithic chip with the potential for replacing ferrite memories on a cost basis. The objective was to break even in cost and go ahead in future extendibility.

The Phase 2I design utilized the Harper cell and pulse power with the peripheral circuits being turned on and off [55]. The organization of the chip was 128×1 . The chip (shown in Fig. 3) was qualified in August 1969. Two of these chips were mounted on a half-inch (1.27-cm) ceramic layer with two of these layers being stacked, resulting in a 512×1 -bit module. This module contained 5700

components occupying one quarter of a square inch of board space. Twenty-four of these modules were mounted on a 4.5 × 3.5-in. (11.1 × 0.9-cm) card and thirty-six of these cards on a 9 × 13-in. (23 × 43-cm) board for a total storage capacity of 49 152 nine-bit bytes. This design was used as the main memory for the System/370 Models 145 and 135 [56]. These IBM systems were announced on September 23, 1970, and on March 8, 1971, respectively. With shipment of the first Model 145 in June 1971, IBM had achieved the first commercial application of semiconductor main memories.

A three-quarter-good program was also implemented with the Phase 2I chip. This permitted 75% utilization of the bits on a chip containing a single, or in some cases multiple, malfunctioning bits. It was the first effort to enhance yields and reduce costs by a partially good chip strategy [57].

The 128-bit chip technology was described in two companion papers which were presented at the 1971 ISSCC. Gates, McKinney, and North [58] described the chip design procedures, and Ayling and Moore [59] described the circuits and logical organization of the chip and memory card. A 256-bit chip of this design was put into production as a cost reduction toward the end of the program. The ceramic module was a one-layer design holding two chips.

By 1971, work on an improved bipolar memory technology was well underway. The main features were the use of two levels of metal, a simpler cell configuration consisting of two cross-coupled npn transistors with dumbbell resistor loads, a self-aligned emitter process, and the addition of Schottky diode gates. In addition, a lateral pnp was used for the bit decode circuits [60].

The design for a 1K RAM was completed about March 1972 and was applied to a product in June of 1972. The chip size was 3.0 × 3.8 mm. The memory units constructed from this technology ran with approximately 90 ns access time at the board level and cycle times of about 110 ns with pulse-powering capability. At the system level, where the technology was combined with error-correcting codes (ECC), cycle times were somewhat slower. When used as a buffer memory without pulse powering, the chip was capable of a 13-ns access and a 45-ns cycle. The chip was incorporated into a 4K × 1 module which consisted of two half-inch (1.27-cm) stacked ceramic substrates with two chips per layer. The chip was first used in the System/370 Models 138 and 148 and later has been used as a cache technology for Model 168 through to the IBM 3033.

• *Future developments*

Two factors limited the further application of bipolar technology to main memory. The first was the emergence of FET technology with fewer masking steps and a high-yield process which combined to produce high-density, low-power, and low-cost memory designs. The second factor was the acceptance of the cache memory concept. As stated previously, the cache memory removed the high-performance requirement from the main memory technology, permitting the slower FET memories to fulfill this role. The continued future application of bipolar technology to high-speed register and cache applications seems secure for the foreseeable future [61]. The scaling principles, while not as simply stated as those for FET technology, still apply. Smaller dimensions result in lower power, improved performance, and improved productivity. For the same lithography dimensions, bipolar memories will continue to offer higher performance than their FET counterparts. The question is whether bipolar memories may, at some future time, re-emerge as a main memory technology [62]. In either technology, the most dense storage cell is likely to remain some form of dynamic charge storage.

MOSFET memory

The principle of the surface field effect transistor was proposed about fifty years ago [63]. Advances which led to practical implementation of the metal oxide semiconductor field effect transistor (MOSFET) took place in the late 1950s and early 1960s. Notable among the many contributions were the demonstration of a thermally grown oxide on silicon as a gate insulator in 1960 by Kahng and Attalla [64] and the publication of a comprehensive paper on MOSFET device design and characteristics in 1963 by Hofstein and Heiman [65].

Distinct from the rest of the industry, which pursued the p-channel technology, IBM made an early decision to develop the more difficult n-channel technology because of its higher performance potential. As a result, IBM pioneered the n-channel technology throughout the 1960s and began manufacturing high-speed (about 50-ns access) 1024-bit memory chips in 1971. Memory systems as large as 2M bytes (almost 20 million bits) were announced on the IBM System/370 Model 158 in August 1972 with shipments starting in April 1973. Probably the first commercially successful p-channel product was the 1024-bit chip (the 1103) which was announced by Intel [66] in 1970 and shipped in large commercial computer systems in the 1972-73 time frame.

The first 64K-bit dynamic RAM engineering parts in IBM were fabricated in 1976, manufacture started in 1977, and 2M-byte memories were shipped in the IBM 4341 system in 1979.

- *Early n-channel work*

Early work in several laboratories throughout the industry indicated that the new MOSFET device would be the best choice for achieving many circuits on a single chip because of its expected process simplicity and high density. A decision was made by the IBM Research Division in 1963 to mount a comprehensive LSI program. The term LSI was coined at that time in IBM to denote Large Scale Integration. To the authors' knowledge this was the beginning of the use of that term throughout the industry.

The n-channel technology was chosen by IBM in 1963 because it had potential for operating at a higher speed than the alternative p-channel technology. This choice was made in spite of the fact that the n-channel technology was expected to be more difficult to implement. Surface scattering and high field effects were expected to diminish its potential three-times mobility advantage. The field polarity in the gate insulators moved positively charged contaminants toward the silicon surface, thus reducing device threshold voltages and increasing leakage and surface scattering problems. Also, unless an extremely high substrate doping was used, the n-channel MOSFET was a depletion-mode or normally-on device. This limited its circuit usefulness and created a severe surface leakage problem.

Several key discoveries in 1963 and 1964 made the n-channel technology viable. Cheroff, Fang, and Hochberg [67, 68] and Lehman [69] of IBM showed that a proper low-temperature annealing process would stabilize the n-channel device mobility at a high value by eliminating fast surface states [67]. (Lehman's work [69] also showed that silicon could be used as the gate electrode material.) The n-channel devices had been essentially nonoperational to this point. Hydrogen was shown to be an important factor in this annealing process [70]. A second key concept, of Cheroff, Fang, and Seraphim [71] and of Heiman of RCA [72], was the use of a substrate bias to control device threshold voltages and thereby turn off both the n-channel switching devices and the parasitic thick oxide devices. A third element was the work of Kerr, Logan, Burkhardt, and Pliskin of IBM [73], which showed that phosphosilicate glass (PSG) over an SiO_2 film resulted in an electrically stable structure with large latitudes in cleanliness and process control.

From 1964 to 1968 considerable effort went into understanding device physics and establishing a reliable and reproducible process. During this period, there were many other laboratories in the industry which were also very active in basic MOSFET work. For example, Snow, Grove, Deal, and Sah of Fairchild Semiconductor Labo-

ratories showed that Na^+ was the major contributor to threshold instability [74]. Later they showed that polarization of the PSG could introduce a threshold shift [75]. A critical accomplishment in IBM was the work of Balk and Eldridge in the mid-1960s which showed how to optimize the thickness and concentrations of the PSG layer to achieve stabilization under practical fabrication conditions without significant polarization effects [76]. Also, Chou and Eldridge [77] showed that the PSG layer improved gate reliability since it forms a barrier between the aluminum gate electrode and the thin oxide. This, combined with improvements in the purity and structural perfection of the SiO_2 insulator resulting from the implementation of a super-clean dry oxidation process in 1963, resulted in dramatic improvements in yield, breakdown voltage, and reliability.

A final ingredient of an optimized n-channel device was the substrate crystal orientation. Work reported in 1965 by DeLord *et al.* of Reed College based on experimental work at Tektronix [78] and by Balk, Gregor, and Burkhardt from IBM [79] showed that $\langle 100 \rangle$ surfaces exhibited a lower charge. Then Fang and Fowler demonstrated that the $\langle 100 \rangle$ surface also had a higher mobility [80]. This firmly fixed the choice of the $\langle 100 \rangle$ orientation for n-channel devices.

The early IBM work was largely devoted to LSI logic. By mid-1966, the basic n-channel device, circuit, and chip designs were established [81]. An automatic artwork generator, which set the direction for the industry, was developed in 1965-66 and was used to make the $10\times$ masks for the experimental MOSFET chips [82].

The use of a substrate bias for the n-channel device proved to be a critical element. Not only did the bias turn off the switching device and reduce leakage, but it provided some very important design flexibilities [83]. It allowed a dramatic reduction in the field oxide thickness needed to maintain proper isolation between devices. Also, it allowed the use of lower substrate doping which reduced substrate sensitivity effects and junction capacitance.

In the mid-1960s, it became apparent that semiconductor memory had the potential of replacing ferrite core systems for main memory applications. Pleshko and Terman of IBM showed that high-speed memories could be implemented by using six-transistor MOSFET static cells in the memory array and by using bipolar circuits to provide the high-speed decoding, driving, and sense-amplifier functions on separate chips [84]. A series of memory test chips were fabricated, including a 48-bit chip in 1966, a 128-bit chip in 1967, and a cross section of a 512-bit chip in early 1968.

These advances were paralleled in the mid-to-late 1960s by the development in IBM of dynamic memory cells which promised further density improvements: the four-transistor cell [85], a three-transistor cell [86], and the one-transistor cell [87]. The one-transistor cell, conceived by R. Dennard, uses a MOSFET device as a switch and a capacitor as the storage element. It has become the standard high-density cell in the industry.

In April 1967 a one-year pre-product memory development program was set up between IBM Research and the product laboratories. By 1968 a process [88] suitable for making complex development parts had been practiced. Considerable data had been gathered on reproducibility, gate shorts, and reliability under stress; and an experimental 16K-bit hardware model was assembled. This model was run successfully under test for two years.

A final requirement was the use of the IBM flip-chip attachment techniques. The residual charge and radiation damage from the required sputtered quartz overcoat were prime concerns. The enhanced design margin provided by the substrate bias and the PSG passivation, combined with clean sputtering techniques [89], resulted in a manufacturable process. A 512-bit product prototype was designed and built in late 1968. A key innovation by G. Sonoda [90] was the bootstrap circuit which allows a gate to be boosted to a voltage higher than the power supply in order to overcome device threshold effects.

The very tight coupling between the device, circuit, and technology efforts from 1963 through 1968 made it possible for a comprehensive device and chip design manual to be written which is still widely used in IBM as a basic MOSFET reference. The highlights of the manual were published externally by Critchlow, Dennard, and Schuster in 1973 [91]. The device design was centered on a 50-nm gate oxide thickness with a 4- μm channel length. The gate oxide thickness was later increased to 70 nm for the actual products.

• MOSFET memory products

Preproduction parts using 512-bit chips were successfully made in 1969 and 1970 and delivered to system builders. The process and design were qualified to meet reliability and yield requirements and a 1024-bit chip was put into production in 1971. This product was soon upgraded to a 2048-bit chip [92].

Four 2048-bit chips with a nominal access time of 50 ns were packaged on an 8K-bit multichip half-inch ceramic module. The memory and support modules were packaged on an 11.5 $\times$ 8.5-cm card to provide 32K $\times$ 8-bit (256K-bit) memory cards which were plugged into boards

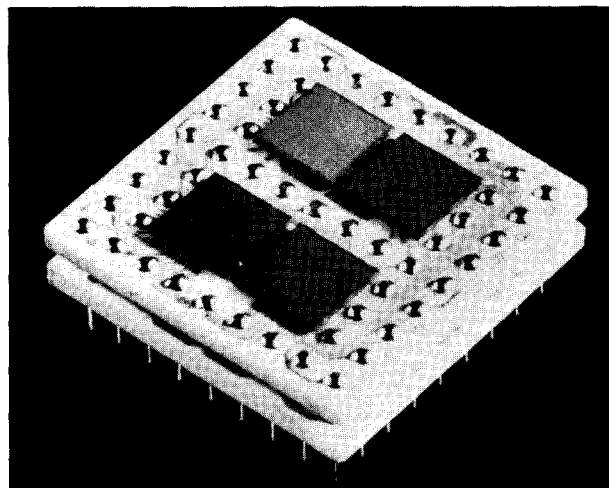


Figure 4 The double-layer, one-inch ceramic module holds eight 64K-bit SAMOS chips for a total of 512K bits. IBM announced this memory technology in October 1979.

to provide a 2M-byte memory system. Error-correction coding techniques were used at the memory system level to meet reliability, availability, and serviceability requirements. A partially good chip approach [57] was used to increase productivity in early manufacturing by utilizing the portion of the chip which met specifications. This technology, with a number of process and design enhancements such as the substrate voltage generator [93], was the mainstay of the MOSFET memory and logic products in IBM throughout the 1970s.

The main thrust of the second generation of IBM RAM products was exploitation of the high-density potential of the one-transistor cell to achieve a low cost per bit. After extensive study, the decision was made in 1972 to develop a unique metal gate MOSFET technology called SAMOS (silicon and aluminum metal oxide semiconductor). The process, invented by Garnache and Smith of IBM [94], uses a 45-nm-equivalent nitride-oxide gate insulator for enhanced gate reliability and a polysilicon field shield to reduce surface leakage to very low levels. A series of product designs [95, 96] were developed using line widths as narrow as 2.5 μm .

The first 64K-bit chips were made in 1975, engineering parts were shipped to systems developers in 1976, manufacturing was started in 1977, and systems containing these chips were shipped in 1979. Thus, the decision to implement the unique SAMOS process in 1972 provided IBM with a 64K-bit-chip memory product well before its competition. A very high packaging density is achieved by placing eight 64K-bit chips on a double-layer, one-inch

ceramic module allowing a 1M-byte memory to be packaged on an 11.3 by 17.6-cm card (see Fig. 4).

This program encountered four major technical challenges. First, the very severe leakage requirements led to the use of the field shield and the development of improved gettering techniques. Second, the small geometries resulted in high fields with the possibility of hot-electron injection into the gate insulator. This led to extensive research on hot-electron effects [97] which has defined one of the limits of MOSFET technologies. Third, the small signal charges of only 200 to 300 fC for the 64K-bit chip required sense-amplifier innovations [98]. The final challenge, of attaining acceptable yields, was alleviated by the use of redundancy techniques in which extra bit and word lines are provided to replace defective lines or cells [99]. Fusible links are fabricated on the second level of metallization to effect the wiring changes. Two further novel features of the SAMOS process are the use of a lift-off metallization technique [96, 100] and the use of a two-level insulator consisting of sputtered quartz covered by polyimide [96].

• Future directions

A major trend in MOSFET technology has been to scale to smaller dimensions and voltages in order to achieve enhancements in density, performance, and power [101]. IBM has been very active in the development of advanced lithography techniques including the development and use of electron-beam direct write exposure systems [102]. Designs and processes have been developed in the laboratory and practiced on complex chips to demonstrate their viability and to quantify practical design limits. For example, an experimental 8K-bit silicon gate memory chip was fabricated with 1.25- μm minimum dimensions in 1975 [103]. This technology was then developed to a much higher degree and used to fabricate complex logic chips in the 1- μm Logic and Array Test Vehicle (LATV) project from 1975 to 1978 [104].

As circuit miniaturization is pushed to the limit, problems of high current densities, hot electrons, and ionizing radiation are becoming more significant. Basic work and innovation continue. For example, as current densities, resistive voltages, and time constants became limiting factors, IBM engineers reported that a second level of metal provides a significant performance advantage for high-speed designs [105]. IBM has pioneered the use of the metal lift-off technique [100], which allows line widths to be greatly reduced while not reducing the line thickness in proportion. Significant contributions have also been made to the use of low-resistivity refractory metal/polysilicon conductor technology to overcome the speed limitations of circuits using polysilicon conductors [104].

There continue to be device innovations. The Merged Charge Memory (MCM) structure [106], which allows Charge-Coupled Device (CCD) concepts to be used to fabricate dense RAM, is interesting in that it may provide a cost/performance tradeoff between RAM and CCD. Improved device structures such as the Lightly Doped Drain (LDD) MOSFET [107] are extending the limits of the technology and promise further speed and density improvements. Advances in CMOS technology indicate that it will become more significant in the future. Clearly we will see further dramatic enhancements of MOSFET memory technology during the 1980s.

Magnetic bubbles

Boback of Bell Laboratories first proposed the use of magnetic bubbles for information storage in orthoferrites [108] in 1967 and then in garnet films [109] in 1970. Researchers at IBM quickly became interested because there was reason to believe this technology might offer the nonvolatility of ferrite cores and magnetic films with a cost even lower than projected for semiconductor memories.

Significant contributions were made to the development of garnet compositions and epitaxial growth techniques by Giess *et al.* [110] in 1971. Amorphous Gd-Co films were developed by Chaudhari *et al.* [111] and shown to support very small magnetic bubbles. The first reported observation of velocity saturation of magnetic bubbles was by Calhoun, Giess, and Rosier [112]. The theory for this phenomenon was developed by Slonczewski [113], and its significance to bubble devices was more fully developed by Argyle, Slonczewski, and Mayadas [114]. A major contribution to the modeling of bubble devices was the closed-form equations of Almasi and Lin [115], which were based on a magnetic circuit model for bubble-PermalloyTM interactions.

Almasi, Chang, Keefe, and Thompson [116] were the first to propose magnetoresistive sensing of magnetic bubbles, which is now used in all magnetic bubble designs. Almasi *et al.* [117] were also the first to report the operation of a fully functional bubble chip. This chip, with 12- μm -diameter bubbles, used magnetoresistive sensing as well as unique on-chip decoding. In 1973 an IBM interdivisional program produced a packaged 1000-bit-chip device which achieved nonvolatile operation at 100 kHz. It incorporated the first in-package preamplifier for noise reduction as well as magnetoresistive sensing [118]. It also made use of propagation elements deposited directly on the garnet as proposed by Shick *et al.* [119] and the major-minor loop organization proposed by Bonyhard *et al.* [120] of Bell Laboratories. Subsequent IBM work on "conventional" bubble devices was aimed

primarily at the use of e-beam [121] and x-ray [122] lithography for device miniaturization.

- *Contiguous-disk devices*

The observation of bubble propagation around masked contiguous disks in ion-implanted garnets reported by Wolfe *et al.* [123] of Bell Laboratories in 1972 generated substantial interest in IBM, where an internal study of the potential and limits of bubble technology had already started a search for gapless structures in order to achieve higher densities and lower costs. A major breakthrough was the identification of a magnetically charged domain wall as the propagation mechanism in these new ion-implanted devices [124]. Making use of this mechanism, Lin, Almasi, and Keefe [125] achieved the first successful demonstration of all-contiguous-disk device functions in 1974. A written account of this 5- μm bubble device first appeared in a review article in 1977. Propagation paths were defined on the garnet by a gold contiguous-disk pattern which was used to mask out ions when the rest of the garnet surface was implanted by high-energy ions. After ion implantation, this gold mask was removed. Then insulating layers, PermalloyTM patterns, and gold lines were deposited on the garnet to form sensors, nucleators, switches, stretchers, and the connecting control lines.

By 1975, there was also strong motivation to demonstrate much higher densities. A double-layer garnet structure was developed [126] in which the EuTmYGaIG composition of the bottom layer (or storage layer) near the GGG substrate was selected for bubble stability and the GdTmYGaIG composition of the second layer (or drive layer) was selected to facilitate magnetic anisotropy sign reversal by ion implantation through a mask to create the desired propagation structures. These double-layer structures were used in the first demonstration of 1- μm bubble propagation and manipulation in contiguous-disk devices [127].

Ferrofluid studies by Lin, Dove, Schwarzl, and Shir [128] provided a detailed understanding of magnetic charged-wall mechanisms in the tridirectional anisotropic $\langle 111 \rangle$ garnets. The words "whip" and "flip" became part of the magnetic bubble lexicon in describing the behavior of charged walls. These studies facilitated a major design breakthrough in which switches used bubble striping between the major and minor loops [129] and crystallographically phased current pulses to select the direction of transfer [130]. It also permitted the effective utilization of a novel self-aligned structure [131] in which the ion-implantation and the control-line masks were combined into one.

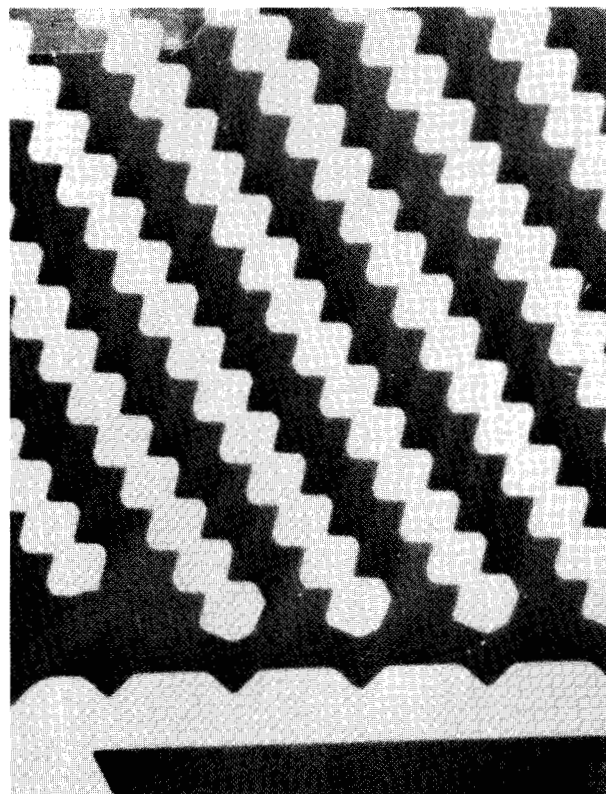


Figure 5 Photograph of a contiguous-disk bubble storage region with a 5- μm propagation period and a density of 3.3×10^6 bits/cm². A control current through the horizontal track is used to switch bubbles from the input track to the storage tracks in this self-aligned structure, described in Ref. 130.

In 1979 Lin, Almasi, Keefe, and Pugh [130] reported the full-chip operation of contiguous-disk devices at 150 kHz with better margins than any previous contiguous-disk devices. These devices utilized an easy-to-fabricate, self-aligned structure, 1- μm bubbles, and a 5- μm period to achieve the highest-density magnetic bubble devices to that time (see Fig. 5).

- *Bubble lattice files*

One of the most innovative ideas to emerge from IBM's bubble work was the proposal made in 1971 by Calhoun, Slonczewski, and Voegeli [132] to use regular, close-packed arrays of magnetic bubbles to store information. Such arrays of bubbles were observed during the 1960s [133], and their general properties such as bubble spacing, diameter, and energy had been described by other workers [134]. However, the idea that bubbles could be coded by means of their domain wall states and then manipulated in an array to provide high-density storage had not previously been proposed.

Demonstration of bubble lattice propagation with magnetic bubbles in a garnet was first achieved in January 1974 and reported in 1975 [135]. This device also demonstrated the use of parallel magnetic stripe domains as buffer regions [136] to either side of the bubble array. The first published description of a complete bubble lattice storage device was provided by Voegeli, Calhoun, Rosier, and Slonczewski [137]. It included the important concept of access channels proposed by Rosier [138] in which access channels were provided at selected positions within the lattice area. The lattice was translated until a desired column of bubbles was in one of the channels. The column of bubbles was then propagated out of the array while new bubbles were inserted from the other end of the channel.

Several methods for distinguishing among different domain wall states were proposed by IBM workers. The method finally implemented was to utilize the different deflection angles observed among bubbles with different wall states as proposed by Slonczewski [139]. The first experimental observation that bubbles with a small number of Bloch line pairs moved at fixed angles to a field gradient was reported in 1973 by Slonczewski, Malozemoff, and Voegeli [140]. The deflection angles were found to be proportional to the S number or "state" of the bubble, defined as the number of rotations of the magnetization in the bubble wall during a complete circuit of the circumference of the bubble.

Experimental work by Hsu [141] showed that two bubble states can coexist in bubble films in which the magnetization is exchange-coupled to an in-plane layer. When the $S = 1$ -state bubble is propagated in a magnetic field gradient, it moves at an angle of 5° to 30° from the field gradient, depending on the material. The $S = 0$ bubbles propagate parallel to the field gradient. Hsu also showed that appropriate application of in-plane fields could be used to switch the bubble from $S = 0$ to $S = 1$ or vice versa. This work verified the operability of Slonczewski's coding scheme and provided the basis for subsequent studies of wall states in bubble lattice devices.

Beaulieu *et al.* [142] identified eleven transition mechanisms between seven different wall structures of which four structures corresponded to $S = 1$, two to $S = 1/2$, and one to $S = 0$. The discovery by Brown and Hsu [143] of better state stability in SmCaGe than in the originally used YEu gallium-iron garnets was of considerable importance to device work.

All of these concepts were tested successfully in a fully functional bubble lattice storage device of 1000 bits in 1978 [144]. Although the demonstration vehicle was

judged to be too complex for commercialization, it had proved that all of the concepts could be made to work simultaneously on the same garnet chip.

Potentially simpler devices had already been proposed by several IBM workers in which bubble array propagation was affected by an external rotating field and Permalloy™ structures similar to those used in conventional bubble devices [145]. The most successful test of these concepts was obtained with a 14 000-bit array by Brown *et al.* [146]. These results showed that the major-minor loop architecture and symmetric Permalloy™ chevron propagation structures of conventional bubble devices could be combined with wall-state coding to achieve very high storage densities.

• Future directions

Several companies have begun to ship "conventional" magnetic bubble products with up to one million bits per chip. This is 16 times more bits per chip than is presently available in any semiconductor memory product. Nevertheless, the projected costs per bit are not yet sufficiently lower than those projected for higher-performance semiconductor memories to ensure adequate sales for magnetic bubble devices. Further advances in conventional bubble technology or a shift to more exotic designs appear to be needed. Contiguous-disk and bubble lattice file devices are still in the research stage; however, work on contiguous-disk devices has been initiated in a number of laboratories, suggesting that an increased rate of progress can be expected.

In any event, semiconductors are expected to maintain a dominant role in memory technology for the foreseeable future. They provide higher performance and, in very small memories, a lower cost than any magnetic bubble device technology proposed thus far.

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