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Real-Time Systems for Federal Applications: A Review of Significant Technological Developments

The Federal Systems Division of IBM has been heavily involved in complex, on-line, real-time systems for over twenty-five years. In this paper a representative sample of these programs are reviewed, and an evaluation of the significant lessons learned from this wealth of experience is presented. The key issues which differentiate real-time systems from their more conventional data processing counterparts are identified and their implications are discussed. This leads to some conclusions regarding the kind of commitment that is necessary in order to succeed in the area of real-time applications.

Introduction

The basic mission of the Federal Systems Division of IBM (FSD) is to serve the special data and signal processing needs of the federal government. Some of these needs can be satisfied with standard products, but other requirements can only be met with a combination of hardware, software, and services configured to satisfy the user's applications.

Fulfillment of FSD's mission has involved a broad range of challenging applications and technology, yet there is a common thread among these widely varied programs: FSD has consistently been involved in on-line, real-time applications. Real-time data processing is characterized by highly structured and repetitive tasks, high speed, stability considerations for closed-loop processing, automated fault detection and decision making, and customized input and output. The following sections of this paper describe programs that trace the evolutionary progress of FSD in real-time systems. An overview of representative FSD systems is given and the FSD design environment is addressed. This is followed by sections on technological implications, real-time digital processing technology, reliability and availability, and total responsibility. The last section of the paper describes the LAMPS (Light Airborne Multi-Purpose System) program to illustrate the nature of one aspect of the division's current activity.

Twenty-five years of challenge: An overview of representative FSD systems

FSD was launched in 1955 as the Military Products Division of IBM. At that time it had two major contracts: the data processing centers for the SAGE (Semi-Automatic Ground Environment) air defense system, and the on-board AN/ASQ-38 navigation and bombing system for the B-52 aircraft. These programs involved real-time systems that were significant technological advances over anything preceding them, and they were representative of the great majority of FSD programs ever since. For example, SAGE was the first of many complex *ground-based command and control systems* for FSD. Subsequent FSD programs in this category include

- SABRE (Semi-Automatic Business-Related Environment)—American Airlines' on-line interactive reservations system [1].
- IBM 9020—the multiprocessing computer system that is the core of the FAA's National Airspace System for

coordinated air-traffic control throughout the United States [2, 3].

- RTCC—the space program's Real-Time Computer Complex in Houston, Texas, discussed further in an accompanying article in this issue [4]. FSD has had an important and growing role in every manned space program: Mercury, Gemini, Apollo, Skylab, and currently, Space Shuttle.
- LPS—Shuttle Launch Processing System [4].
- LCC—Saturn Launch Control Complex [4].
- DFCS—the Drone Formation Control System, at White Sands Missile Range, which allows control from the ground of aircraft flying in close formation and/or performing maneuvers that would not be feasible in piloted aircraft [5].
- SPRINT—a command and control system for police cars in New York City.
- The control center for the New York Power Pool, Guiderland, NY.
- GPS—the control segment for the Global Positioning System, a recent (1980) ground-based control system awarded to FSD. This system features precise position measurement of the constellation of satellites through continuous worldwide monitoring. The satellites relay the ground-based computations to suitably equipped users, permitting precise navigation worldwide in all weather. IBM is prime contractor to the Air Force and will provide the entire system, including RF, data processing, and software elements.

Similarly, the B-52 avionics system of the 1950s was the first of many *onboard data processing systems* for aircraft, missiles, satellites, ships, and submarines—the kind of products and systems that have become a way of life for FSD. A sampling of subsequent programs in this category would include

- Titan II (ASC-15 computer)—IBM's first onboard computer in the missile and space field. It was a drum machine, and was also used in Saturn I and IB.
- OAO—the Orbiting Astronomical Observatory onboard processor, which utilized quad-redundant components [6].
- Gemini—manned orbiting vehicle computer.
- Saturn V—Apollo launch vehicle computer.
- Space Shuttle—redundant computer.
- System/4 Pi—FSD's family of avionics computers. Thousands of 4 Pi machines have been delivered on scores of different applications, including over 2000 missile guidance units for the Harpoon program, more than 1400 avionics computers for the A-7 aircraft, and additional computers for the F111, FB111, A-6, and EA6B aircraft.
- AN/BQQ-5—the Navy's first digital submarine sonar system: an integrated onboard signal processing and control complex. The technology of the time was such that 600 System/360 Model 65s would be required to duplicate the function of its digital beam-former—a special-purpose processor designed in 1970 [7].
- APR-38 Wild Weasel—an airborne radar signal-processing system consisting of 14 separate units and more than 50 antennas which detect, locate, and classify radar emitters.
- MCS—The Modular Computer Series, the latest generation of System/4 Pi machines. By an interesting coincidence, the first several hundred MCS processors will be used on the B-52 aircraft as part of an overall replacement of avionics equipment produced in the 1950s and 1960s [8].
- E-3A AWACS—FSD is responsible for the data processing system in two generations of the Airborne Warning And Control System which flies aboard a modified Boeing 707 aircraft [9].

Finally, the combination of the SAGE and B-52 was a precursor of yet a third area of FSD business: *system integration responsibility for onboard command and control systems*—for submarines, ships, aircraft, and space vehicles. This has become a premier business of FSD and has included such major programs as the following:

- Saturn V Instrument Unit (IU)—Saturn V was the launch vehicle (rocket) for the Apollo moon landing program, and IBM provided one entire section of it. The IU physically interconnected the third stage of the three-gigagram launch vehicle with the top section containing the Apollo spacecraft. It served as the central control and communication element of Saturn V. IBM was responsible for total system integration, assembly, and checkout of the more than sixty pieces of equipment contained in the IU. The Guidance Computer, Data Adapter (I/O Unit), Switch Selector (signal routing unit), Operational Flight Software, and Ground Command and Control Software were designed and provided by FSD [10].
- TRIDENT CCS—the TRIDENT Command and Control System consists of five subsystems requiring the integration of more than a million lines of software and over 100 different major hardware units [11].
- LAMPS—FSD has total responsibility for the overall performance of an electronics-packed, ship-based helicopter plus all of the associated shipboard equipment [12]. The LAMPS program involves all of the issues discussed in this paper and we will return to LAMPS subsequently to examine the total range of responsibility and commitment required to succeed in the world of real-time systems.

The foregoing comprise a representative sample of the scores of real-time applications that FSD has addressed

over the past quarter century. A further examination of the environment in which these systems operate, and the conditions under which they are procured, will help to highlight some of the unique issues that must be faced in this area.

Application-driven design environment

FSD systems usually have to be tailored to the specific environment of each application. "Onboard" systems, for example, usually fit into very limited (and sometimes very odd-shaped) volumes. They must be lightweight and low-power and must operate reliably over ambient temperatures ranging from −55°C to 71°C, while subjected to such hostile environments as shock, vibration, dust, and salt spray.

Often the most significant accommodations that must be made are the unconventional interfaces inherent in many real-time applications. For example, the basic inputs of a sonar system are audio signals. Airborne radar and electronic countermeasures systems operate at the other end of the spectrum with carrier frequencies in the gigahertz range. These systems detect, analyze, and emit various types of electromagnetic pulses—with each type having its own unique waveforms, pulse repetition rates, carrier frequencies, and other specialized characteristics.

Typical avionic and missile data processing equipment must interact with a wide range of sensor and control subsystems, each with its own unique data and control interfaces. For example, in determining present position, an avionic system may utilize inputs from the gyros, accelerometers, and gimbal angle sensors of an inertial sensor system; position fixes from radar or visual sights; doppler velocity measurements and altitude readings from radar or barometric subsystems; data from active ground- or satellite-based navigation reference systems; plus manual inputs which select modes of operation, identify fixes, etc.

On the output side, an avionic computer may provide commands and data to align, stabilize, and correct an inertial platform from which it obtains velocity and altitude measurements. The overall operation of the radar system is usually computer-controlled, and most FSD systems include computer-driven dynamic situation displays. Ground-based systems, such as SAGE, SABRE, the FAA Enroute Traffic Control System, and various military command and control systems, require special communications networks to interconnect data processing equipment at widely dispersed sites [1, 3].

One current example of such a real-time communications processing system is SACDIN (Strategic Air Command DIgital Network)—designed to provide reliable, secure communications among the geographically dispersed facilities of the Strategic Air Command. The three headquarters commands are linked by SACDIN subnet communications processors to one another and to 16 dispersed base communications processors (BCPs). SACDIN further interconnects the BCPs with 20 aircraft wing command posts and 26 missile base command posts which, in turn, are interconnected to 128 launch control centers.

As an element of the worldwide military command and control system, SACDIN must accommodate a wide variety of message protocols and must interface with a number of different communications systems. SACDIN involves such functions as message organization/processing/accountability/journaling; recovery and reconfiguration upon loss of equipment or interconnectivity; encryption/decryption and overall security of both message traffic and data base; diagnostic capability and status reporting; and data base management and system traffic control [13].

A major challenge in this class of real-time communication systems is to simultaneously provide two somewhat mutually exclusive capabilities:

1. The levels of security—including partitioning, access control, and accountability, as well as encryption—that are a fundamental system requirement in a strategic command and control network.
2. The certainty of access to/by qualified users throughout the network—even in the face of massive losses of equipment and communication links—that is equally essential to the function of a strategic command and control network.

The Saturn V IU program illustrates the range of different I/O requirements that may be encountered in a single real-time application. With more than sixty different pieces of equipment to integrate, the IU involved a massive variety of unique interfaces. A single unit, the IBM-built Launch Vehicle Data Adapter (LVDA), provided an interface for 402 different signals [10].

It is evident that one of the singular and significant realities of real-time systems is the extent to which the user's requirements drive the design. This characteristic has required FSD to be involved in a broad range of technical disciplines that stretch beyond the boundaries of conventional signal and data processing requirements.

Technological implications

FSD's pursuit of real-time systems has involved a wide range of technical disciplines: radar, stellar mechanics,

aircraft and missile flight dynamics, rf antennas, sonar, space navigation, ballistics, inertial alignment, phased-array beam-forming, precision tracking of high-speed aircraft, and the integration and operational debugging of complex on-line, real-time systems. FSD has developed a strong capability in many forms of advanced signal processing, including sonar, precision emitter location systems, emitter classification and identification, synthetic aperture radar, moving-target detection, image processing, Kalman filtering, and seismic data processing [14–17].

Some of this expertise has been put to good use by the rest of the Corporation. A recent example is the IBM 3838 Array Processor, which will be discussed in more detail subsequently. In addition, the major challenges which FSD has faced in real-time control software development have led to substantial contributions to software engineering within IBM [18].

The trend toward standard digital intra-system interfaces has kept FSD at the forefront of emerging technology in fiber optics. Work was complete in 1980 on a Navy contract to develop and demonstrate both a 1-MHz, serial, MIL-STD-1553B-compatible fiber optic data bus [19] and a 50-MHz fiber optic data bus suitable for the forecasted avionic requirements for the 1990 time period [20]. In addition, FSD is actively participating in the drafting of a new military standard for fiber optic data buses [21].

A unique technological ramification of FSD's operational environment is a continuing reliance on and significant progress in magnetic core, drum, and disk storage technology. Many applications include requirements for non-volatility (instant recovery after interruption of power) that can only be met by core main store and magnetic media mass storage [22].

The capacity of a SAGE drum was 0.4 megabits. The FSD drum used on numerous programs since 1970 has a 15-megabit capacity in a much smaller volume and meets the full military specifications (MIL-Spec) range of shock, vibration, temperature, etc. Each 4096-word SAGE core memory required approximately 2.8 m^3 to house the memory with its electronics [23]. The full MIL-Spec core memory in FSD's Modular Computer Series provides 64 000 (32-bit) words in 0.004 m^3, including electronics—an improvement of more than 10 000:1 in packaging density. And, of course, performance, reliability, and power consumption have also improved considerably. In fact, FSD core memory technology development continues to cut the volume, failure rate, and power dissipation of core memories in half every few years.

During the last decade, DOD (Department of Defense) programs were generally followers rather than leaders in the development of mainstream data processing technology, such as integrated circuits. The sheer volume of commercial applications made it far more practical to "hitch a ride" by hardening commercially available technology rather than trying to amortize high development and tooling costs over much smaller DOD procurement quantities.

The advent of VLSI (very large scale integration) is forcing a change in this pattern. Heretofore it has been quite practical to design unique processors using readily available unit logic and the modest levels of integration available to date. But the higher the level of integration, the more specific the function tends to be—and thus the less readily adaptable to multiple applications. At the same time, the characteristics of VLSI are just as critical in opening up new DOD applications as in accomplishing similar objectives for commercial and consumer applications. In fact, the cost, power, reliability, weight, and volume advantages of VLSI are absolutely essential to the practicability and effectiveness in satisfying many future DOD requirements.

The government has recognized this situation and has allocated substantial funding for basic VLSI technology development under its VHSIC (very high speed integrated circuits) and DARPA (Defense Advanced Research Projects Agency) VLSI programs [24]. FSD was given one of the nine contracts awarded to industry for VHSIC Phase Zero government sponsorship. But even before the VHSIC program, the division had recognized the need for a strong VLSI capability and had focused the requisite facilities and skills in FSD Manassas [25]. The objective of FSD's VLSI advanced development program is compatible with that of the VHSIC program: development of submicron technology during the 1980s. In the process, FSD expects to make a significant contribution to IBM's total capability in this key technological area.

Real-time digital processing technology

The problems addressed by computer technology can be characterized by two generic problem types [26]:

- General-purpose processing, somewhat unstructured in nature, and
- Signal processing, which by comparison is highly structured.

FSD develops computers to address both of these generic problem types. There has been a remarkable evolution in these computers through the 1970s as both component technology and organizational technology have experienced continuing improvement. A review of that

Table 1 Representative FSD-developed computers.

Model	*Date of prototype delivery*	*Type of machine*	*Thousands of operations per second*	*Circuit technology (delay time)*	*Degree of MSI*	*Control components (cycle time)*	*Main store (access time)*
AP-1	1971	GPC	360	Standard TTL (11 ns)	Very Low	Hardwired SSI	8K × 18 Core (1 μs)
SP-0	1971	GPC	230	Standard TTL (11 ns)	Very Low	Hardwired SSI	4K × 18 Core (1.3 μs)
CC-1	1973	GPC	740	Schottky TTL (6 ns) introduced	Low	256 × 4 PROM (80 ns)	8K × 18 Core (1 μs)
AP-101	1973	GPC	550	Schottky TTL	Low-Medium	256 × 4 PROM (80 ns)	8K × 18 Core (0.9 μs)
ASP	1975	SP	to 60,000	Schottky & Low Power Schottky TTL (11 ns)	High	1K × 1 RAM (70 ns)	4K × 36 FSU (0.8 μs)
ML-1	1975	GPC	550	Dutchess LSI Custom	(LSI)	512 × 4 PROM (70 ns)	16K × 8 Core (0.85 μs)
ARP	1976	SP	to 20,000	Schottky & Low Power Schottky TTL	High	512 × 4 PROM (60 ns)	1K × 36 RAM (0.07 μs)
ML-0	1977	GPC	550	Schottky & Low Power Schottky TTL	High	512 × 4 PROM (60 ns)	16K × 36 RAM (0.85 μs)
IBM 3838	1977	SP	to 30,000*	Schottky TTL	High-Very High	1K × 1 RAM (70 ns)	8K × 36 FSU (0.8 μs)
AP-101C	1978	GPC	600	Schottky TTL	Very High	2K × 8 PROM (90 ns)	32K × 18 Core (0.8 μs)
CC-2	1980	GPC	2000	Super Schottky TTL (3 ns)	Very High	1K × 1 RAM (40 ns)	32K × 18 Core (0.8 μs)
Series/1 (MIL)	1980	GPC	350	Dutchess LSI Custom	(LSI)	512 × 8 PROM (85 ns)	64K × 18 DRAM (0.66 μs)

Legend: GPC—general-purpose computer.
SP—signal processor.
*—floating-point operations.
First-level package = circuit carrier, typically flatpacks.
Third-level package = card interconnection, typically multi-layer backpanel.
Dutchess is IBM's name for a 100-TTL-circuit-per-chip technology.
MSI—Medium-Scale Integration.
LSI—Large-Scale Integration.
TTL—Transistor-Transistor Logic.
DRAM—Dynamic Random Access Memory.
FSU—Functional Storage Unit (semiconductor memory).

evolutionary process should aid perception of two of FSD's more recent development efforts:

- The IBM Advanced System/4 Pi CC-2 general-purpose computer, and
- The IBM 3838 Array Processor.

Table 1 lists a number of significant computers developed by the division in recent years. If one were to characterize these members of the IBM System/4 Pi family of avionic computers by performance, four categories could be formed:

- Low-performance (SP-0, ML-0) general-purpose processors, generally embedded in a subsystem such as complex I/O control/multiplexor or displays—emphasizing low power, volume, and weight rather than performance as the key parameters.
- Medium-performance [AP-1, AP-101, ML-1, AP-101C, Series/1 (MIL)] general-purpose processors, typically used as the central computer of an avionics system. The price/performance of these machines has tracked the improvements experienced with general-purpose machines (Fig. 1).
- High-performance (CC-1, CC-2) general-purpose processors used in command/control systems. In addition to the obvious benefits of increased speed and density in both logic and memories, these machines have also taken advantage of advanced organization techniques to provide higher levels of performance.
- Signal processors (ASP, ARP, IBM 3838), whose performance is several orders of magnitude greater than general-purpose processors as a result of the nature of the signal processing problem and the willingness to spend hardware to achieve very high performance. The

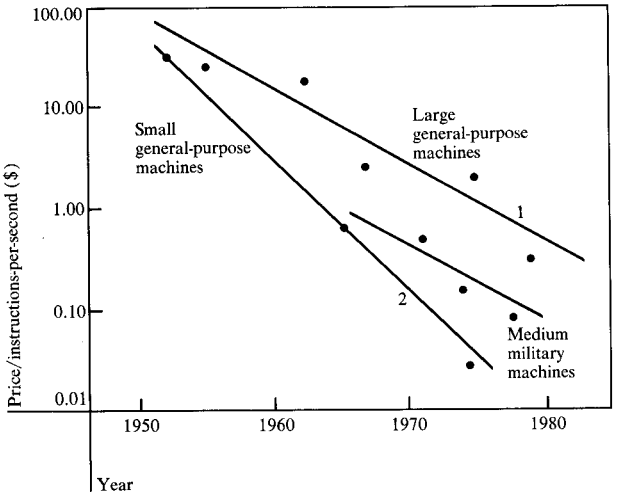

Figure 1 Computer price/performance trends. Curve 1 represents an average improvement for large general-purpose machines of 15% per year; Curve 2 represents an average improvement for small general-purpose machines of 25% per year.

contrast between high-performance general-purpose processing and signal processing will be described in greater detail subsequently.

The advance of technology through the 1970s can be seen in the data presented in Table 1. The technologies listed are those employed in the prototype hardware. Frequently the storage technologies, both control store and main store, have been retrofitted in production.

- *Logic technology*

Logic technologies have seen marked improvement in performance and, more importantly, in circuit density. Schottky devices were introduced early in the 1970s and offered a doubling of performance but at higher power dissipation. The need to constrain power in many military and space applications motivated the introduction of low-power Schottky devices. More recently, advances in circuit geometry have permitted continued improvement in the circuit speed-power product, particularly the introduction of high-performance Super Schottky.

- *Memory technology*

Neither of the two elements of memory technology, main memory and control memory, have seen performance improvements to match those of logic technology. Both have, however, seen dramatic improvement in density, as discussed earlier. Most DOD real-time applications have required non-volatile memory. However, the cost, performance, and volume advantages of monolithic memory have become so compelling that DOD users are exploring such means as battery-backup power, memory hierarchies, and fault-tolerant memory organization to take advantage of these benefits.

The increased usage of microprogram control has been a result of several factors. Foremost was the availability of a cost-effective technology beginning in 1972 with reliable programmable read-only memory (PROM). Although the integration level of PROMs has evolved from the original 256 × 4-bit chips to the current 2K × 8-bit chips (K = 1024), the performance of these devices has held fairly constant, probably due to the dimensional constraints of the programmable cells. Those seeking higher performance for microprogram control have used static RAM, which offers comparable density and improved performance but unfortunately is volatile and requires supporting IMPL (initial microprogram load) logic.

The advantages of microprogram control have typically been ascribed to the flexibility it offers in implementing custom functions. Of greater importance to the computer designer is the regularity afforded by microprogram control. Control logic (as opposed to data flow logic) tends to be irregular, complex, unsuitable to increased integration levels, and subject to high probability of engineering change. The attractiveness of microprogram control regularity resulted not only in increasingly horizontal microwords (*i.e.*, using many bits to directly control data flow elements, rather than imposing combinational logic between an information-dense microword and the data flow elements), but also in the use of PROMs and PLAs (programmable logic arrays) wherever possible to replace combinational logic.

- *Packaging technology*

The increasing circuit integration levels (MSI, LSI, PROMs, RAMs, PLAs) and the desire to pack more function into available volume produced new problems in component cooling and interconnection. About 160 integrated circuits on two multi-layer boards sharing a frame and a 196-pin connector could be mounted on a 4 Pi page or card. Heat was conducted from the page frame to the cooling plenum through a pair of ears with limited cross section. The maximum power dissipation allowable (to keep junction temperatures below 125°C with conductive cooling) was about 20 W. As power density increased, several approaches to cooling evolved, including integral heat exchangers, air flow through the page frame, larger thermal surface contact area, and, when possible, direct air impingement on the components. The current IBM Advanced System/4 Pi Modular Computer Series (MCS) page permits indirect cooling of up to 40 W by employing a pair of wedge-locked surfaces.

The technology evolution just described has culminated in a pair of products which exemplify the merging

of organization and technology. Both the IBM 3838 and the CC-2 designs illustrate the impact of technology on organizational issues and the organizational approaches to coping with the limitation of technology.

- *Signal processing*

Perhaps the most challenging and significant work done by FSD in special digital processors has been in applications involving signal processing. The signal processing problem typically involves repetitive, highly structured computations on very large data sets. To do this in real time requires very high throughput—tens of millions of floating-point operations per second in some cases. To provide this level of performance under the size, weight, power restrictions, and operating environment encountered in military applications is extremely challenging.

This challenge has been successfully met by a combination of tactics. First of all, the highly structured nature of signal processing tasks has allowed generality to be traded off for optimized performance. The AN/BQQ-5 sonar signal processors designed in 1970 were basically hardwired fast-Fourier-transform (FFT) array processors whose input and output data structures were fixed. Subsequent FSD products, such as the Advanced Signal Processor (ASP) [27], used on several different military contracts, and the IBM 3838 Array Processor [17], have been programmable processors designed for a range of signal processing applications.

The Advanced Signal Processor is an IBM product developed primarily for sonar applications and has been designated the DOD standard signal processor, AN/UYS-1. Its sonar applications include operation in long-range patrol aircraft, fleet protection helicopters and destroyers, and in submarines. Other applications include ground data processing of Air Force and NASA satellite data. The IBM 3838 Array Processor is a floating-point commercial derivative of the ASP. A wide range of signal processing algorithms are microprogrammed into its highly efficient and pipelined arithmetic processors, including recursive and finite impulse response filters, fast Fourier transforms, envelope magnitude detection, and quadratic interpolation.

These designs also reflect the fact that many of the operations being performed are independent from one another—such as an element-by-element vector sum. This allows both pipelined computation to increase the throughput of a given processing element and parallel processing elements to achieve the desired total processing capacity.

In other applications, advanced statistical processing techniques have been used with general-purpose computers to overcome limitations in input signal quality due to overt energy interference, operating range, practical constraints on the size and sensitivity of airborne or spaceborne sensors, and phenomena with inherently poor signal-to-noise ratios. One of many examples that could be cited is the work in Kalman filtering done in conjunction with the Safeguard Anti-Ballistic Missile (ABM) program. Techniques were developed by IBM to greatly improve tracking capability with a given processing capacity through the use of extended Kalman filters with adaptive tuning and chi-squared validation techniques using corrected covariance. These developments were supported by IBM's own tools and methodologies for filter design and system simulation evaluation [28].

Reliability and availability

The generally accepted definition of reliability is the probability that the system will perform satisfactorily for a specified period of time when operated within its specified environmental conditions [29]. In the early 1950s, when FSD entered into defense business, it was revolutionary to see this performance parameter specified.

When it became intuitively obvious that single equipments could not satisfy performance demands, massive redundancy of equipment was utilized. The SAGE system required continuous operation around the clock to monitor airspace coverage; loss of the system for a failure and subsequent repair time was intolerable. Therefore, two systems capable of performing the same function were placed on line, thus negating the problems associated with a single failure. The small probability of loss of two systems at the same time was addressed through overlapping coverage from adjacent sites. Since there were few constraints applied on the design regarding weight, volume, and power, the system redundancy solution was acceptable.

In the avionics world, these constraints became more meaningful. While the airborne mission was much shorter in time and noncontinuous in nature, the technology of the day (vacuum tubes) combined with the complexity of the system designs raised grave concerns about the ability to satisfactorily complete a mission. Initially, these concerns were addressed by redundancy in the deployment of aircraft.

In the mid-1950s, R. Mettler performed a study for DOD in which he quantified the probabilistic nature of the reliability problem and focused attention on this parameter in future system designs. A joint government-industry advisory group on reliability of electronic equipment

(AGREE) was formed. The work pioneered by this committee led to the evolution of reliability from an art to the technical discipline known today.

The decade of the 1960s brought FSD into the missile and space age. For missile guidance hardware, the most critical design parameters were light weight, low power, and computation accuracy. Required computational speeds did not demand state-of-the-art breakthroughs; however, the environmental considerations did demand solid state componentry (in that era, germanium devices with proven reliability).

The advent of manned spaceflight led to the most stringent reliability requirements ever placed on computer hardware, *i.e.*, a probability of success of 0.99 for a mission duration of 250 hours [30]. To satisfy this requirement, a simplex computer would require a mean-time-between-system-failure of 25 000 hours, which was not achievable with state-of-the-art technology. A unique design employing triple modular redundancy with intermediate "voting" was developed for Saturn V which permitted individual piece-part failures to occur without affecting the correct system output. This design was packaged in a single lightweight frame fabricated from magnesium-lithium, and incorporated internal fluid cooling to maintain semiconductor junction temperatures less than 40°C for reliable device operations. By packaging the redundant computer into a single unit, significant savings in weight and volume were achieved.

Another significant reliability achievement in space applications was the design of the processor and the large memory for the Orbiting Astronomical Observatory [31]. This unmanned vehicle was required to operate for one year in orbit. A unique redundancy design was employed at the circuit level, using a quad-component arrangement which tolerated shorts or opens in individual components. The systems were launched and operated error-free for four years until shut down by ground command.

In the late 1960s and early 1970s, significant technology changes were being incorporated into hardware design. Logic circuitry with about five gates per chip was common in 1965. During the 1970s, MSI (medium scale integration) ranging from 30 to 100 gates per chip was employed in avionics computers. By the mid-1980s, logic densities of 20 000 gates per chip will be applied in military computers, with a corresponding improvement in per-gate failure rates. The higher-density circuits have also permitted fault-detection circuitry covering 99% of computer faults to be incorporated within the critical weight, power, and volume restrictions associated with many military applications.

But despite tremendous improvements in reliability, failures will still occur. And many real-time systems involve processes too critical to allow a failure to disrupt normal operation. The Space Shuttle onboard flight-control system provides an excellent example. It controls the spacecraft through all mission phases, including re-entry and landing [32]. Once again, redundancy is a necessity.

The Space Shuttle flight control system must satisfy a NASA requirement of fail operational/fail safe (FO/FS). This means that there is to be no impact on system performance in the event of a single failure and that the system must provide a safe return even after two failures.

A total of five identical computers are used. Four of these run identical programs and are fully synchronized. By comparing outputs, a failed computer can readily be detected, isolated, and eliminated from the system. The remaining three computers can then cope with the possibility of yet a second failure by comparing outputs in the same manner. The fifth machine runs a different backup program which protects against the possibility of a generic failure in the identical software used by the four primary computers.

Comparison of outputs among the four primary machines is performed by the computers themselves, with each of them passing its output data to one other computer for comparison. Under the assumption of non-simultaneous hardware failures, agreement between any two computers provides assurance that both are current. When there is a failure, the pattern of agreement/disagreement among comparison pairs easily isolates the faulty machine.

Synchronization is maintained on a software, rather than hardware, basis. Each of the four primary computers informs the others when it is ready to begin the next task in the common sequence they are all executing. No computer proceeds with a task until the others are also ready to proceed with it.

On Space Shuttle, all data communication between system elements occurs via 24 independent data buses and each computer has access to all 24 buses. For flight-critical data, these are used in redundant sets of four buses with each of the four controlled by a different computer. When one computer intends to read input data, it prenotifies the other three, then commands the input. All four computers thus receive identical, simultaneous inputs from each sensor, eliminating the need for any correction or interpolation.

In addition, all critical sensors are provided in redundant sets of three, each controlled from a different com-

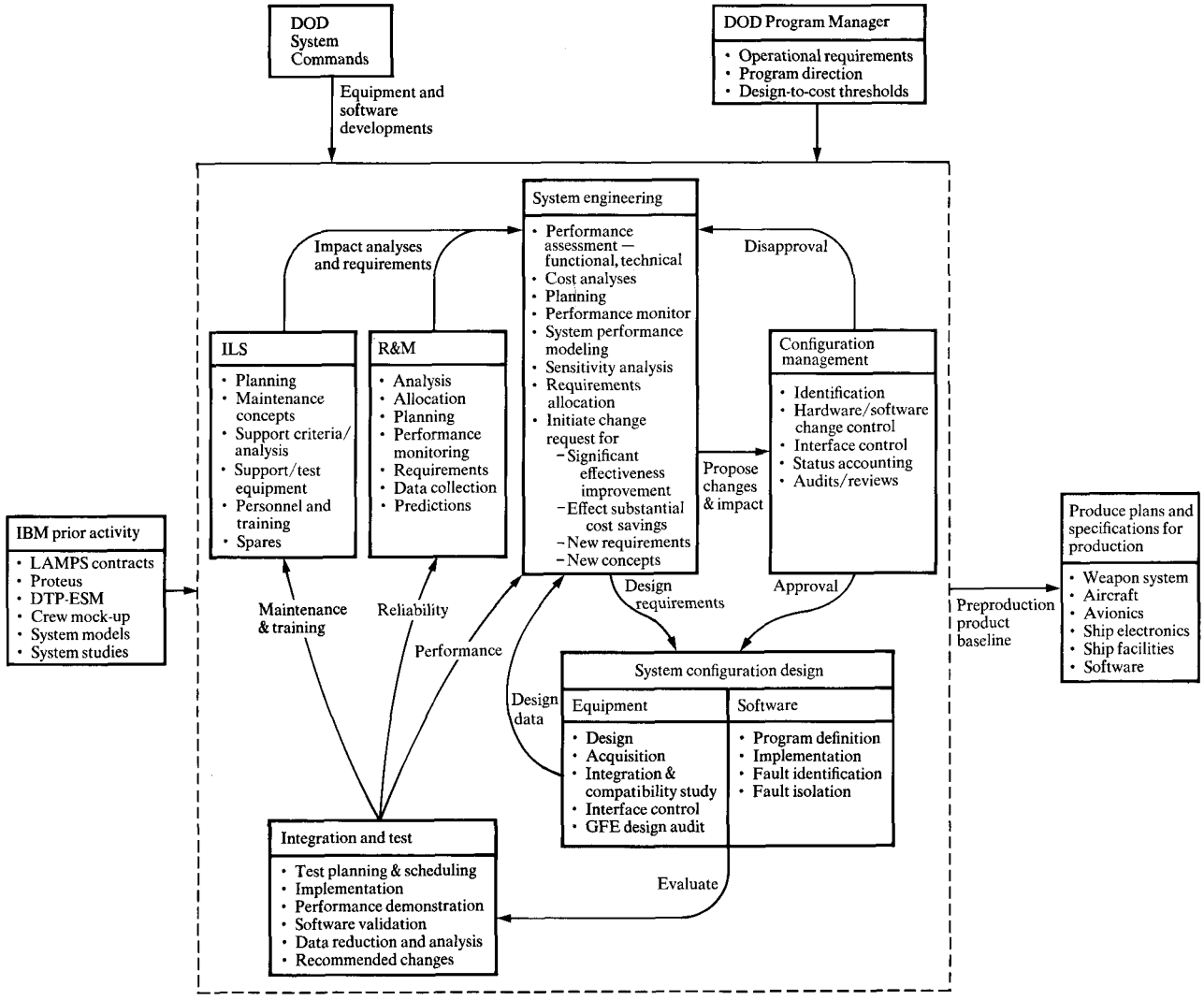

Figure 2 Role of the system prime contractor. ILS—Integrated Logistics Support; R&M—Reliability and Maintainability; DTP—Design To Price; ESM—Electronic System Management; GFE—Government Furnished Equipment.

puter. Since all buses can operate simultaneously, and the start of each task is synchronized, all three sensors are read at the same time. This arrangement allows for detection, isolation, and elimination of a failure anywhere in the system: computer, data bus, or sensor.

Total responsibility

Much of FSD's business consists of delivery of products (hardware, software, subsystems) to the government or another contractor. The involvement in other programs is different: As SPC (system prime contractor), FSD is responsible to the government for all aspects of system performance, from development to deployment and field operations, throughout the life of the program. SPC responsibilities consist of many or all of the following:

- Total system performance—including design, development, and delivery and field support of the system.
- Specification of interfaces between associate contractors.
- Design, development, and procurement of avionics/electronics and supporting software.
- Integration in the laboratory.
- Testing and evaluation of the total system in the field.
- Specification of reliability and maintainability system requirements and assurance that they are met.
- Development of integrated logistic support (ILS) requirements and establishment of a program to ensure support in the field.

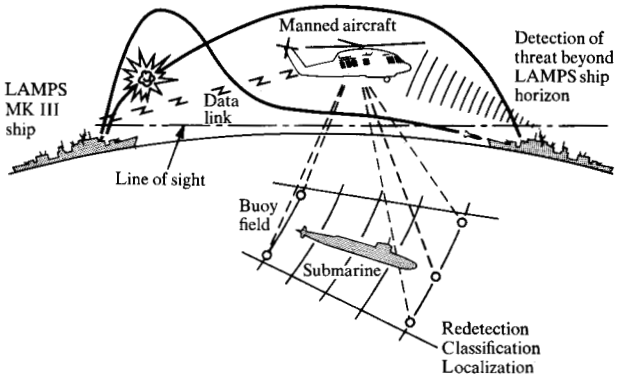

Figure 3 LAMPS MK III Weapon System—mission concept.

- Definition of training requirements and development of a training program, including acquisition and turnkey operation of training devices.
- Cost and technical performance tracking and reporting.
- Control and accountability for total system configuration status (change control of hardware and software).

Any major system must be developed through an iterative process of analysis, development, integration, and testing culminating in a complete set of validated specifications and plans for the production phase.

IBM's objectives in the integration of a major system, possibly encompassing avionics, air vehicles, shipboard electronics, and support facilities, plus a variety of technical and management disciplines and interfaces, is to ensure that the system

- meets the required operational objectives;
- satisfies the design-to-cost boundary conditions and provides minimum life-cycle costs, including the indirect costs of manning and logistics;
- minimizes risk relative to performance requirements, predicted availability, cost thresholds, and schedule milestones;
- provides visibility to the government and utilizes related government expertise and developments.

Attainment of these objectives is a significant challenge which can only be satisfied by establishing and executing, on a timely basis, the proper system engineering plan and methodology which allows 1) definition of the complete requirements for each of the subsystems and interfaces with proper consideration to constraints of cost and risk; and 2) early integration, test, and evaluation to either verify performance or identify problems in time for corrective action to be initiated.

In the development phase the SPC performs the following role: implementation of the development test program; documentation and planning for the production programs; management coordination and technical support for the government program manager; and support of government test programs.

The interrelationship between the tasks required to successfully design/develop/integrate and test the LAMPS weapon system is illustrated in Fig. 2. In essence, the SPC must act in the interest of the DOD agency in all matters in order to ensure orderly progression of the system development program through the major phased-procurement milestones [Defense System Acquisition Review Council (DSARC)] leading to the introduction of a new mission capability into the DOD inventory. The LAMPS program provides the best example of the technological complexity and the types of activities involved when FSD is called on to accept total responsibility for a major military undertaking.

LAMPS program

Early in 1974 FSD was selected as the SPC for the Navy's LAMPS MK III program. FSD is responsible to the Navy for the total performance of the LAMPS MK III weapon system, which embodies the integration of the parent ship (frigate, destroyer, cruiser) and the manned aircraft (SH-60B Seahawk helicopter) operating from that ship for both Anti-Submarine Warfare (ASW) and Anti-Ship Surveillance and Targeting (ASST) missions (Fig. 3).

The LAMPS III weapon system performs the four classical phases of the ASW problem (detection, localization, classification, and attack) in an interlocking manner, in which the ship does the initial detection and classification, and its aircraft accomplishes redetection, localization, reclassification, and attack. Information sharing, by means of a wide-band duplex data link between the parent ship and the helicopter, commences when the helicopter is launched. The data link is synchronized, and navigation is initialized relative to the ship position when the helicopter is first airborne and prior to transit to the threat area. As sonobuoys are deployed, the acoustic data are transmitted along with radar or electronic warfare information by data link to the ship for processing. These data are also processed on board the helicopter. Command and control, though maintained by the ship, can be delegated to the helicopter after contact is established and the target is being tracked by the airborne unit. Final localization and attack are accomplished independently by the helicopter using its total acoustic and nonacoustic sensor onboard capability.

In the ASST mission, the LAMPS aircraft provides a mobile elevated platform for observing, identifying, and

localizing threat platforms beyond the parent ship's horizon. Primary sensors used in the ASST mission are radar and electronic warfare support measures equipment. Thus, the effective surveillance, detection, and targeting ranges of the parent ship are greatly extended to permit targeting of platforms that might launch a missile attack. The helicopter performs ASST at significant distances from the threat platform to minimize its vulnerability to attack.

• *System integration requirements and challenges*

The LAMPS MK III weapon system posed system integration challenges of a degree and complexity that mandated primary emphasis on this design parameter during development. The problem was compounded by having to check out new computer programs in parallel with the introduction of new data processing and display equipment and newly defined interfaces, both in air and ship systems. Both IBM and the Navy recognized the importance of utilizing formal documentation to ensure successful integration both within the LAMPS system and with major ship systems with which LAMPS must interface.

The LAMPS ship and air system is comprised of eight computers and 140 black boxes weighing approximately 900 kg on the helicopter and 3200 kg on board the ship. A total of almost 600 000 words of operational and maintenance software is resident in eight different computers. An additional 600 000 words of simulation software was required. The major subsystems in LAMPS MK III include the following:

- Navigation—Teledyne AN/APM-217 Doppler radar set, Collins AN/ARN-118 TACAN, and Texas Instruments AN/APS-124 radar set.
- Communications—two Collins AN/ARC-159 UHF radio sets for line-of-sight, and one Collins AN/ARC-174 HF radio set for over-the-horizon.
- Acoustics—Hughes AN/UYQ-21 shipboard acoustic display, and two EDMAC Corp. AN/ARR-75 radio receiving sets for sonobuoy signals.
- Magnetic Detection—Texas Instruments AN/ASQ-81 magnetic detecting set including a towed magnetometer.
- Data Processing—two IBM Proteus AN/UYS-1 processors to process acoustic data aboard the aircraft and the ship, two Control Data Corporation AN/AYK-14 standard airborne computers, and two Univac AN/UYK-20 standard shipboard computers. In addition, one Univac AN/UYK-7 standard shipboard computer is required in the Combat Direction System (CDS).

The data link, which moves data simultaneously in both directions, consists of a Sierra Research Corporation AN/ARQ-44 radio set in the aircraft with two directional antennas and Sierra's AN/SRQ-44 set on board ship with a high-gain directional antenna. The data carried include clear or secure voice, secure computer, radar/IFF or acoustic data, and sonobuoy command tones.

In order to facilitate the software development and integration of hardware and software, FSD set up a facility which includes a System/370 computer to provide tactical conditions for land-based test operations and to simulate sensors and interfaces prior to operational hardware delivery. This facility has subsequently been identified as the "LAMPS Land-Based Test Site" by the Navy. A sizeable number of Navy personnel are resident, both for training purposes and also to validate the operational and technical testing being performed. Other facets of the Land-Based Test Site facility include

- Sonar signal processing and display laboratory.
- Avionics subsystem integration laboratory, where prime hardware from 25 contractors is integrated and tested. It is configured so that eight sensor subsystems, which go on the helicopter, can be independently tested or integrated into one system.
- Shipboard laboratory, which is a simulated combat-information center containing four operator consoles and their associated electronics, which are used to evaluate operator functions and to validate shipboard software, and also can be interconnected with the avionics bench or a helicopter in flight.
- Air system master bench, a full-scale mockup of the Seahawk's cabin area. It has been used to train Navy crews, to integrate mission avionics hardware and software, and to test performance.
- Hangar, landing pad, and control tower, which are used to house two Seahawk helicopters for avionics installation and checkout and functional flight test operations. A realistic antisubmarine warfare mission can be flown from Owego, New York, using the ship laboratory both for functional evaluation and crew training.

The first flight took place in December 1979 [33] and the combined ship/air weapon system performance demonstration took place during the last three weeks in February 1980. The third week was used by the Navy to try to "break" the system; it could not be broken. Since then, a total-weapon-system test has been completed and testing by the Navy has begun. Throughout the history of this project as well as others mentioned in this paper, IBM has striven to fulfill the role of a responsible system developer.

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