# Wire Length Distribution for Placements of Computer Logic

It is shown from simple theoretical considerations that the distribution  $f_k$  of wire lengths for a good two-dimensional placement on a square Manhattan grid should be of the form  $f_k = g/k^{\gamma} (1 \le k \le L)$  and  $f_k \approx 0 (k > L)$ , where  $\gamma$  is related to the Rent partitioning exponent p by the equation  $2p + \gamma \approx 3$ . Three placements were investigated and the distribution functions for wire length were found to follow the above relationships.

#### Introduction

In the layout of integrated logic circuit chips, particularly for VLSI applications, a major portion of the physical space of the chips is required for interconnection routing. Theory and experimental results have been developed [1, 2] which allow an approximate prediction of wiring space requirements. This work is based upon the so-called "Rent's Rule," [3, 4] which relates circuit count to I/O count. We take this work one step further and use a rather crude theoretical derivation and experimental study to develop a wire length distribution relationship. This result is important for calculating average results for circuits, which depend not on average length but on other averages, as for example average inverse length. In particular, we find that the distribution function is given by

$$f_k = g/k^{\gamma} \qquad (1 \le k \le L)$$

$$\approx 0 \qquad (k > L), \tag{1}$$

where  $f_k$  is the fraction of wires with length k; g is a normalization constant; L is a constant related to the size of the array and adequacy of the placement; and  $\gamma$  is a constant characteristic of the logic.

We find that L is of the order of W/2, when the size of the array is  $W \times W$ . The Rent relationship [3, 4], which was used to develop the wire length relationship in the earlier work [1] and was experimentally verified for a number of graphs [3], states that the average number of terminals T per complex of C circuits is given by

$$T = AC^{p}, (2)$$

which gives us another constant, p (which we shall call the Rent constant), characteristic of the logic complex. We find, both from simple theoretical considerations and experimental results, that

$$\gamma \approx 3 - 2p. \tag{3}$$

In this context it should be noted that M. Feuer [5] found that Rent's Rule can be derived by using the distribution law of Eq. (1) with Eq. (3).

Equation (1) is of the form of the Pareto-Levy distribution [6] when  $1 \le \gamma < 3$ ; similar laws occur in many contexts, e.g., word frequencies, noise in transmission channels, and many others. Like the Gaussian distributions, however, they have the property that their convolutions are again Pareto-Levy distributions; however, they do not have finite second moments, and for  $\gamma \leq 2$ , not even finite averages; in our case, however, the truncation at k= L ensures that both first and second moments are finite, even if they may be extremely large. Table 1 shows the asymptotic behavior of moments which may be observed from our results [we use Eq. (3) to relate  $\gamma$  and p]. Relatively large second moments are indicated for wire length, even if the average wire length is small, as when p < 0.5. I believe that the distribution log presented here depends on the chip following Rent's rule and on the placement algorithm optimizing wire lengths as far as possible. However, even if the placement algorithm does not optimize completely, the large second moments derived here probably still hold true.

Copyright 1981 by International Business Machines Corporation. Copying is permitted without payment of royalty provided that (1) each reproduction is done without alteration and (2) the *Journal* reference and IBM copyright notice are included on the first page. The title and abstract may be used without further permission in computer-based and other information-service systems. Permission to republish other excerpts should be obtained from the Editor.

The fact that a large fraction of the wires have long wire lengths has a significant impact on system performance, since circuits with long wires tend to be slowed down; such an impact has been observed in practice [7]. Unfortunately, Dansky does not give the full distribution of the wire lengths in the nets, so the distribution law of his net lengths cannot be determined from the results presented in that paper. However, the long tail observed by him is suggestive of a distribution law similar to that given in this study.

### **Mathematical considerations**

We develop here a crude derivation of Eq. (1). In previous work [1, 2], a formula for average length distribution was derived using Rent's Rule and a hierarchical placement method. Essentially, this consists of dividing a square array of cell locations into four equal square arrays. One knows then, from Rent's Rule, the number of connections crossing boundary lines. Each of the four areas is again subdivided into four equal areas and the logic partitioned to fit into those four areas. This is continued until the individual areas are individual elements of the original logic.

Let us denote by  $t_K$  the number of terminals for a complex consisting of K elements (in units, modules, cards, etc.). Then [3, 4]

$$t_{\kappa} = AK^{p}, \tag{4}$$

where p is the Rent exponent and A the number of terminals per individual complex. Let C be the number of elements to be placed and  $T_K$  the total number of terminals for K-sized groups. Then

$$T_K = AK^pC/K$$
$$= ACK^{p-1}.$$
 (5)

Denote by  $N_K$  the number of connections crossing boundaries of K-sized groups; denote by  $\alpha_K$  the number of connections per terminal for nets connecting K-sized groups; then we have

$$N_{\kappa} = \alpha_{\kappa} A C K^{p-1}. \tag{6}$$

Note that  $0.5 \le \alpha_K \le 1$  and that it does not introduce significant error to assume that  $\alpha_K$  is constant; *i.e.*,  $\alpha = \alpha_K$ .

Secondly, we may compute the number of connections between K-sized groups not connecting groups of size 4K, as

$$\Delta N_{K} = N_{K} - N_{4K}$$

$$= \alpha C K^{p-1} (1 - 4^{p-1}). \tag{7}$$

We note that these connections tend to have an average

Table 1 Asymptotic behavior of distribution moments.

p γ a		m <sub>1</sub> (first moment average wire length)	m <sub>2</sub> (second moment)		
>0.5	<2	$\approx L^{2p-1}$	$\approx L^{2p}$		
=0.5	=2	$pprox \log L$	$\approx L^{2p}$		
<0.5	>2	f(p)	$\approx L^{2p}$		

Table 2 Placement results.

Graph ID	Node count	No. of connections	Array size	Exptl. Ř	p	$0.57 \times \bar{R}_{theor.}$
(A)	2146	7302	48 × 48	3.53	0.7	4.30
(B)	576	1383	24 × 24	2.98	0.7	2.99
(C)	528	1046	24 × 24	2.20	0.5	2.29

length of roughly  $\sqrt{K}$ ; we may consider these connections to be distributed among the lengths  $\sqrt{K}$  to  $2\sqrt{K} - 1$ , so that, if  $n_k$  is the number of connections of length k, then

$$\sqrt{K} \le k \le 2\sqrt{K} - 1$$
:  $n_k \approx CK^{p-1}(1 - 4^{p-1}) / 2\sqrt{K}$ .

Actually, we note  $k \approx \sqrt{K}$ , so we may write very crudely

$$n_k \approx \alpha C k^{2p-2} \frac{(1 - 4^{p-1})}{2k} ,$$
 (8)

or, if  $f_k$  is the fraction of wires with length k, then we may write

$$f_k = k^{2p-3} / \sum_{k=1}^{L} k^{2p-3}, \tag{9}$$

with L being an upper bound on k. This crude argument leads us then to Eq. (1). No value for L is derived; we do note that it should be of the order of  $\sqrt{C}$ .

#### **Experimental results**

Studies were carried out on three graphs:

- (A) A graph representing high-speed logic studied previously by Landman and Russo [3] and denoted there as L2; its Rent exponent was found to be 0.75.
- (B) A 572-node graph, which was partitioned out of graph (A); its Rent exponent was found to be 0.75.
- (C) A 524-block graph representing a hand calculator logic chip. Its Rent exponent was found to be 0.59.

The graphs were placed using the hierarchical placement program developed earlier [8]; distances were obtained as shown in Table 2. The placement for (A) was, as com-

153

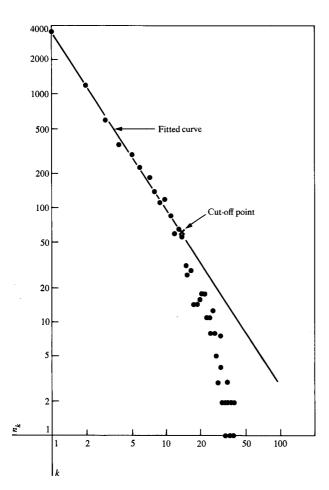


Figure 1 Graph (A): plot of  $n_k$ , number of connections of length k, versus k.

pared to the theoretical  $\tilde{R}$ , better than either of the other two graphs; however, the algorithm was allowed to do a far better job in that case than in either of the other two cases.

The wire length distribution from placement is given in Table 3. A fit was done to the first k points such that at least 95% of all the wires were included; the equation to be fitted was

$$\log n_k = \log A - \gamma \log k, \tag{10}$$

and a least-squares method was used. The plots in Figs. 1 and 2 show that for k > L there is a rapid drop in  $n_k$  below that predicted by the fitted equation; we approximate this by saying that for k > L,  $f_k$  is zero. Table 4 holds the results for fitting Eq. (1) for  $\gamma + 2p$ , where the standard deviation is also given. APL plots of the data with the computed curves are included in Figs. 1 and 2 on a log-log scale. The fit is adequate in all cases for the first set of points. In agreement with the crude theory described in the introduction,  $\gamma + 2p$  is quite close to 3 in all cases.

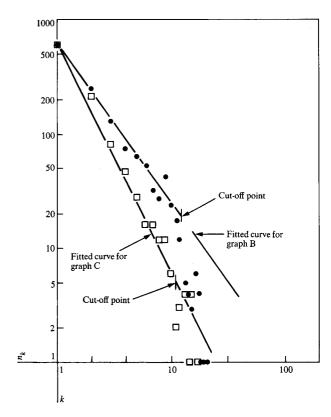


Figure 2 Graphs (B) and (C): plot of  $n_k$ , number of connections of length k, versus k.

We consider briefly the case of an exponential distribution; we would then find that  $n_{k+1}/n_k$  is roughly a constant; however, Table 5 shows the values found for the three cases. The fact that this ratio increases with k makes this kind of distribution unlikely. Other kinds of distributions (e.g., Poisson) would yield a decreasing ratio with k, so such distributions are even more unlikely.

## **Acknowledgments**

I would like to thank W. R. Heller for suggesting the study of this problem, and both Heller and R. L. Russo for encouragement and support. I am indebted to W. F. Mikhail for many fruitful discussions of this work, a careful reading of this document, and suggestions for the improvement of the presentation.

## References and note

- W. E. Donath, "Placement and Average Interconnection Lengths of Computer and Systems," *IEEE Trans. Circuits and Systems* CAS-26, 272-277 (1979).
- W. R. Heller, W. E. Donath, and W. F. Mikhail, "Prediction of Wiring Space Requirements For LSI," Proceedings of the 14th Design Automation Conference, New Orleans, 1977, pp. 32-43.
- 3. B. S. Landman and R. L. Russo, "On a Pin or Block Relationship for Partitions of Logic Graphs," *IEEE Trans. Computers* C-20, 1469-1479 (1971).

Table 3 Wire length distributions.

k	$n_k$	k	$n_k$	k	$n_k$	k	$n_k$	k	$n_k$
				Grap	h (A)				
1	3480	11	84	21	18	31	6	42	1
2	1206	12	60	22	18	32	2	44	1
3	615	13	66	23	11	33	2	45	1
4	369	14	56	24	11	34	1	46	1
5	309	15	33	25	8	35	2		
6	233	16	26	26	12	36	3		
7	194	17	29	27	8	37	1		
8	141	18	15	28	5	38	2		
9	111	19	15	29	3	39	1		
10	119	20	16	30	4	40	2		
				Grap	h (B)				
1	605	6	51	11	17	16	6		
2	250	7	32	12	12	17	4		
3	129	8	26	13	5	18	1		
4	75	9	42	14	4	20	1		
5	65	10	24	15	3	29	1		
				Grap	h (C)				
1	592	6	16	11	2	17	1		
2	219	7	16	12	3	21	1		
3	82	8	12	13	4	25	1		
4	46	9	12	14	1				
5	29	10	6	15	3				

Table 4 Results for fitting distributors.

Graph ID	Graph No. of Log ID points fitted		Α γ		$\gamma + 2p$		
(A)	L = 14	$3.55 \pm 0.04$	1.55 ± 0.05	0.75	$3.05 \pm 0.04$		
<b>(B)</b>	L = 12	$2.79\pm0.07$	$1.48 \pm 0.09$	0.75	$2.98 \pm 0.09$		
(C)	L = 9	$2.82\pm0.08$	$1.91\pm0.06$	0.59	$3.09 \pm 0.06$		

**Table 5** Distribution ratios  $(n_{k+1}/n_k)$ .

	Graph (A)	Graph (B)	Graph (C)
k = 1	0.35	0.41	0.37
k = 2	0.51	0.51	0.37
k = 3	0.61	0.58	0.56
k = 4	0.82	0.87	0.63
k = 5	0.76	0.79	0.54

- W. E. Donath, "Equivalence of Memory to 'Random Logic,' "IBM J. Res. Develop. 18, 401-407 (1974).
   M. Feuer, "Connectivity of Random Logic," Proceedings of the Workshop on Large-Scale Networks and Systems, IEEE 1980 Symposium on Circuits and Systems, Houston, TX, pp.
- 6. Application of such distributions is characteristic of much of the work of B. Mandelbrot, who was very helpful in introducing me to the necessary subject matter. See for example B. Mandelbrot, "Self Similar Error Clusters and Communications Systems and the Concept of Conditional Stationarity," IEEE Trans. Commun. Syst. COM-13, 71-90 (1965); and P. Levy, Theorie de l'Addition des Variables Aleatoires, Gauthier-Villars, Paris, 1954.
- 7. A. H. Dansky, "Bipolar Circuit Design for a 5000-Circuit VLSI Gate Array," IBM J. Res. Develop. 25, 116-125 (1981, this issue).
- 8. W. E. Donath, IBM Tech. Disclosure Bull. 17, 3121-3125 (1975).

Received October 14, 1980; revised December 8, 1980

The author is located at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598.