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A High-Density Bipolar Logic Masterslice for Small Systems

A new high-density bipolar logic masterslice which uses a simple Schottky Transistor Logic (STL) circuit cell as its basic building block is presented in this paper. The STL cell is derived from Integrated Injection Logic (I^2L). The use of low-barrier Schottky diodes for AND logic, as diodes function in Diode Transistor Logic (DTL), makes possible achieving the NAND circuit operation. A brief description of the Schottky diode fabrication process is also given. A new concept of contact hole personalization is introduced and is shown to be an efficient approach to masterslice design as well as a factor in achieving high cell density. Due to the unusual structure of the basic cell and the arrangement of the cells in the masterslice, a new physical design methodology was developed for the design of different part numbers, corresponding to unique logic functions, on this masterslice. The STL circuit operates with a 1.7-V power supply and yields a typical delay of 3 ns at 0.5 mW and 5 ns at 0.15 mW. The I/O circuits are TTL-level compatible. The cells, the circuits, the unique features of the masterslice, and its application in an I/O controller chip are described.

Introduction

A typical conventional integrated Diode Transistor Logic (DTL) three-way NAND gate [Fig. 1(a)] requires four diodes, three resistors, and one transistor, and all devices except resistors must be individually isolated. The approach to masterslice design (for example, see [1]) would have all the diffusion processes completed and contact holes protected by a layer of platinum before the wafers are held in stock for custom wiring or personalization. A typical DTL cell layout [Fig. 1(b)] would have extra "blank" areas for "wiring channels" for interconnections between circuits.

We investigated various techniques for improving circuit density, in particular the cell structure of Integrated Injection Logic (I^2L). The highly integrated nature of the I^2L cell [2, 3] lends itself very readily to a densely packed cell array. Using the integrated technique, we designed a cell based on a conventional npn transistor in which six low-barrier Schottky diodes (LBSD) are in-

tegrated at its collector (the barrier height is approximately 0.5 V) [4]. The basic cell and circuit schematic are shown in Fig. 2. The basic cell contains two resistors and one transistor with six LBSD. The NAND logic function is accomplished by wiring together the anodes of LBSD from different logic blocks to the input (base of the npn transistor) of another logic block (Fig. 3).

This simple circuit is called Schottky Transistor Logic (STL). The masterslice which uses the STL as the basic cell has been fabricated. This STL circuit is a saturating circuit with a measured typical switching speed of about 3 ns at 0.5 mW and about 5 ns at 0.15 mW. This chip uses both a 5-V and a 1.7-V power supply. The 1.7-V supply for the internal circuits, which can be generated on the chip with a regulator circuit, provides a better power/delay product-enhancing performance. A typical chip with 1300 circuits wired dissipates about 1 W. It operates over a junction temperature range from 10–100°C.

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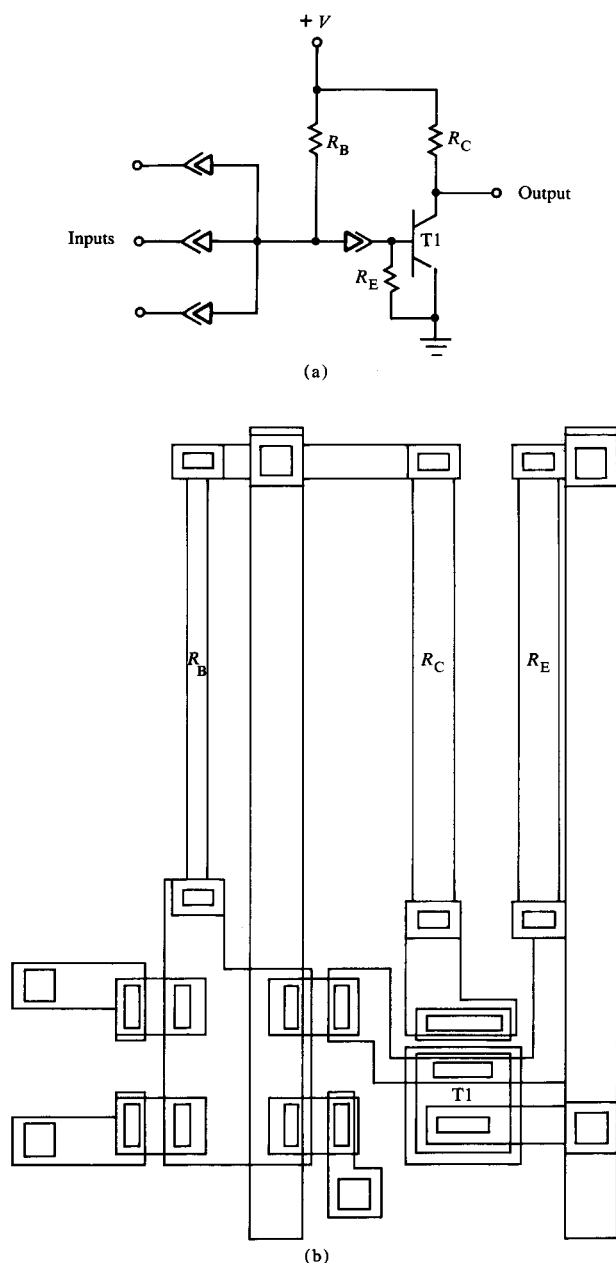


Figure 1 (a) DTL circuit schematic; (b) cell layout.

This STL cell is slightly larger than an I^2L cell but offers significant speed improvement [5]. It also offers better logic implementation and higher fan-out capability. The STL cell and chip layout offer significant density improvement over a typical Transistor-Transistor Logic (T^2L) or DTL cell layout. To enhance the masterslice wireability, some new physical design schemes, such as a wire-through cell technique, cell depopulation schemes (allocating certain cell areas for wiring channels), and personalization at the contact level, were implemented to im-

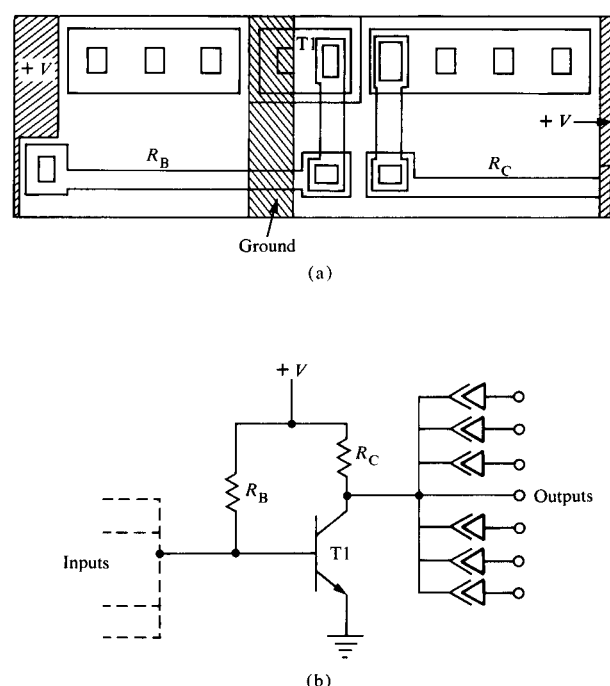


Figure 2 (a) STL cell layout; (b) circuit schematic.

prove the chip density, resulting in 1200–1300 NAND gates being wired on a chip of 4.7×4.7 mm; these schemes are detailed in the paper. The STL design, therefore, can provide a high-density, low-cost, relatively high-performance gate array chip for application in small computer systems.

Masterslice and process description

• Masterslice design

The STL logic chip is a high-density masterslice (Fig. 4). The chip has four basic cell types: internal cell (I-cell) for internal logic and off-chip receiver circuits, external cell (E-cell) for off-chip drivers in push-pull or open collector configuration, clamp diode cell (CD-cell) for clamp diodes, and a voltage regulator cell (VR-cell) for an on-chip voltage regulator.

The cells are organized in 35 columns by 104 rows. Column C-0 contains 28 E-cells plus a VR-cell. Column C-34 contains 30 E-cells. Each of the columns C-1 through C-33 contains 98 I-cells and four CD-cells. (The six rows are used for internal second-level power distribution with clamp diode cells designed under the four inner rows of power buses.)

The I-cells, the basic building blocks of the STL masterslice, are arranged in groups of four. Thus, almost the entire area of the chip is utilized to provide these unit

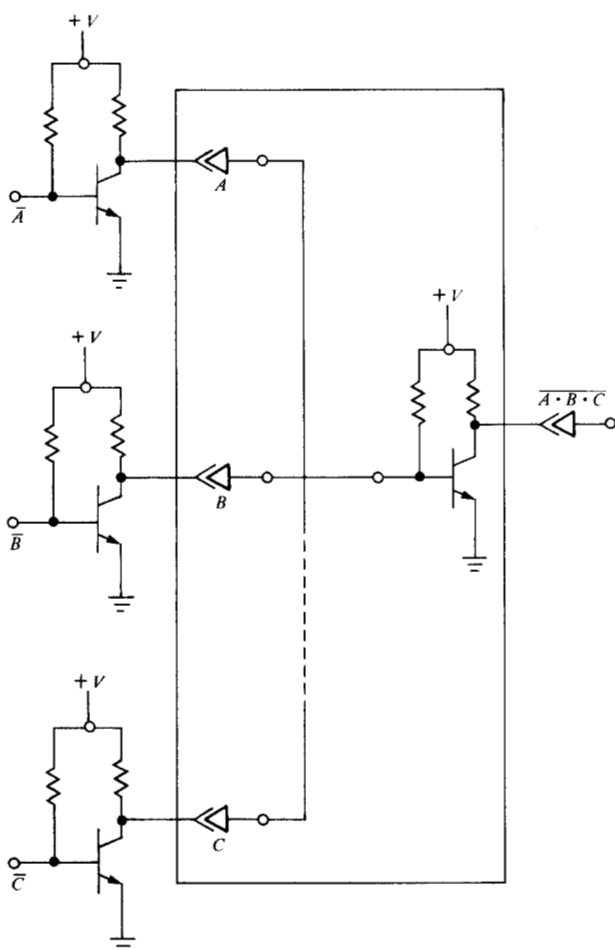


Figure 3 NAND logic function.

cells. The STL masterslice contains 3234 I-cells, 58 E-cells, 132 CD-cells, and one VR-cell with a chip size of 4.7×4.7 mm.

To facilitate ease in diagnostics for fault detection in functional testing, the chip must be designed using the Level Sensitive Scan Design (LSSD) techniques [6]. The logic designer generates a set of input test patterns with the associated expected output states, and the logic tester steps through these input patterns and detects the outputs for logic "faults."

After testing, the wafers are diced and good chips are picked out and stored in chip banks. Each chip has 122 lead-tin pads arranged in a partially populated 13×13 array. The chip is "flip-chip" mounted on a 28-mm 116-pin ceramic substrate. Ninety-six I/O pins are available for logic input/output connections.

• Process description

The STL masterslice discussed here uses the same semi-

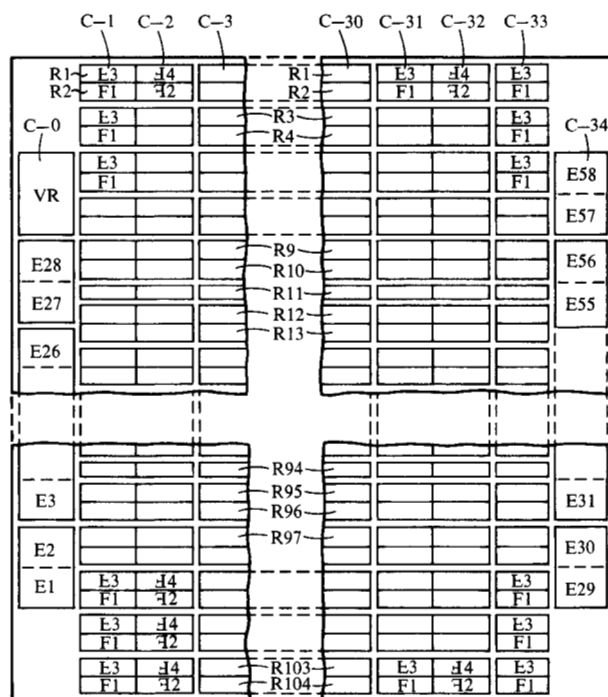


Figure 4 STL masterslice image. C-0 through C-34 designate 35 columns. R1 through R104 designate 104 rows.

conductor technology as the circuit masterslice (termed 704) used in the IBM 4300 systems [7]. It is a bipolar process with a $2\text{-}\mu\text{m}$ -thick epitaxial layer and three levels of alternating metal and insulator. Figure 5 shows the top and cross-sectional views of the basic STL cell. At the point illustrated, all the diffusions have been completed, and all the contact holes have been opened through the oxide and nitride, except for the LBSD anodes, which are protected with SiO_2 . The subsequent Pt deposition allows only PtSi to form in the opened contacts.

Next, a noncritical "block-out" photoresist mask is used to expose the LBSD anodes and allow the oxide to be opened during a BHF dip etch. To define the first metal pattern, a lift-off structure [8] consisting of consecutive layers of polysulfane, photoresist underlay, resin glass, and a top coat photoresist is applied to the wafer. The pattern is exposed and developed into the photoresist top coat, and a reactive ion etch process follows which removes the resin glass photoresist and polysulfane under the developed areas. A quick-dip etch is used to remove any residue or native oxide from the contact holes. The wafer is now ready for metal deposition.

The wafer is loaded into an evaporator and a layer of Ta is deposited through the lift-off mask. The Ta-Si interface forms the LBSD [9]. The conducting metal, aluminum-

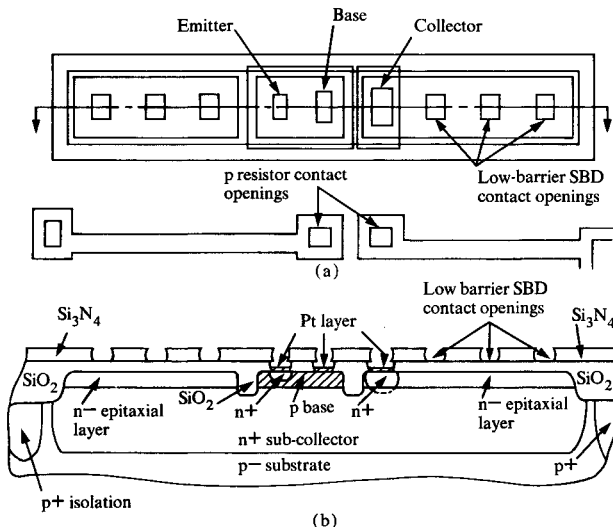


Figure 5 (a) Top and (b) cross-sectional views of STL device.

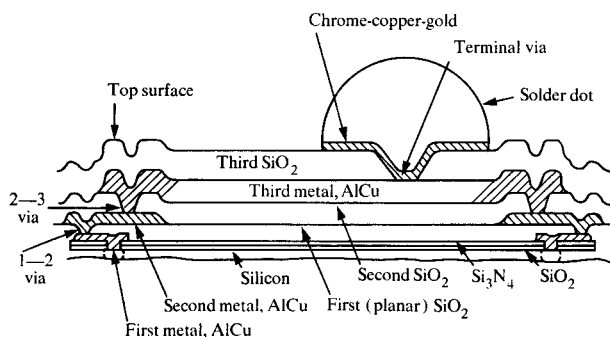


Figure 6 Three levels of metallization and terminal metal.

copper, is then evaporated over the Ta layer; the lift-off structure is subsequently stripped, leaving behind only the conducting metal patterns.

A layer of planar SiO_2 is sputtered on the wafer (Fig. 6). A photo process and oxide etch defines and opens the first metal to second metal via (internal level metal contact hole) patterns. Subsequently, another lift-off process, similar to that performed on the first metal, is administered to define the second-metal pattern. At the second metal only AlCu is used. A second layer of SiO_2 is sputtered over the wafer and a similar via etch is processed. Next, the AlCu is blanket-evaporated and the third-metal pattern is subtractively etched. A final layer of SiO_2 is deposited and the terminal via pattern is defined and etched. The terminal metallurgy consists of layers of chrome, copper, and gold, with lead-tin solder, which is evaporated through a metal moly mask. After the Pb-Sn reflowing the process is complete and the wafer is ready for final testing (Fig. 6).

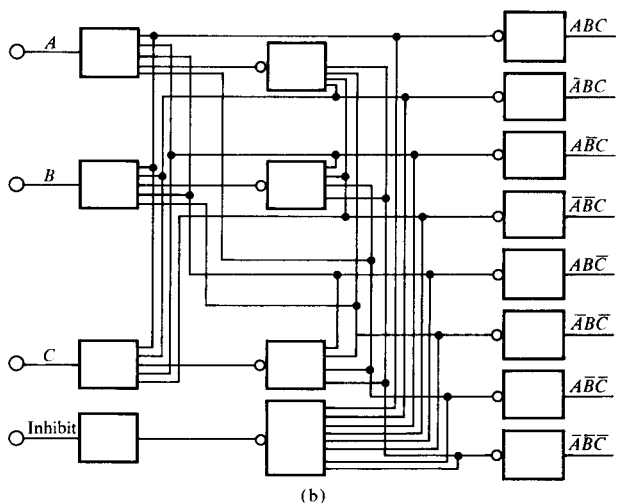
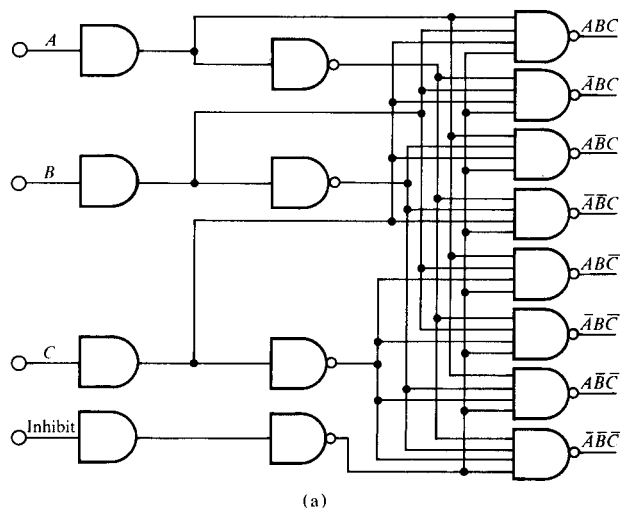


Figure 7 A 3 to 8 decoder with inhibit function: (a) logical representation; (b) physical representation.

• Chip "personality" design

A customized set of circuits ("books") are pre-wired using I-cells or E-cells. These "books," each with its assigned unique name, are stored in the IBM Engineering Design System [10]. The "books" are designed by using an Interactive Graphic Design System [11] to interconnect the devices to form circuits. Each design must conform to rigid design system rules such that it can be automatically checked for errors or violations.

The IBM Engineering Design system is a comprehensive software system used by IBM engineers to implement their logic design, simulation, and physical wiring of the chip for a particular logic function. The logic is coded in standard NAND gates format and the Engineering Design System programs convert the logic information to physical equivalents (Fig. 7) and proceed to place the

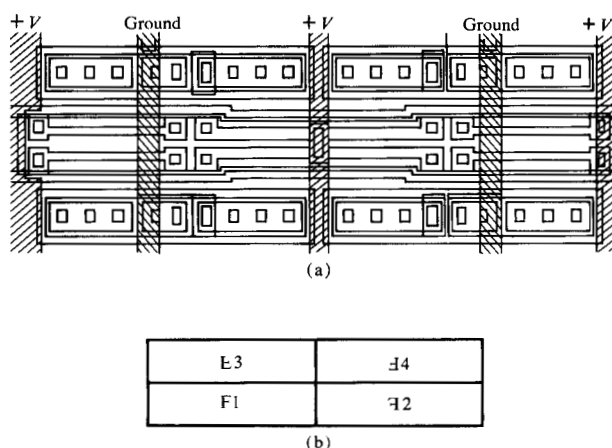


Figure 8 (a) Four-cell group; (b) orientation of cells within group.

"books" on the masterslice array matrix. Next, the Engineering Design System programs interconnect the "books" to realize the desired logic functions.

Due to the "brick-wall" structure of the I-cells, no additional area is allocated for wiring channels. Wiring channels are made available by not placing "books" over cells where wiring channels are needed. This is the reason for customizing or personalizing at the contact hole level.

For a typical part number, about 1300 circuits are wired on a chip. After the physical design is completed, the Engineering Design System programs provide a check of the physical data against the original logic design to ensure that no error exists. The physical data are then processed for masks or direct-write electron-beam processing [12, 13].

Cell and circuit description

Internal cell (I-cell)

The basic building blocks of the STL masterslice are arranged in groups of four. Each cell is designed to utilize a minimum of semiconductor area and has a unique geometrical orientation with respect to the remaining three cells of its group. This geometrical orientation is shown in Figs. 4 and 8. Each of the four rectangles shown in Fig. 8(b) contains an I-cell represented by the alphabetic letter F varied in the orientation. The I-cell is 120 μm in length and 42 μm in width for a ground rule dimension of 3.0 μm .

The internal circuits are operated with a 1.7-V power supply. The reason for choosing a low voltage supply for these circuits is to obtain improved performance by reducing the circuit voltage swing. Figure 9 shows the mea-

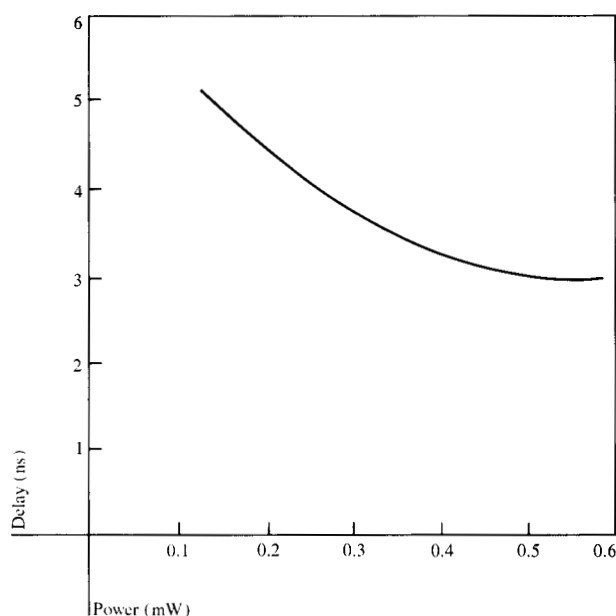


Figure 9 Power delay curve of internal circuit.

sured power/delay curve for these internal circuits; note the point corresponding to a 1.7-V supply yielding the stated performance of 3 ns delay at a power dissipation of 0.5 mW. However, this lower voltage swing results in a noise margin for the on-chip circuit of 50 mV, which is quite adequate for on-chip circuit operation. In contrast, off-chip circuits have a noise margin of several hundred mV which is required to overcome transmission line reflection and crosstalk on the second-level package.

The I-cell circuit (Fig. 2) performs the AND-Invert function. The logic operation is accomplished by steering the current from resistor R_B . If one or more of the input signals to the base of the transistor T1 is at the down level, T1 is cut off and the output signal at the anodes of the LBSD is at the up level of 0.8 V. When all of the input signals to the base of T1 are at the up level, the input diodes are reverse biased and T1 is conductive, and the anodes of the LBSD are at the down level of 0.4 V. An AND function of the STL circuit is generated by wiring together diode outputs from different circuits. These diodes are actually formed in the collector region of the driving gate transistor. The base of the transistor is the input of the driven gate. Figure 3 shows a multi-way NAND function, with a conventional logic primitive with multiple inputs and single output contained within the rectangle.

The STL circuit performance can be further improved by incorporating an integrated high-barrier Schottky diode (HBSD) between base and collector of the switch-

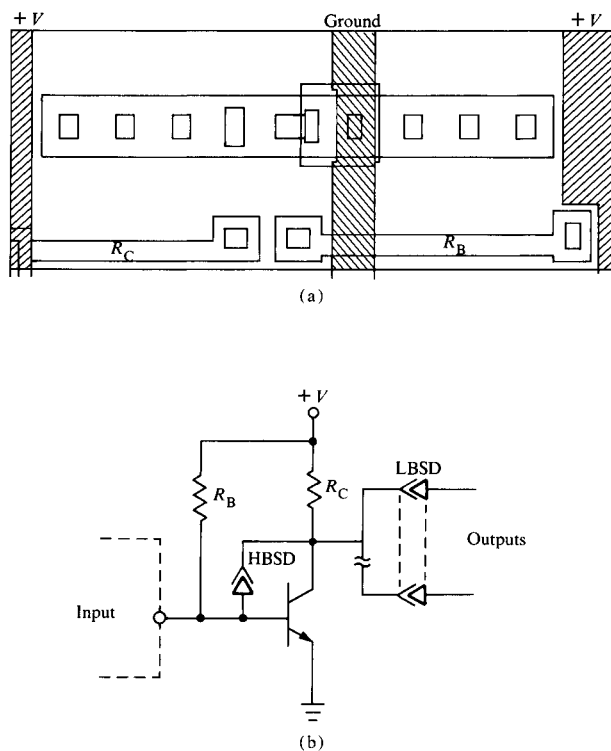


Figure 10 (a) Cell layout and (b) circuit schematic of STL with clamp diode.

ing transistor. This prevents the transistor from entering saturation and, therefore, improves the switching speed of the circuit without increasing the power dissipation. The cell size has to be increased slightly to accommodate the clamp diode. Figure 10 shows the layout and the circuit schematic.

Two I-cells may be personalized to provide an STL off-chip in-phase receiver, as shown in Fig. 11. A great number of these receivers can be placed on the chip in a wide range of locations; this flexibility enhances the placement and wiring of the chip.

To enhance the STL masterslice wireability, the transistor from the I-cell can be used as a group of six remote Schottky diodes. These diodes are used to reduce wiring congestion by placing the fan-out point close to a group of circuits driven from a common source (Fig. 12). The cell being used for remote diodes has only the cathode (collector) and the anode contact holes opened. The base, emitter, and resistor contact holes are not opened and these areas can be used for wiring channels.

• External cell (E-cell)

Two columns of E-cells are located on the left and right of the STL masterslice. E1 through E58 are actually structured as 29 pairs of E-cells. Adjacently positioned cells,

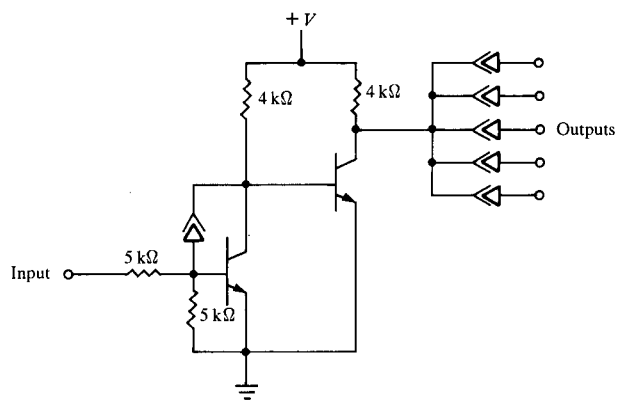


Figure 11 Off-chip receiver circuit.

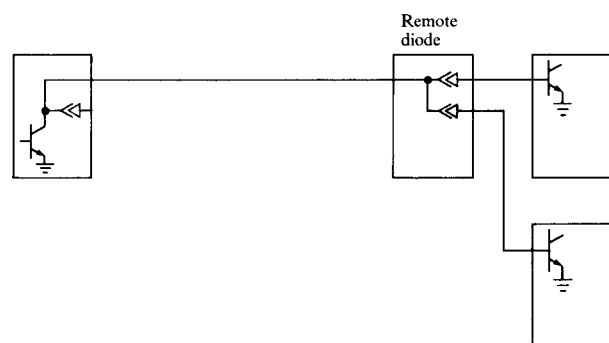


Figure 12 Remote Schottky barrier diodes to reduce wiring congestion.

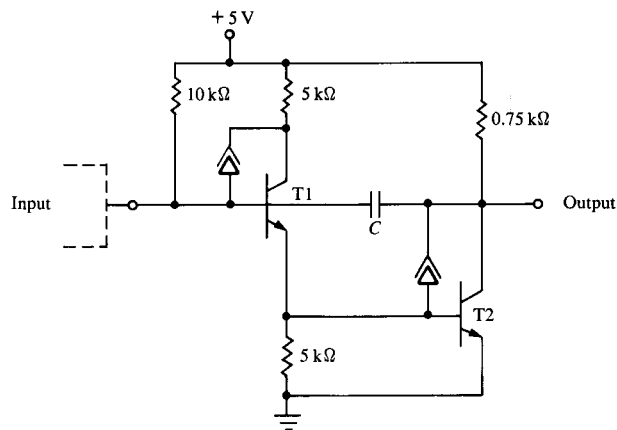


Figure 13 Open-collector driver.

e.g., E1 and E2, are a pair, as are cells E3 and E4, etc., through E57 and E58. Each pair of E-cells contains six transistors, nine resistors, and two capacitors. The cell pair may be configured as two open-collector drivers (Fig. 13), or one push-pull driver (Fig. 14) and one open-collec-

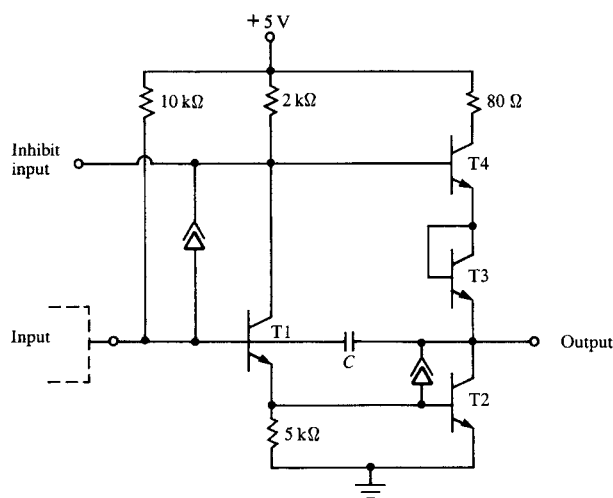


Figure 14 Push-pull driver.

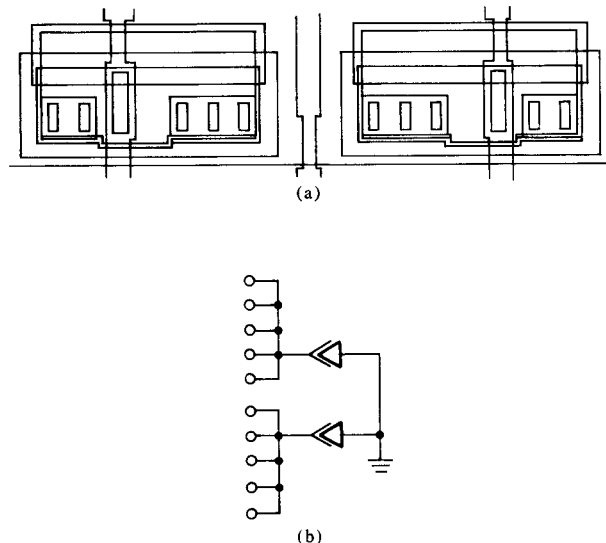


Figure 15 (a) Clamp diode cell layout and (b) device schematic.

tor driver. This is because there is only one set of devices for active pull-up on the push-pull driver. Therefore, the STL masterslice can only provide a maximum of 29 push-pull drivers and 29 open-collector drivers or a total of 58 open-collector drivers.

These drivers convert the on-chip logic levels of 0.4 to 0.8 V to standard T^2L levels of 0.3 to 5.0 V. The circuits perform the NAND function. An AND function is accomplished by wiring together diode outputs (Schottky diode anodes) from different circuits to the input of the driv-

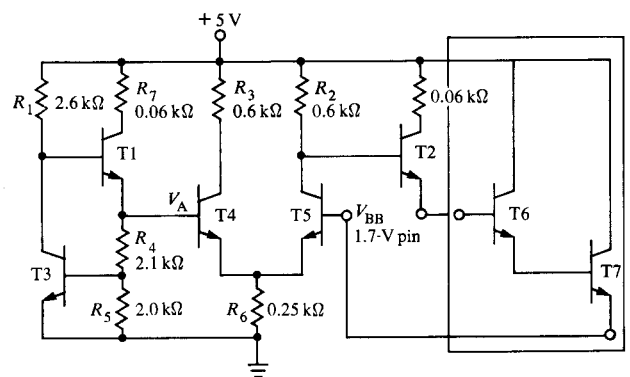


Figure 16 Voltage regulator circuit.

er circuit. The output is up when one or more of the inputs is at a down level, and the output is down when all inputs are at an up level. Capacitor C is used to slow down the output falling transition time and to reduce the unwanted inductive ground shift.

When T2 turns on, and if the output is falling too fast, the capacitor C takes away part of the base drive from T1. This slows down the transient base drive to T2, which in turn slows down the falling transition time at the output. The push-pull driver has the added feature of active pull-up for a faster rise-time. The base of the active pull-up transistor T4 is available as an inhibit input. This together with the AND input (both at down level) will put the driver output at a high impedance state.

• Clamp diode cell (CD-cell)

The purposes of the clamp diode are 1) to minimize the negative undershoot amplitude at the receiver input due to impedance mismatching; and 2) to reduce the chances of damaging the chip packaged in a module due to unwanted electric static discharge from mishandling. Figure 15 shows the layout of two CD-cells and their relative orientation. Each rectangle represents a unit CD-cell. The clamp diode cell contains a Schottky barrier diode in parallel with a parasitic pn junction diode. The diode has five separate selectable cathode contacts and one grounded anode. By personalizing the contact hole and metalization layers, the cathode is opened and connected to the input of the receiver and chip I/O.

• Voltage regulator cell (VR-cell)

The referenced voltage regulator is located at the upper left corner of the chip. It occupies the same area as a pair of E-cells. It contains five transistors and seven resistors. These devices may be personalized to provide an integrated on-chip voltage regulator. The schematic of this circuit is shown in Fig. 16.

The dc voltage of V_{BB} is set by the voltage at node V_A through a matched pair of transistors T4 and T5. Node voltage V_A can be designed by adjusting the ratio of R_4 to R_5 such that $V_A = [(R_4 + R_5)/R_5] \times V_{BE}$ of T3. V_{BE} (T3) can be determined by adjusting the device size of T3 and the value of R_1 . Thus, the V_{BB} of the circuit can be determined approximately an order of magnitude less than the tolerance of the 5-V power supply. T2 is a current amplifier which provides additional current to drive the off-chip Darlington transistor pair T6 and T7. This Darlington is capable of providing large amounts of current to the chip without increasing the chip power dissipation. This circuit offers a very economical way to provide a low voltage supply needed for the internal circuits when one may not be available in the system.

Physical design considerations

The physical design of a logic chip is done through the use of a series of automatic programs in the IBM Engineering Design System. Because the physical representation of the STL logic does not conform to the standard NAND gate structure used by logic designers and shown in Fig. 7, the initial task is to convert the logic input to a physical representation. The physical description of the part number takes the form of a logic list and the appropriate pre-wired physical "books" which are selected from a circuit library of previously designed and constructed macro blocks. The circuits occupy from one to sixteen STL I-cells or one E-cell depending upon the circuit function. The nature of the STL design allows a high degree of flexibility in the selection of circuit location on the internal grid. This small cell size is achieved because the cells occupy the entire wiring plane and because the contact holes are personalized to facilitate the usage of unoccupied cells for wiring channels.

Use of the wire-through cell (*i.e.*, a cell with a small amount of internally fixed wiring, allowing global wiring through the cell area), coupled with the ability to swap Schottky outputs to the extent of collectors dotting for remote Schottky diodes, provides significant flexibility for the interconnection of vertical lines. This, plus the ability to provide cell depopulation (removal of cells) in regions which have heavy wiring traffic, provides increased wiring capacity for this masterslice.

The aspect of a smaller cell size for circuit placement allows the use of highly specialized algorithms for making local adjustments in placement. This adjustment consists of depopulating areas of high wiring density and providing wiring streets where they are needed based on the type of random logic being implemented [14]. Another attractive feature of the STL design is the availability of the remote Schottky diodes. If wiring congestion occurs in one area

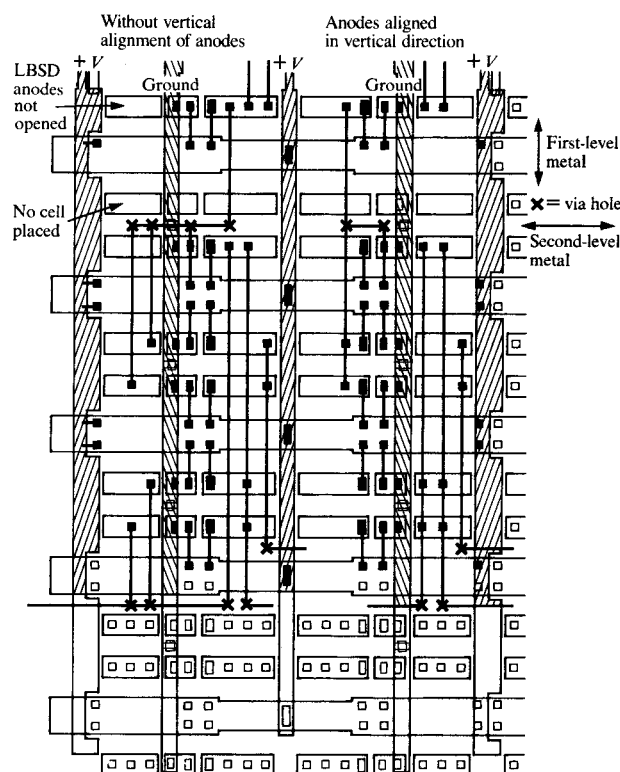


Figure 17 STL wire-through cell with and without vertical alignment of LSBd anodes.

of the chip, the use of remote Schottky diodes can dissipate the congestion by transferring some wiring to less congested areas. This capability at placement time allows for a higher degree of freedom in the use of connection length reduction algorithms and offers areas for new exploration in program development.

In order to interconnect the STL logic automatically, special algorithms were developed to utilize both depopulated cells and occupied cells for wiring. The wire-through cell allows the use of channels with no Schottky anodes wired for global wiring (Fig. 17). By means of careful swapping of outputs one can align connections in the vertical direction to maximize wire density; this, coupled with a two-directional line pack (a method of wiring: first the vertical plane is packed, using a line-packing algorithm to achieve maximum density vertically. The horizontal direction is then packed, based on the vertical wiring.), provides for a high degree of wire density. However, some redefinition of the I-cell can provide for even greater densities in the future. We have learned from this design that the use of a line of contacts is effective but the wireability of the cell could be increased significantly by adding two additional free channels in the vertical direc-

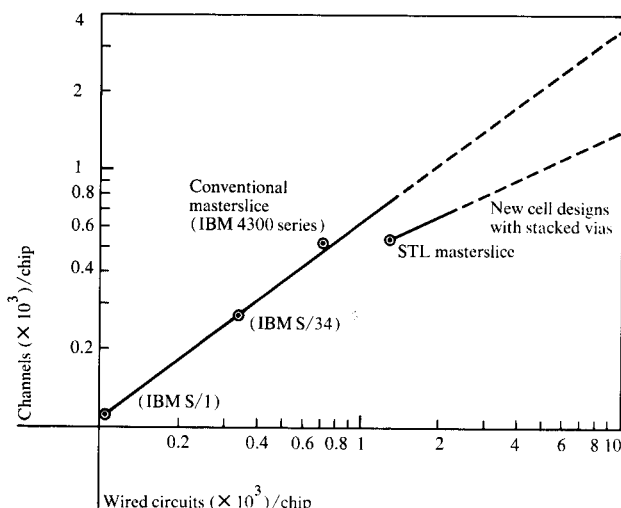


Figure 18 Wired circuit density versus wiring channels.

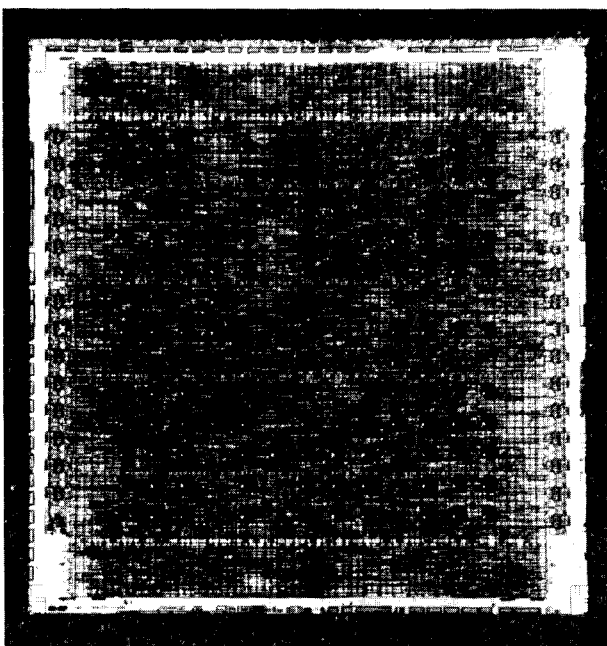


Figure 19 I/O controller chip.

tion and two in the horizontal direction [15]. This compromise, so to speak, in the direction of wiring "bays" allows a great reduction in wiring congestion and provides the masterslice image with an opportunity to be fully populated.

Additionally, the use of stacked vias is a significant improvement in the wireability of chips. This allows the addition of another metal plane which enhances the wireability by 20 to 30%. Without the ability to stack vias (see Fig. 6) directly on top of one another, the third plane has

little value since two wiring channels would be required for each level change. The combination of these improvements results in significantly higher density. The graph depicted in Fig. 18 shows the possible improvement.

Applications

The masterslice described above is technologically advanced and offers a significant amount of flexibility to the system designer. Using the IBM Engineering Design System, a large number of custom-wired logic chips can be designed and fabricated. One of the parts fabricated is an I/O controller. This device contains an 8-bit-wide ALU and an 18-bit-wide instruction with parity checking. There are also two 13-bit control store address registers, one for each program level, 6-bit program status word, 9-bit selector, and random control logic circuits. This I/O controller chip is being used in the IBM System/38 to control various I/O devices. The I/O controller uses 1626 I-cells, 55 E-cells, 40 CD-cells, 1 VR-cell, and 92 signal I/Os. Implementation of this chip requires 3746 connections and 7253 vias; the metallization needed for global wiring of the chip is 66 cm and 106 cm for the first- and second-level metal, respectively.

Figure 19 is a photograph of the I/O controller chip. The depopulated 13×13 array of lead-tin balls are used to join the chip to the ceramic package.

Summary

This STL masterslice provides 3234 internal cells, of which a typical part would contain 1200-1300 equivalently wired NAND gates. The masterslice approach permits system designers to design as many custom-wired parts as required without the very long turnaround time of custom design and certainly at much less cost. The STL chip of this paper is a relatively small chip, 4.7×4.7 mm, yet it provides over 1200-1300 NAND gates with 96 I/Os. The new concept of contact hole personalization in conjunction with the brick wall organization of the cells, the allocation of unused cells for wiring channels, and wire-through cell capability are responsible for the high cell density achieved. The very compact cell structure and the use of low-barrier Schottky diodes are the main reasons for the reported performance of this chip.

Acknowledgment

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