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Delay Regulation—A Circuit Solution to the Power/Performance Tradeoff

This paper introduces the concept of delay regulation as a means of controlling circuit delay variations from chip to chip, which is especially important in VLSI products. An embodiment of this concept which applies a phase-locked loop to individually control chip performance and power is presented together with computer-simulated results of an example design. It is shown that accurate delay equations and the potential for improved product yield result from application of the concept. The circuit overhead for large circuits is shown to be negligible. Application to a wide range of logic circuit types is also described.

Introduction

Continuing improvements in both lithography and the control of process steps in the manufacture of integrated circuits have resulted in shortened logic and array circuit delays and reduced power dissipation. However, manufacturing variability dilutes these improvements by causing designers to specify a machine based on the longest delays and the hottest (fastest) chips. Many factors contribute to this variability: process steps, such as mask alignment and silicon doping, power supply voltage, power distribution, and operating temperature [1]. These factors affect the characteristics of the devices in the circuits or their operating conditions and are included in a delay equation (an analytic expression for logic gate delay), and thus variations in these factors result in a distribution of delay values. The equation typically yields a tolerance on the computed delay values of ±50%. Reference [2] gives an example of a system which has tolerances of this magnitude. The designer is thus required to partition the critical circuit path (a serial connection of circuits which has a delay that determines the machine's maximum operating speed) on multiple chips to maximize the statistical advantage of manufacturing differences; this partitioning statistically minimizes the overall path delays and tolerances. If the critical path were contained on one chip, machine performance would be determined by the circuit performance of that chip and its tolerances.

Future machines will have higher levels of integration, and therefore the practice of statistically averaging delay paths will no longer be viable. In an extreme case, one-chip machine performance is determined by the slowest acceptable chips. The situation is illustrated in Fig. 1, which shows three chips with nominal, best-case (fast chip), and worst-case (slow chip) performance. Given the same input to the three chips, one finds three different path delays. Clearly, the product specification is determined by the slow chip, which penalizes the nominal and fast product. The VLSI dilemma is this: On a chip, if one circuit is slow, all circuits are slow; in a VLSI machine, if one chip is slow, the machine is slow.

The motivation behind the concept of delay regulation presented in this paper as a solution to the VLSI problem is to vary the power in a circuit in order to achieve the desired delay [3]. Figure 2 shows the statistical speed/power family for a logic circuit. The three curves depict

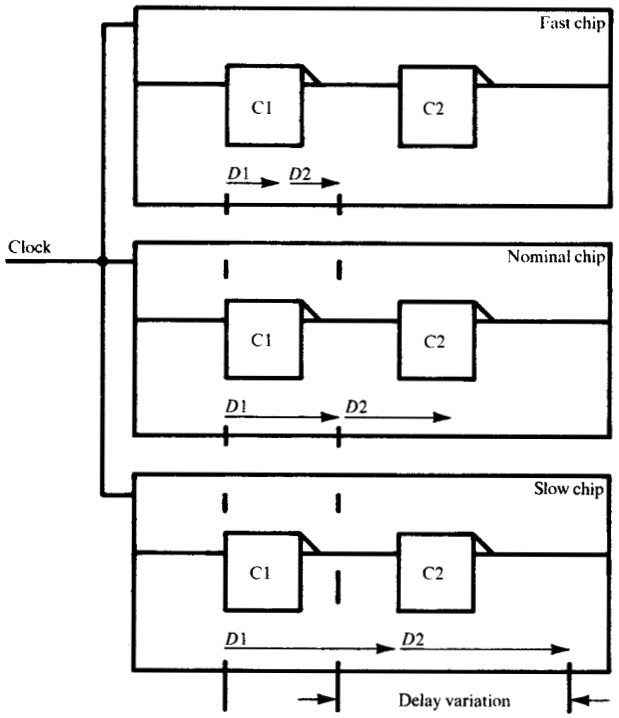

Figure 1 Problem: Delay variation showing a 3-chip 2-circuit path with variation of ±50% from fast chip to slow chip; delay variation equals slow path minus fast path, which in turn equals (nominal + 50%) − (nominal − 50%), which finally yields a delay variation equal to the nominal delay!

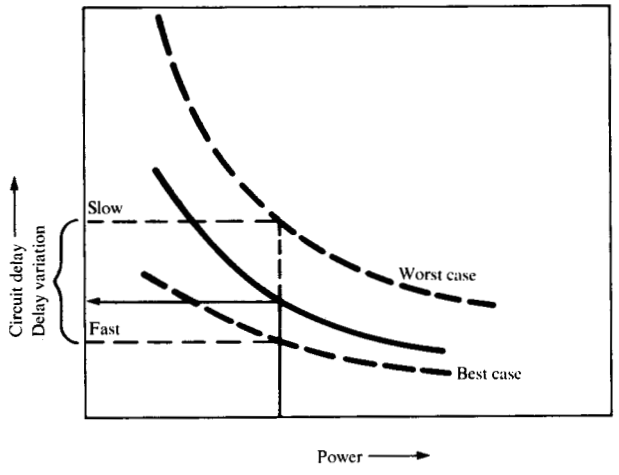

Figure 2 Fixed circuit power causes variable circuit delay.

the circuit delay *versus* power characteristics expected for a logic circuit design over its manufacturing lifetime. Also depicted is the current design practice of selecting a power operating point for the logic circuit and accepting the resulting delay. As perturbations occur in the manufacturing process and system environment, the delay will vary. The logic/system designer must contend

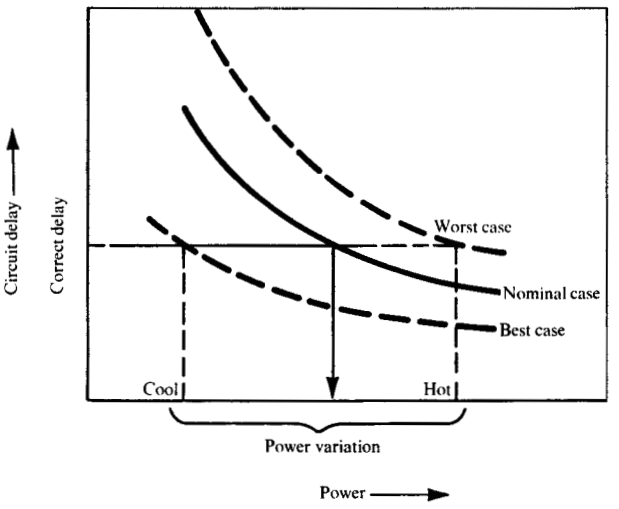

Figure 3 Adjustable circuit power produces fixed circuit delay.

with this type of relationship. Because the system is designed to attain a specific performance, not a specific power dissipation, we contend that emphasis should be changed from selecting a power operating point to compressing the circuit delay variations. Figure 3 shows the key to delay regulation, the compression of delay to the desired value with the resulting power dissipation variation.

In the application of delay regulation to obtain the same circuit delay from chip to chip described, special circuitry is placed on each chip to measure its performance, to compare the performance to an off-chip system reference signal, and to adjust the power in the on-chip circuits to achieve the performance dictated by the system reference. The reference signal goes to all chips in the system; therefore, all chips will have essentially the same performance. The on-chip circuit delay tolerance is not reduced by this approach, but the chip-to-chip variation is reduced.

The paper will describe delay regulation, its theory of operation (including the phase-locked loop), the results of its proper application, new testing capabilities, system usages, and applications to different types of circuits.

Circuit implementation of delay regulation

Figure 4 depicts an example of delay regulation. The delay regulator consists of a phase comparator, a filter, and a voltage-controlled oscillator (VCO) circuit. The phase comparator circuitry compares the off-chip reference clock signal to the VCO signal. The outputs U and D

create a signal with a pulsewidth directly proportional to the phase difference of the input clock and VCO signals. This pulsewidth-sensitive signal has the same frequency as the input clock signal.

The signals U and D are fed into the filter, which removes this carrier input clock frequency from the signal. The V_{CS} signal controls the power in the logic gates on the chip. In this example, the V_{CS} controls the current source of the logic gate. Increasing or decreasing V_{CS} correspondingly increases or decreases the power in the gates.

The VCO produces a frequency which is proportional to the input V_{CS} signal. The VCO circuit is composed of the same type of logic gates as are on the remaining part of the chip, connected in a loop so as to oscillate. Thus, as the V_{CS} signal affects the delay of the logic gate, it also changes the frequency of the VCO. This arrangement of the phase comparator, the filter, and the VCO circuits creates a phase-locked loop.

By this phase-locked loop technique, the VCO will lock onto the input clock reference signal. Lock is a term used to indicate that the native frequency is essentially the same as the reference clock frequency. This phase-locked loop action will reject process, temperature, and power supply changes within the ability of the VCO to lock onto the reference clock signal. Once the VCO has locked, the power to the remaining logic gates on the chip is such that the gate delay is controlled by the input reference clock signal. The signal, which goes to all chips now at the system level, controls the gate delay on each chip. This occurs regardless of the power dissipated by the logic gate, the temperature of the chip, or the lot-to-lot process changes that occur during the manufacturing of the chip. Note that the circuit-to-circuit delay tolerance on-chip is not improved, just chip-to-chip delay variation.

Note also that the phase comparator and the filter circuitry need not be on the same chip. The circuitry required on the chip is the VCO, which senses the speed or gate delay existing on the chip.

Delay regulation—theory

The delay regulation concept is based on a feedback circuit in which the output (VCO frequency) is compared to the input (reference clock signal). A more complete treatment of phase-locked loops is given in [4]. The basic circuit operation is shown in Fig. 5(a). The basic equation describing its operation is as follows:

$$\frac{\phi_O}{\phi_I} = \frac{H(s)}{1 + H(s)} .$$

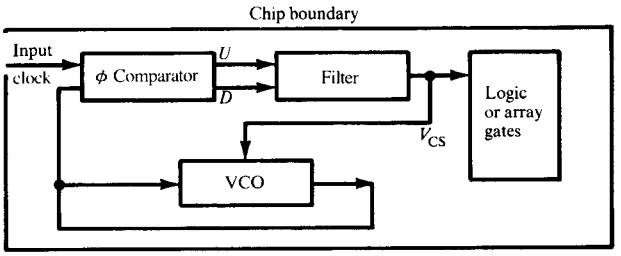

Figure 4 Concept of delay regulation. Line V_{CS} controls power within circuits.

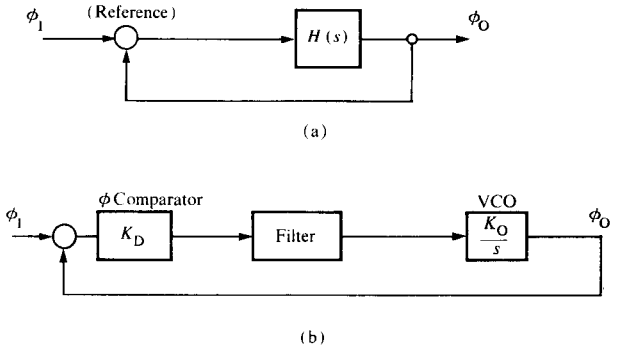

Figure 5 Delay regulation block diagram and equations: (a) Overall transfer function; (b) detailed block diagram.

For the delay regulation application, the block $H(s)$ is composed of the phase comparator, filter, and VCO circuits [see Fig. 5(b)]. The equation for the transfer function then becomes

$$\left[H(s) = K_D F(s) \frac{K_D}{s} \right],$$

$$\frac{\phi_O(s)}{\phi_I(s)} = \frac{H(s)}{1 + H(s)} = \frac{K_D F(s) \frac{K_O}{s}}{1 + K_D F(s) \frac{K_O}{s}} ,$$

where

K_D is the gain of the phase detector $\left(\frac{V}{\text{radians}} \right)$,

$F(s)$ is the transfer characteristic of the filter $\left(\frac{V}{V} \right)$,

and K_O is the gain of the VCO $\left(\frac{\text{radians}}{V \times s} \right)$.

The worst-case values of K_D, K_O, and $F(s)$ (obtained using ASTAP [5] statistical analysis) were used to ensure loop stability in the above equation.

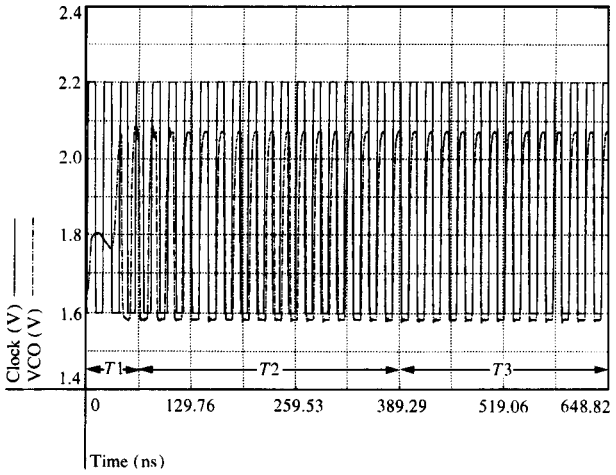

Figure 6 Reference clock signal and VCO signal *versus* time.

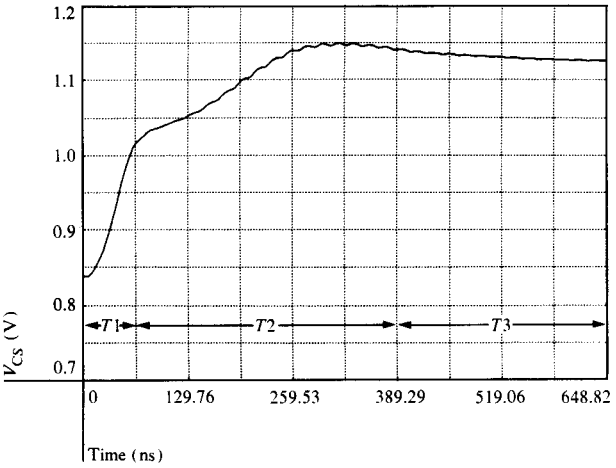

Figure 7 Current source voltage (V_{CS}) *versus* time.

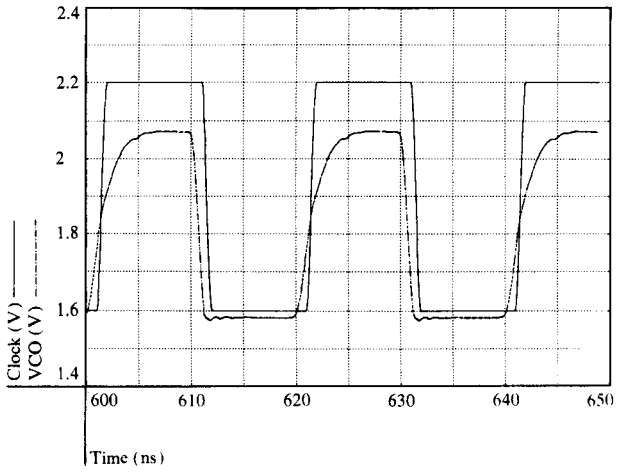

Figure 8 Reference clock signal and VCO signal *versus* time.

The delay regulation concept was modeled using circuits intended for on-chip use. Each circuit used chip device models which included statistical manufacturing and environmental tolerances. The concept was simulated by applying an idealized reference clock signal to the modeled delay regulator circuit and permitting that circuit to lock on the reference clock signal. Figure 6 shows both the idealized reference clock signal and the VCO signal in the delay regulator as a function of time. The plot is divided into three time periods. Period 1 ($T1$) consists of the initial start-up sequence. Where time < 0, there is no reference clock signal input to the delay regulation circuit, so the VCO circuit is powered down. At time $= 0$, the reference clock signal is applied and appears as a step input to the delay regulation circuit. Since the circuit is turned off, there is a delay before the VCO circuit is powered up.

During period 2 ($T2$), the VCO is powered up and begins locking onto the reference clock signal. The VCO initially overshoots but eventually settles into the intended locking position. This occurs in time period 3 ($T3$). Figure 7 is a plot of the current source voltage (V_{CS}) as a function of time. V_{CS} controls the power in the VCO circuit and logic gates on the chip. As V_{CS} increases, the power and speed (frequency) within the VCO circuit and logic gates increase. Figure 8 is a plot of the reference clock signal and VCO signal as a function of time during time period 3, showing the VCO signal locked to the reference clock signal.

This simulation used nominal characteristics for the devices in the circuits. The simulation was repeated using the worst-case statistical device characteristics in the same circuit models and applying the same reference clock signal. As in the nominal characteristic simulation, the delay regulation circuit adjusted the power within the VCO circuit to obtain lock. The remaining logic on the chip would have its power adjusted to this level, resulting in the same gate delay on a worst-case characteristic chip as on a nominal chip.

Results of delay regulation

Figure 9 shows a solution to the chip-to-chip delay variations previously mentioned (Fig. 1). The desired delay is defined as the speed of an externally supplied reference clock frequency, which may or may not be that of the system clock. This reference clock drives the different chips, which in turn regulate themselves to the desired delay. Note that the delays are equal and are locked with respect to the reference frequency.

Now, the system/logic designer can employ delay equations that are precise *and* accurate. The statistical delay

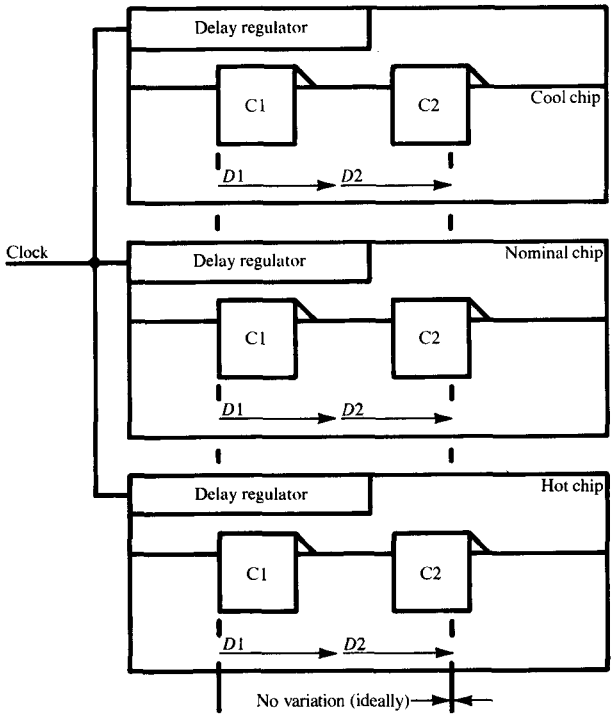

Figure 9 Solution: Applying delay regulation to a 3-chip 2-circuit path resulting in "no" variation. All chips have the "nominal" delay.

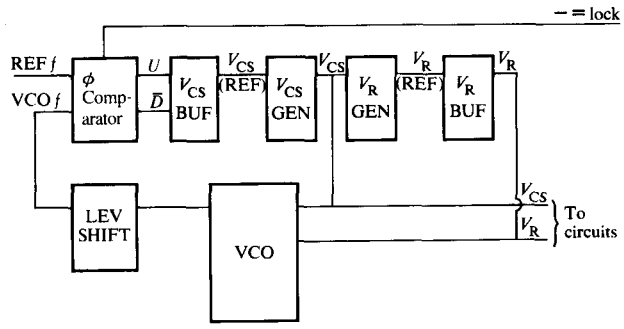

Figure 10 Implementation of delay regulation.

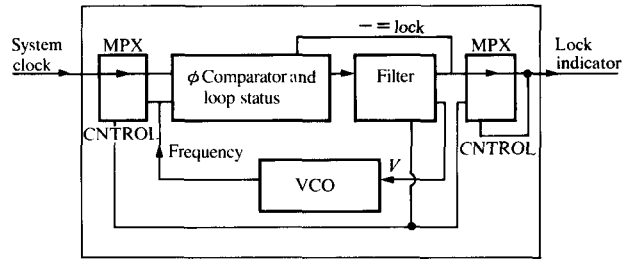

Figure 11 ac assurance using the delay regulator. In normal operation, the VCO is delay-regulated.

adder for the critical delay path can be eliminated. By use of the delay regulation concept, the following novel testing assurance techniques are made possible. In Figure 10, the delay regulator is shown in its use configuration and, although one can "dc" functionally test the chip, ac testing will not be performed. Figure 11 shows this loop with particular attention given to the ϕ comparator and loop status. During normal operations, and during final dc functional test, the system clock is applied to the chip and the lock indicator presents a negative level if the loop achieves lock or a positive level if it fails. Now the final test procedure can vary the power supplies and determine whether the product fails to maintain lock. Lock ensures precise *and* accurate gate delay.

The system designer will use the lock indicator as a real-time indication of the system (subsystem) product speed. This permits real-time verifications of the performance of the machine by the maintenance processor. Figure 12 shows detailed logic of the ϕ comparator and the loop status (see note [6]). Note that in addition to the – = lock output, other indicators are available (the + = fast, + = slow lines). This enables certain diagnostics such as process monitors to be performed. In a practical embodiment, the overhead has been shown to be less than 100 circuits and two I/O pads; this overhead on a 10K circuit chip is very small.

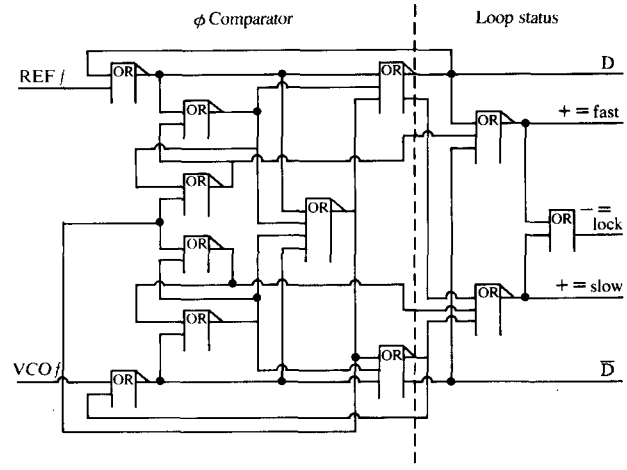

Figure 12 ϕ comparator and loop status logic.

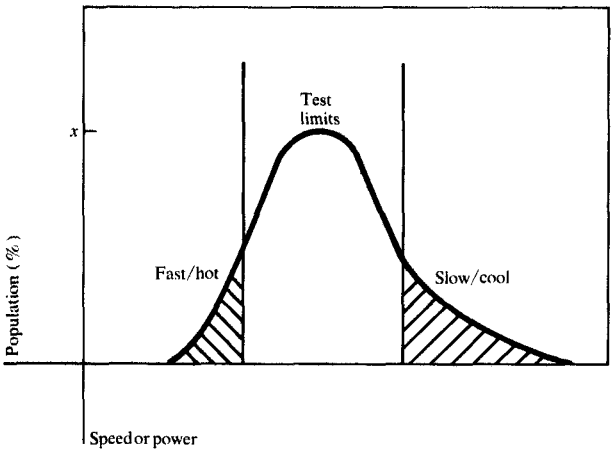

Figure 13 Speed/power product population distribution without delay regulation.

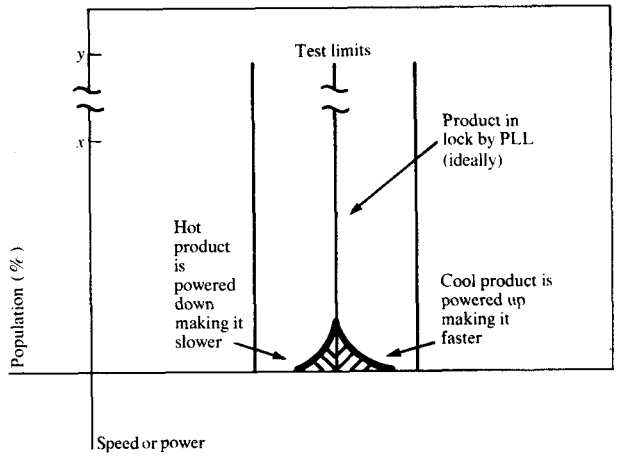

Figure 14 Speed/power product population distribution with delay regulation. Note that level y indicates a much greater relative population than does level x shown here and in Fig. 13.

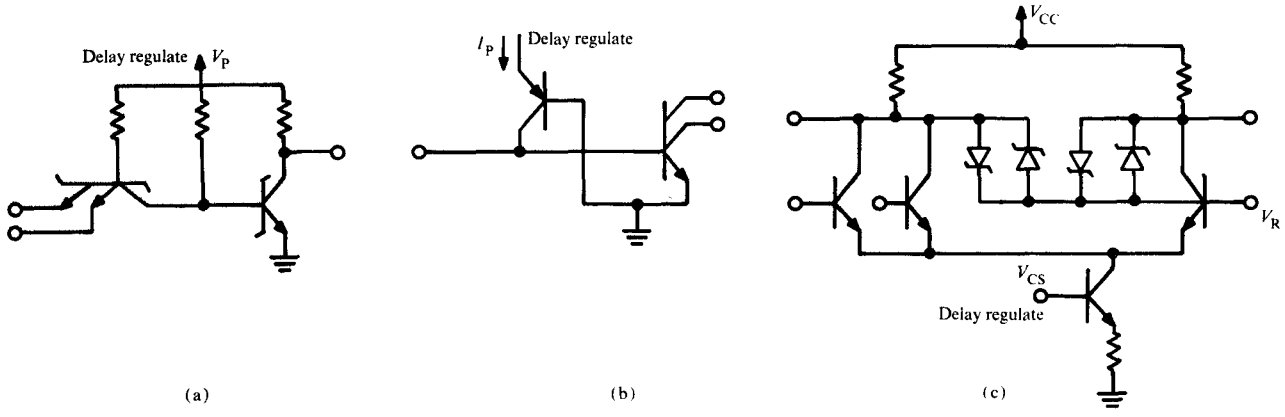

Figure 15 Examples of delay-regulatable circuits: (a) T^2L; (b) I^2L; (c) ECL.

Product implications

Figure 13 shows a typical distribution giving the tradeoff of power *versus* performance. In order to obtain an improved yield (product made of VLSI circuits with a particular performance), power is added to the slow product and removed from the fast product so that all product converges on the performance preselected as the optimum yield point (see Fig. 14). The nature of a phase-locked loop is such that it forces the power of the product to be whatever is required to achieve lock.

Figure 14 shows the resulting representative product population after delay regulation has occurred. A much higher percentage of product population is at the desired point. Although a small percentage of noncapture is shown here, total population lock is possible. If a particular product performance is desired, the reference frequency can be varied to shift the lock point. However, less product would be captured.

Applications

Figure 15 demonstrates simple examples of delay regulation applied to the major types of bipolar circuits: T^2L (Transistor-Transistor Logic) by varying the positive supply (V_p), I^2L (Integrated Injection Logic) by varying the injection current (I_p), ECL (Emitter Coupled Logic) by varying the current switch current, and in general any type of circuit which has a speed/power relationship.

Summary

The performance and power of semiconductor products are influenced by parameters such as processing, packaging, power supplies, temperature, and aging. Delay regulation provides an *in situ* product adjustment of power *versus* performance and thereby reduces these influences.

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References and notes

1. *MECL High Speed Integrated Circuits*, Motorola Series B. Motorola Semiconductor Products, Inc., Phoenix, AZ, 1978, pp. 1-14.
2. A. H. Dansky, "Bipolar Circuit Design for a 5000-Circuit VLSI Gate Array," *IBM J. Res. Develop.* **25**, 116-125 (1981, this issue).
3. Portions of this paper appeared in the article by E. Berndlmaier, J. Dorler, J. Mosley, and S. Weitzel entitled "Delay Regulation—A Performance Concept," which appeared in the *Proceedings of the IEEE International Conference on Circuits and Computers ICCC80*, Port Chester, NY, October 1-3, 1980, p. 701.
4. Floyd M. Gardner, *Phaselock Techniques*, John Wiley & Sons, Inc., New York, 1966.
5. *Advanced Statistical Analysis Program (ASTAP), Program Reference Manual*, Pub. No. SH20-1118-0, IBM Corporation, Data Processing Division, White Plains, NY 10604.
6. Motorola Phase Frequency Detector P/N MC12040. The theory of operation is described in Motorola data sheets MC 4344/4044.

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