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A 1024-Byte ECL Random Access Memory Using a Complementary Transistor Switch (CTS) Cell

This paper presents the design of a 1K-byte random access memory using a cross-coupled complementary transistor switch (CTS) cell. The memory operates with a 4.25-V power supply and achieves a 15-ns access time with a power dissipation of 1.8 W. This paper also demonstrates the advantages of using the CTS cell to achieve high circuit density and good performance of memory arrays. Array attributes, cell selection criteria, and cell operation (both ideal and in situ) as well as design considerations are covered. Hardware performance is also briefly summarized.

Introduction

With the emergence of VLSI through the advantages of integrated circuit technology, denser random access memory (RAM) array chips (>3072 bits) with high-speed access times (≤50 ns) are becoming a regular requirement in computing machine designs. As we strive for higher and higher computing speeds, measured in millions of instructions per second (MIPS), we must decrease the time required to complete each instruction. By increasing array densities, we reduce the numbers of array chips required to perform a specific function and therefore the overall function delay. This paper describes a RAM designed to meet these requirements. Possible applications for such a RAM are control stores, cache memories, general-purpose registers, and table functions.

The array chip designed and fabricated is a 10 240-bit emitter-coupled logic (ECL) RAM. It is externally organized as 1024 cells × 10, of which one of the 10 outputs is allowed for redundancy (to enhance manufacturing yields). Internally it is organized as 128 cells × 80 cells. There is an 11 × 11 I/O pad matrix provided for communication with the chip. Of the total 121 pads, 69 are functional (24 for power supplies and 45 for signals); the remaining 51 pads, while not electrically functional on this design, do provide thermal enhancement via thermal conduction.

The designed array has a typical access time of 15 ns and a nominal power dissipation of 1.8 W, and is contained within 28 square millimeters of silicon area. Different personalizations of a monolithic masterslice make possible compatibility with two separate and distinct power supply systems, one having ground as the most positive supply and −4.25 V as the most negative, the other having +5.0 V as the most positive supply and ground as the most negative. The speed, power dissipation, and size of this array chip were achieved through the use of an epitaxial layer 2.0 μm in thickness, recessed oxide isolation (ROI), three separate levels of metallization, and 2.5-μm optical photolithographic images [1, 2]. However, in addition to these process specifications, the key to the ability to achieve the array attributes was the use of the complementary transistor switch (CTS), Fig. 1, as the memory cell element. This cell achieves extremely low cell area and standby power while giving up neither speed nor stability. The memory

Table 1 Array chip attributes.

	Typical
Access time	15 ns
Cycle time	15 ns
Power dissipation	1.8 W
Array power dissipation	46 mW
Chip size	5.3 × 5.3 mm
Bits per chip	10 240
Bits per mm^2	404
mW per bit	0.17
PJ per bit	2.6

element is comparable to a static FET memory element in area usage; however, it possesses the speed associated with bipolar devices. (Another array with similar characteristics was designed independently and was uncovered during research for this paper [3].)

This paper focuses on the embodiment of the CTS cell in a memory array to achieve the performance and density objectives. It presents the array attributes (Table 1) and discusses the cell selection criteria and the cell and array operations. Some of the chief concerns in the design of the array are the dc cell characteristics, including the effects of the negative resistance region, transient stability, and the maintenance of minimum write cycle times. The design considerations which treat these concerns are presented. Hardware performance is briefly summarized.

The CTS cell

- *Cell selection*

The emphasis of this design was primarily on density, speed, and power dissipation for an output width of 1 byte (9 bits). Candidates for the memory element included the "modified" Harper cell [4] (modified only by the inclusion of the SBD clamps), Fig. 2, the Schottky-gated pnp load (SGPL) [5–7], Fig. 3, and the CTS cell.

During the comparison of these choices, the design ground rules were kept constant along with the manufacturing process. The comparison proved the CTS cell to be superior in both density and power dissipation. In density the CTS cell was 19% and 46% greater than the SGPL and Harper cells, respectively. In standby power the CTS cell dissipated an amount approximately equal to the SGPL cell and an order of magnitude less than the Harper cell. The speed relationship also favored the CTS cell.

It should be noted that there are no resistors contained in the cell (refer to Fig. 1), which is entirely made up of active devices. It is for this reason that a cell with both small area (1600 μm^2) and low standby current (5 μA) is

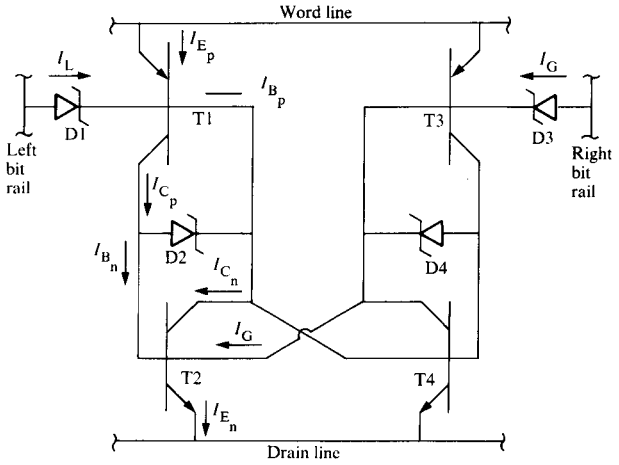

Figure 1 Complementary transistor switch cell.

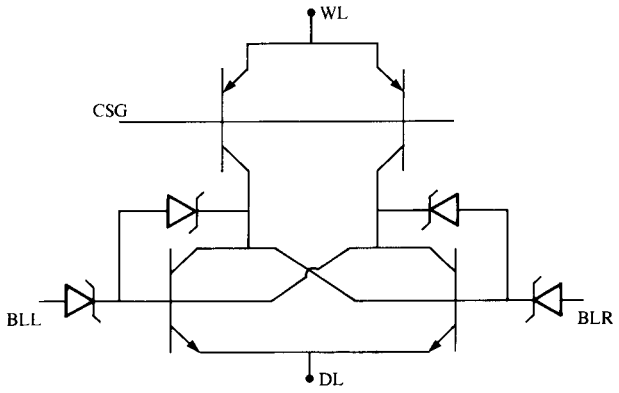

Figure 2 Harper cell schematic.

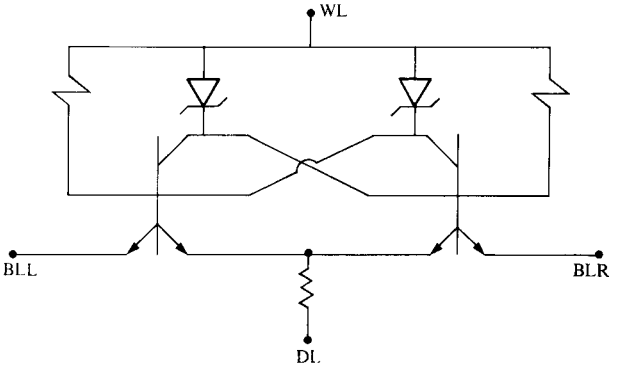

Figure 3 SGPL cell schematic.

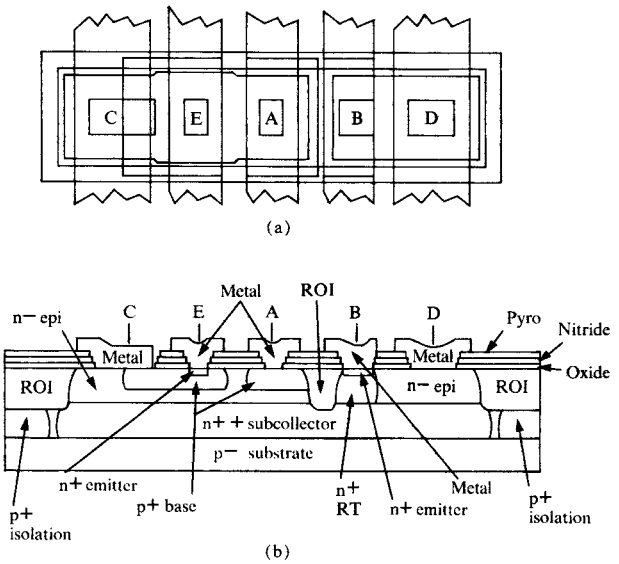

Figure 4 SCR physical layout: (a) Layout with metal; (b) cross section (not to scale). Pyro is pyrolytic oxide. ROI is recessed oxide isolation. RT is reach-through.

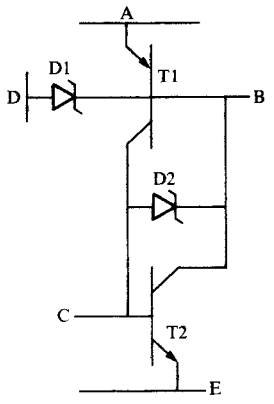

Figure 5 SCR schematic.

achievable. With reference to Fig. 4, it should be noted that one-half of a CTS cell is totally integrated into one device structure, with isolation required only between device structures. This level of integration is not attainable with the other cells considered. It was primarily for these reasons that the CTS cell was chosen as the memory element in this 1K-byte RAM.

• *CTS cell description*

The bit cell (Fig. 1) consists of two cross-coupled silicon-controlled rectifier (SCR) pnpn devices. Each SCR (Fig. 5) contains a vertical npn transistor (T2), a lateral pnp transistor (T1), a read/write Schottky Barrier Diode (SBD) (D1), and an anti-saturation clamp SBD (D2).

The vertical silicon representation is shown in Fig. 4. The pnp emitter (contact "A") is p+ acceptor-type material. Contact "B" is a combination pnp base, npn collector, read/write SBD cathode, and anti-saturation SBD cathode contact. This contact is made through emitter n+ and n+ reach-through diffusions. The actual lateral pnp base region is the n− epi between base diffusions.

A second combinational contact is contact "C." The portion of the metal that contacts the n− epi defines the SBD anti-saturation clamp anode; the remaining portion contacts a p+ base region which serves as the pnp collector and the npn base. Contact "D" is the read/write SBD anode contact. The npn emitter diffusion is defined by contact "E."

The cell aspect ratio (x dimension divided by y dimension) is important to ensure compatibility with support circuits to keep the array size as square as possible. The overall silicon component area occupies 92% of the active chip.

• *Cell operation*

The three modes of operation of the cell are standby, read, and write. This section provides the mathematical description of cell stability during standby, one-half select, and full selection operation. A description of cell operation in standby, read (select), and write modes is also given.

Figure 1 identifies the terms used in the following expressions. These conditions must be maintained to guarantee stable cell operation.

• *General stability*

$$I_{C_p} + I_G \geq (I_L + I_{B_p})\frac{1}{\beta_n},$$

$$\alpha_p I_{E_p} + I_G \geq \frac{I_L + I_{E_p}(1-\alpha_p)}{\beta_n},$$

$$\alpha_p I_{E_p} + I_G \geq \frac{[I_L + I_{E_p}(1-\alpha_p)](1-\alpha_n)}{\alpha_n}.$$

Standby $(I_L, I_G \equiv 0)$.

$$\alpha_p I_{E_p} \geq \frac{I_{E_p}(1-\alpha_p)(1-\alpha_n)}{\alpha_n},$$

$$\alpha_p I_{E_p} \geq \frac{I_{E_p} - I_{E_p}\alpha_p)(1-\alpha_n)}{\alpha_n},$$

$\alpha_n + \alpha_p \geq 1$ (Standby condition for cell stability).

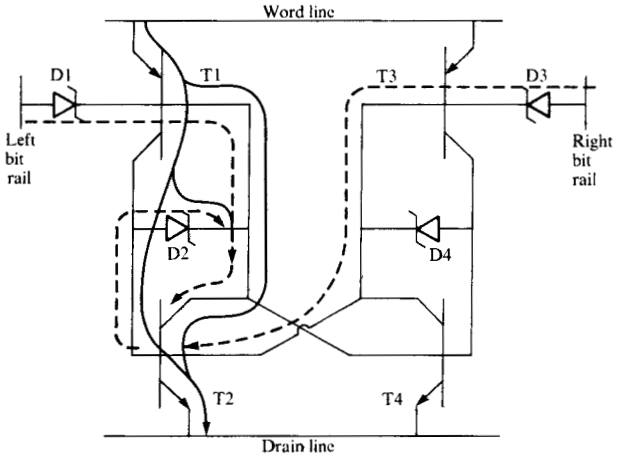

Figure 6 Complementary transistor switch cell.

Half select $(I_G \equiv 0, I_L \equiv 0)$.

$\alpha_n + \alpha_p \geq 1$ (Half select stability condition).

Full select $(I_{E_p} \equiv 0)$.

$$I_G \geq \frac{I_L(1 - \alpha_n)}{\alpha_n},$$

$I_G \geq \beta_n I_L$ (Full select condition for stability).

Standby (Fig. 6, solid lines for current)
During standby, both pnp transistors are in the conduction mode while both bit rail Schottky diodes (D1 and D3) are non-conducting. The cell in this condition is stable at very low currents provided that the sum of the npn and pnp transistor alphas exceeds unity. Excess npn base current is directed through the npn base-collector anti-saturation SBD (D2), thus establishing an appropriate cell base-base differential voltage (≈0.5 V). A standby current of 5 μA/cell was chosen as the best compromise between power and performance.

READ (Fig. 6, dashed lines for current flow)
During a read operation, the cell pnp transistors are turned off. The npn current is supplied through the bit rail SBDs only. In this fashion the cell pnp transistors are restricted to very low currents, thereby limiting the amount of pnp capacitance which must be dealt with during a write operation.

WRITE (Fig. 7, solid line present state, dashed line next state)
During a write operation the desired bit rail voltage is driven above the previously conducting npn transistor base voltage by approximately 0.5 V. This action is sufficient to create a regenerative process within the npn

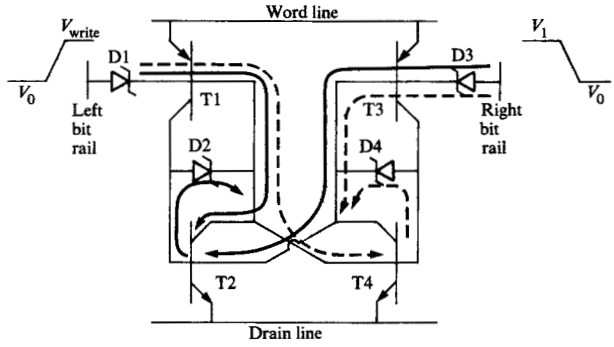

Figure 7 Complementary transistor switch cell during write.

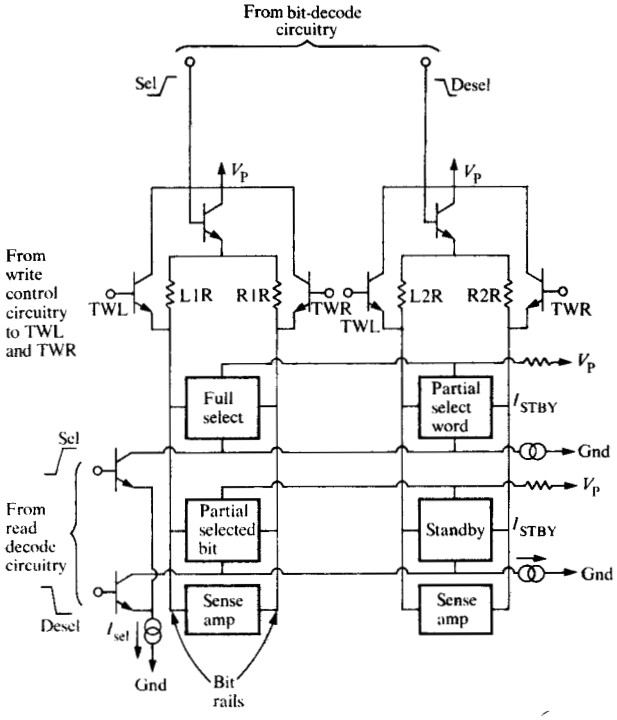

Figure 8 CTS array read/write operation.

transistors and this flips the cell. The key to this write operation is the absence of active SCR action. With the cell pnp transistors off during selection/write, coupled with a "voltage mode" write, the array write cycle of 20 ns is achieved.

Array operation

- *Select/read (Fig. 8)*

Through word and bit decoding, selection of 10 fully selected and 70 partially selected cells is achieved. Larger

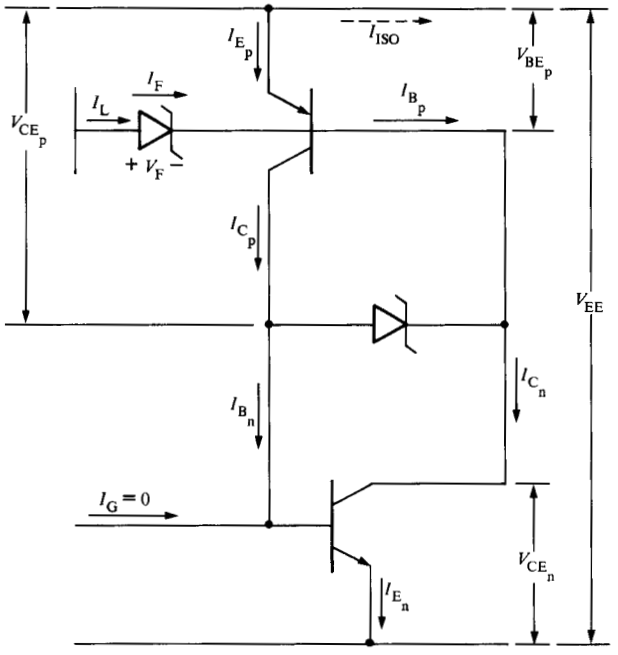

Figure 9 Half-CTS cell reference schematic for Figs. 10–14. For the characteristics in Figs. 12–14 the emitter of the npn transistor is open.

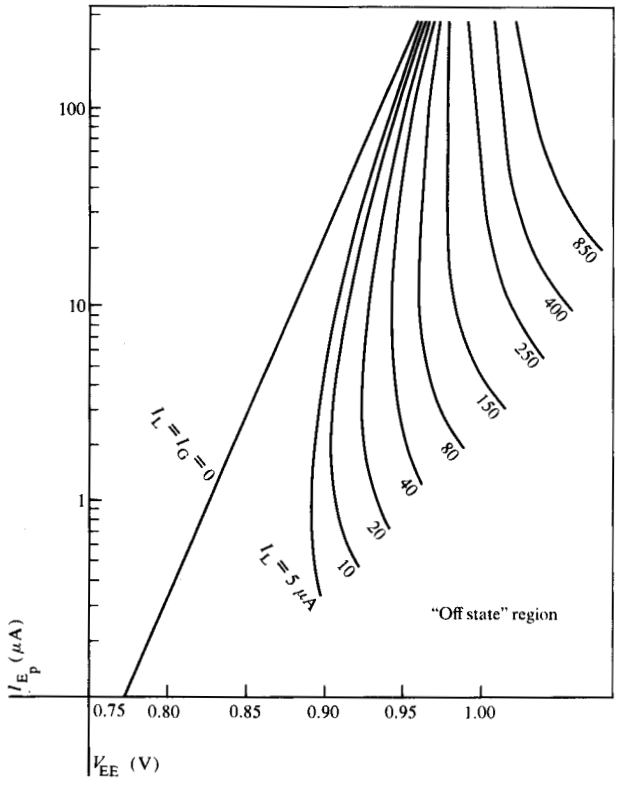

Figure 10 Half-cell (half-select) SCR characteristics. $I_G = 0$. The curve $I_L = I_G = 0$ is the standby condition.

select currents (≈1 mA) are supplied only to the selected cells. The remaining partially selected cells are powered to 30 μA while the unselected cells are powered to 5 μA. This greatly reduces total chip power. The npn collector and base components of the selected cell current are supplied through the bit rail resistors R1R and L1R. The voltage developed across these bit rail resistors is differentially sensed and drives an output stage. The speed of the word selection mechanism is proportional to the amount of select current supplied to the selected word line. A typical access time of 15 ns has been demonstrated on product with 12 mA of select current. Referring to the selected word line, it should be emphasized that the half-selected cells on that word line are powered up, thereby increasing their differential voltage and increasing immunity to word line disturbs. The cells on all remaining word lines are in a standby mode conducting 5 μA per cell.

Write (Fig. 8)

The write operation is performed by voltage mode emitter-follower action. As described earlier, the desired *selected* bit rail is driven approximately 500 mV above the present "1" level in the cell. This is accomplished through the data-in circuitry and the write control circuitry in conjunction with write transistors TWL and TWR. This voltage transition is sufficient to flip the state of the cell. Regenerative feedback and dc stability of the SCR hold the newly written state until the next write operation once again changes it.

Design considerations

Several concerns were addressed in using the CTS cell and designing the support circuitry. They may be categorized as follows:

1. dc cell characteristics and effects of inherent negative resistance on current sharing of (parallel) cells on a common word line.
2. Cell stability during transient word or bit switch.
3. Circuit schemes for maintaining minimum write cycle times.

Cell characteristics

The device characteristics to be described were measured on an actual product wafer test-site at 21°C and have been verified by modeling simulations (see Fig. 9, reference schematic of half the CTS cell). Figure 10 displays the voltage across the cell V_{EE} as a function of the pnp supply current for various load currents I_L with gate current I_G set to zero.

Not all of the pnp current flows out of the bottom of the cell. Depending upon the subcollector-isolation and sub-

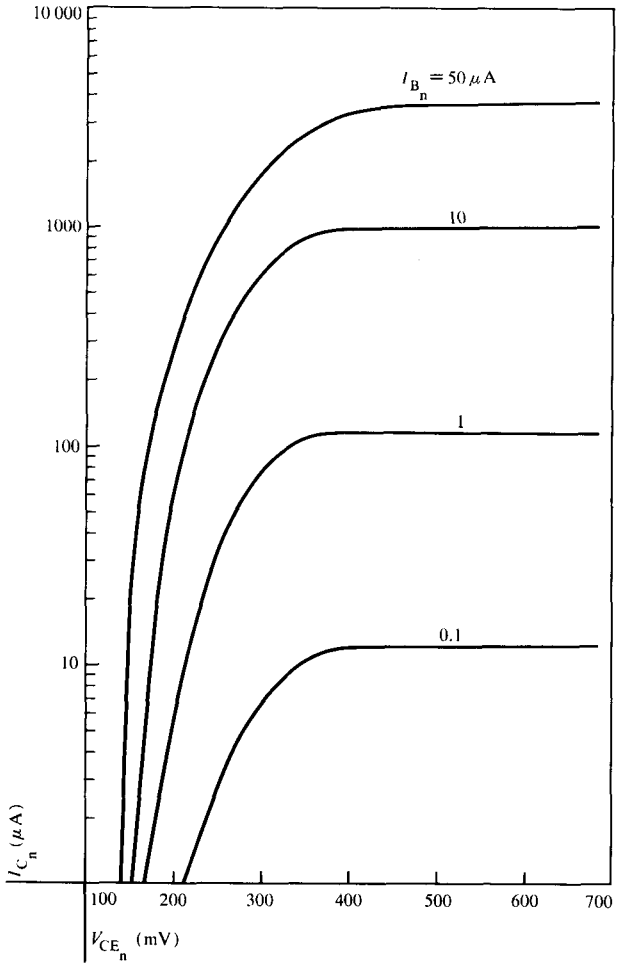

Figure 11 Half-cell npn beta curves.

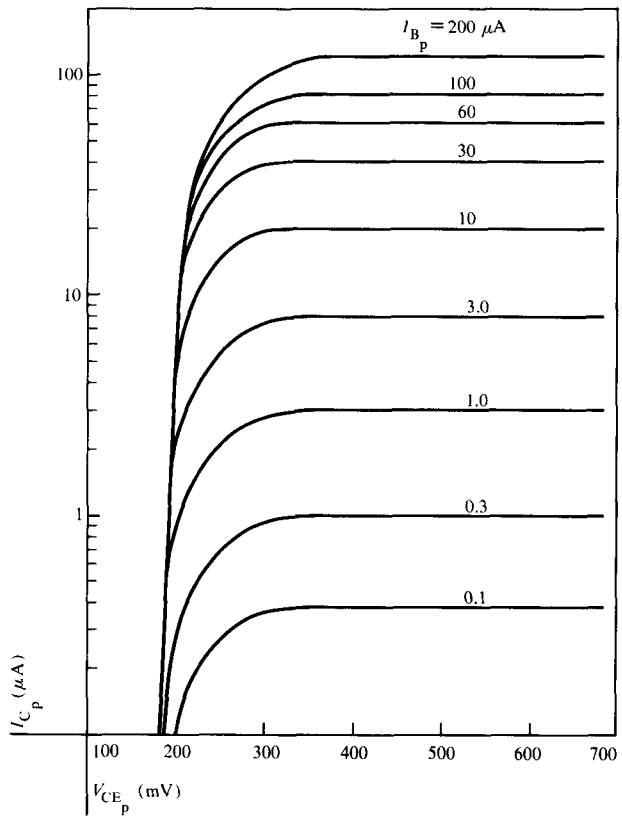

Figure 12 Half-cell pnp beta curves.

collector-ROI spacing, a portion (≈30%) of the total pnp current flows into isolation. The curve at the far left describes the pure SCR characteristics used in the standby mode. The positive slope characteristics of this curve are easily designable. Cell stability can be maintained at very low currents providing leakage currents are negligible.

The remaining curves shown in Fig. 10 display regions of zero or negative resistance slopes which should be avoided. Design in these regions is difficult due to the current-robbing concerns of the parallel cells and a multiplicity of design solutions which can exist.

The negative resistance and the "off-state" regions as shown in Fig. 10 can be explained with the help of the V_{CE_n} (sat) characteristics shown in Fig. 11. At fixed load currents, as the base drive is increased V_{CE_n} decreases. If this decrease is larger than the corresponding increase in pnp V_{BE}, a net V_{EE} reduction results ($V_{EE} = V_{CE_n} + V_{BE_p}$). Therefore, the negative resistance region of Fig. 10 corresponds to the saturation edge of the V_{CE}/I_L characteristic. The "off" state of Fig. 10 describes the region where insufficient base drive is available to maintain the required load current in saturation.

Figure 12 shows the beta characteristics of the lateral pnp device (2.5-μm base width). Betas are typically 4 at 0.4 μA, 3 at 3 μA, 2 at 20 μA, and 0.7 at 100 μA. The lateral pnp V_{BE} *versus* I_E is shown in Fig. 13. To complete the characterization, the Schottky forward characteristics are shown in Fig. 14. "Minority" carrier current into isolation occurs at current densities (J) above 1 kA/cm^2.

As mentioned earlier, the basis of the dc design is to eliminate operation in the zero- or negative-resistance portion of the characteristic curves. Therefore, bit rail resistors should supply the npn base and collector components for the selected cells. A bit line differential (≈0.4 V) is established as adequate for read sensing, and also as sufficient to satisfy the V_{CE_n} (sat) characteristics without requiring additional pnp gate drive. Thus, selected cells effectively define the lower (drain) voltage of the cell. The remaining "half" selected cells are biased such that their bit rail Schottky diodes are nonconducting ($I_L = I_G = 0$). These cells are maintained stable with pnp

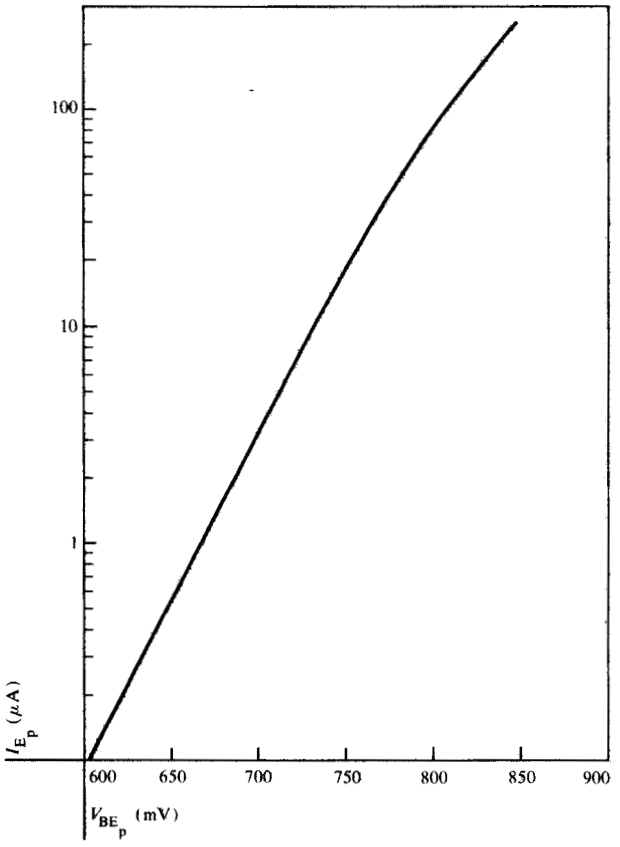

Figure 13 Half-cell pnp V_{BE} curves.

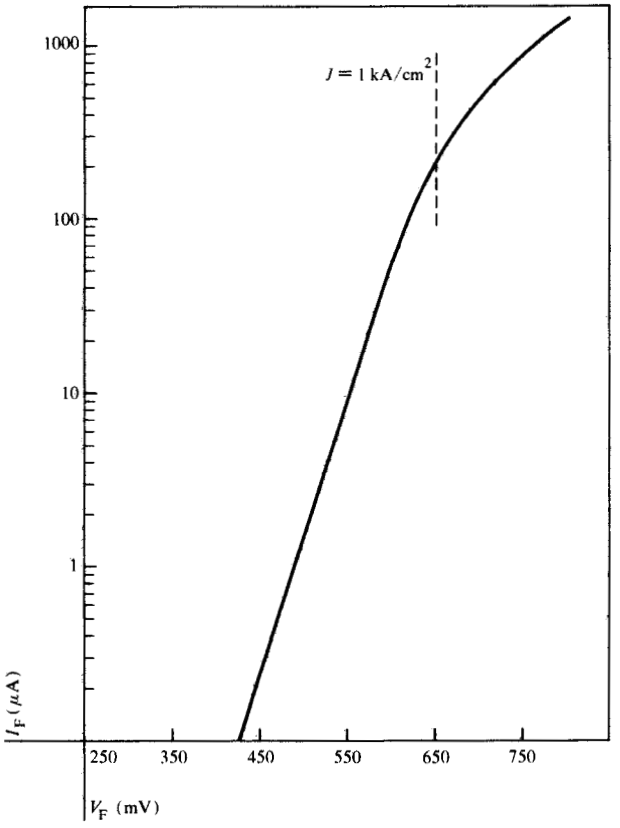

Figure 14 Half-cell bit SBD curves.

conduction and SCR operation as described in Fig. 10. Thus these half-selected cells define the voltage at the top of the cells (word line).

Modeling simulations have shown that improper use of these design curves, together with inaccurate estimates of metallization drops, can and most likely will result in difficult-to-detect array operating conditions. These conditions could result in loss of data after several microseconds or inoperability at very slow cycle times.

Transient cell stability

A decrease in cell npn base-base voltage during word de-select and bit select transitions has been observed. Figure 15 examines the cell during word de-select. A row (word) is de-selected by switching off its high-value-select current and simultaneously pulling up the top of the cells through a low-impedance emitter-follower driver. The internal cell down level immediately follows the upper word line due to the high capacitive coupling of the "on" pnp device. The "1" side of the cell likewise rises once its pnp device starts conducting. The minimum cell differential is reduced to 100 mV during the transient, and eventually recovers to a steady-state 500 mV.

A loss in base-base differential is also incurred during the positive bit select transient as shown in Fig. 16. The bit rail Schottky connected to the more negative cell "0" level conducts before the "gate current" to be supplied by the opposite bit rail Schottky (with its cathode at the cell "1" level) can conduct. Therefore the low-value pnp current must be of sufficient drive to maintain the cell down level until eventual re-enforcement from the bit rail Schottky takes place. Cell minimum differential is reduced to 300 mV during this transient.

Write stability

The write operation is depicted in Fig. 17. In order to maintain a minimum write cycle time during a word address change, a de-selected word line is quickly pulled positive by a low-impedance driver as described in the previous section. The write is performed by raising the desired bit rail and corresponding cell "0" approximately 0.5 V above the cell "1" level. During this operation a minimum write cycle can only be achieved if the charge

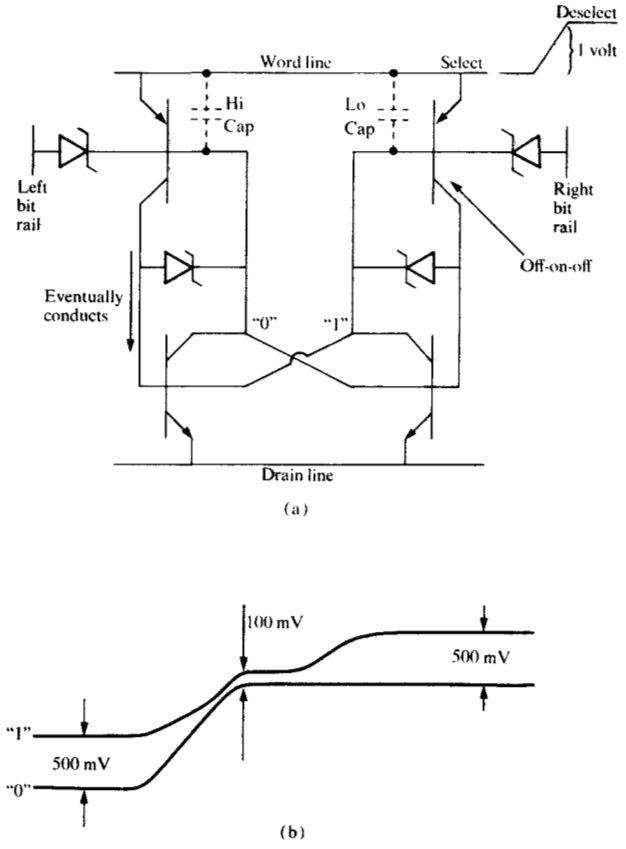

Figure 15 Complementary transistor switch cell: (a) Cell stability during word de-select; (b) Cell base-base voltage.

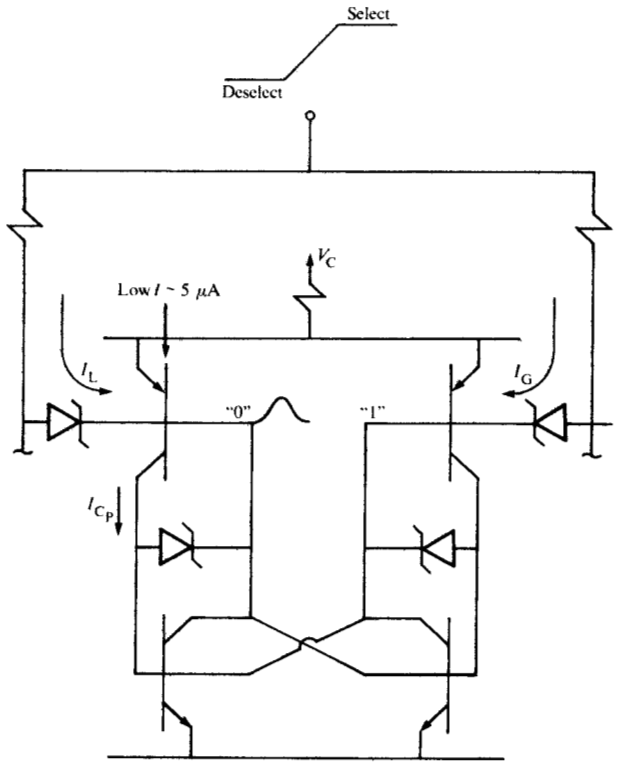

Figure 16 Cell stability during bit select. During the bit select transient the left SBD conducts first, and the low pnp current I_{C_P} must satisfy the load current I_L requirements until reinforced by I_G.

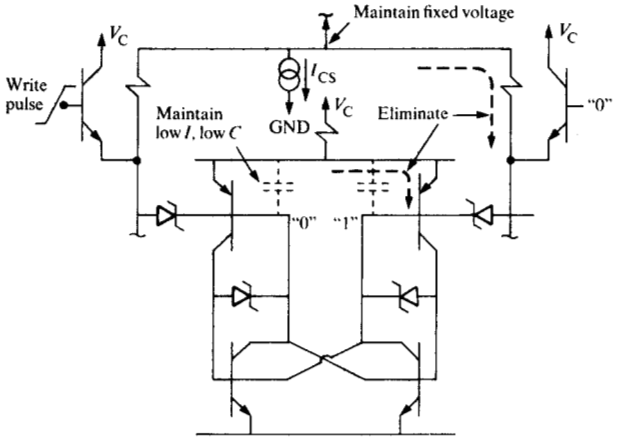

Figure 17 Write operation (reduce charge coupling to cell "1").

coupled to the cell "1" mode is minimum. Coupling is minimized by operating at low pnp currents (therefore low emitter base capacitance). Also, a path for the bit rail resistor current is satisfied by current source (ICS), thereby maintaining a fixed selected bit voltage and preventing a positive voltage pulse from sustaining the cell "1" level.

Summary

This paper describes the authors' experiences in designing a 1K-byte RAM using the complementary transistor switch cell (CTS). The array attributes (typical access 15 ns at 1.8 W), cell selection process, cell operation, and design considerations have been addressed. Through the use of the CTS cell such attributes as 2.6 pJ/bit and 365 bits/mm^2 were made possible [based upon 9216 bits and 5.03 mm^2 of active array area, 404 bits/mm^2 based upon 10 240 bits]. However, it should be emphasized that to achieve the attributes possible with this design, the design considerations in applying this kind of cell which are presented in this paper should be adhered to. This design effort has produced a 1K-byte RAM that is certainly extendible to denser arrays because of the efficiency of the CTS cell in its use of silicon and its relatively low power consumption. As technology advances and the array chip densities in bits per square millimeter increase, cell size and required power become paramount. It is the opinion of the authors that as more dense static bipolar array chips become necessary, a wider use of the CTS cell will emerge.

Acknowledgments

The success of this project is due to the dedication and extraordinary efforts of many people on the design team in Hopewell Junction, NY, which consists of Circuit P. E., Chip/Mod P. E., Manufacturing, Test Engineering, Quality Engineering, and Product Assurance. The authors wish to recognize the efforts of the groups whose work is represented in this paper. Special thanks are given to P. Low, F. Wise, and W. Siegle for their support in making this publication possible. Special mention is also given to E. Rymaszewski and R. M. Esposito, through whose support an actual chip design was realized and produced.

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Received September 9, 1980

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