Preface

Rapid progress in miniaturization and integration has brought the computer and semiconductor industries to the brink of a new era of microelectronics. This is the era of VLSI, Very Large Scale Integration. Its goal is to design and develop a reliable and reproducible high-density fabrication process that can yield semiconductor chips containing a million or more devices.

The successful design and fabrication, at the IBM East Fishkill and the IBM Boeblingen facilities, of a 5000-circuit (45 000 transistors, resistors, and diodes) bipolar, high-performance, experimental microprocessor chip, encompassing a data flow equivalent to that of the IBM System/370 Model 138, coupled with industry-reported successes in fabricating one-micron and submicron device features, make this goal attainable. While no known fundamental physical barrier to achieving this goal has been identified, it is important to recognize that a number of difficult technical problems and tradeoffs do exist. Analyses of these problems and the experience gained from the experimental 5000-circuit microprocessor chip effort referred to earlier indicate a need for close coordination among the various disciplines and functions involved in the production and maintenance of VLSI-based digital computer systems. In particular, the system development methodology must be viewed as the synchronization and close coordination of the system developers, circuit designers, semiconductor physicists, design automation specialists, and manufacturing engineers who fabricate the chips and develop and test the final product.

This issue of the *IBM Journal of Research and Development* contains five papers dealing with different aspects of VLSI. The first paper, "Techniques for Improving Engineering Productivity of VLSI Designs," by Joseph C. Logue *et al.*, describes a two-pass VLSI design approach based on the use of PLA macros and a laser beam for rapid personalization and repairing of design errors. A. H. Dansky's paper, "Bipolar Circuit Design for a 5000-Circuit VLSI Gate Array," describes the technology selection criteria, the design process, the selection of the gate array chip image, and the performance and power dissipation tradeoffs made in the development of the experimental microprocessor chip.

A third paper, "A 1024-Byte ECL Random Access Memory Using a Complementary Transistor Switch (CTS) Cell," by J. A. Dorler *et al.*, demonstrates the advantages of using a cross-coupled complementary transistor switch cell for achieving good density and performance in memory arrays. Another paper, "Delay Regulation—A Circuit Solution to the Power/Performance Tradeoff," by E. Berndlmaier *et al.*, deals with the VLSI problem of the widening statistical tolerances on computed delay values. The new concept is to vary the power in the circuit in order to regulate and achieve the desired circuit delay, narrowed distribution, and improved yield. The authors discuss the analysis, new testing capability, and application of this concept to different circuit types.

In the fifth paper in this group, "A High-Density Bipolar Logic Masterslice for Small Systems," by J. Z. Chen *et al.*, the authors describe a bipolar logic masterslice containing an unusual arrangement of a Schottky Transistor Logic Circuit Cell and a new physical design methodology that permits the personalization of different unique part numbers.

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