Errata

In "A System Solution to the Memory Soft Error Problem" (D. C. Bossen and M. Y. Hsiao, *IBM Journal of Research and Development* **24,** No. 3, May 1980, pp. 390–397), the following changes should be noted:

p. 392 The sentence beginning at the top of Column 2 should be:

"This situation is a predominant case because if the solid error is a chip kill or word-line kill or bit-line kill, . . ."

p. 392 The sentence in the second column beginning "For example, a DEC-TED . . ." and the sentence following it should be replaced by:

"For example, a DEC-TED code requires 15 check bits instead of 8 in the case of 64 data bits. Adding the extra 7 check bits to every address increases the cost proportionately."

p. 395 The sentence beginning "Soft failure rate:" should be:

"Soft failure rate: varies from 0.1 to 1% per 1000 power-on hours per chip."

p. 395 The first sentence of paragraph 3 should be:

"Modeling of strategies which do not completely clean the memory when a UE occurs requires simulation [12]."

p. 396 The last line in Table 2 should be changed to: "0110 1000".