

Electron-Beam Resists for Lift-Off Processing with Potential Application to Josephson Integrated Circuits

Several electron-beam resists suitable for lift-off processing have been investigated with particular attention to the requirements for fabricating Pb-alloy Josephson integrated circuits. The desired resist must perform well with a baking temperature near 70°C, provide a reproducible undercut edge profile with good linewidth control, and adhere to the necessary substrates. Diazo resists as well as the commonly used PMMA and copolymer materials were studied. Initial results suggest that [®]AZ-1350J soaked in chlorobenzene to enhance the undercut profile can satisfy many of these requirements. At present, the amount of undercut obtained is larger than desired, limiting the minimum separation between exposed features to about 1.5 μm .

Introduction

Lift-off processing [1-9] is commonly used for patterning evaporated thin films. In this technique, the film to be patterned is deposited over a resist stencil with an undercut edge profile such as that shown in Fig. 1. The resist is then dissolved, removing the material on top of it. The undercut ensures a clean separation at the pattern edges. Lift-off processes have been described for resists exposed with ultraviolet light [1-7] or with electrons [8, 9].

Lift-off processing has been widely used in patterning Josephson junction logic and memory circuits [3-5] since most of the patterning steps involve evaporated films. Comparatively complex Josephson integrated circuits have been fabricated and shown to provide high switching

speeds with low power dissipation [10, 11]. The fabrication process consists of the evaporation and patterning of a number of thin film layers of superconductors, resistors, and insulators and the use of plasma cleaning and oxidation processes [12, 13]. Patterning has generally been carried out using optical lithography with minimum feature sizes of about 2.5 μm .

As in other technologies, improved lithographic resolution can lead to significant benefits for Josephson circuits. A preliminary examination [14] has shown that scaling present circuits down to a smaller minimum linewidth is expected to reduce logic delays. In addition, circuits of present minimum linewidths should benefit from tighter dimensional control. Narrower spreads in critical parameters such as junction area should improve circuit performance and device yield.

The increased resolution and tighter dimensional control can potentially be provided by electron-beam lithography [15]. Writing directly on wafers with an electron beam also eliminates delays associated with making photomasks and allows easy pattern changes. In order to use e-beam lithography, however, a suitable lift-off process must be developed. This requires selection of a resist

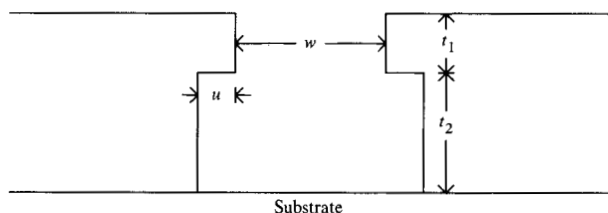


Figure 1 Idealized lift-off profile.

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and testing of a process for applying, exposing, and developing it. The process requirements for Josephson circuits are different from those for other technologies where e-beam lithography has been applied. For example, the materials used in Pb-alloy Josephson junction circuits are not compatible with the high baking temperatures usually employed with resists such as PMMA. While microbridges [16], superconductor-normal metal-superconductor junctions [17], and isolated tunnel junctions [18] have been fabricated by e-beam lithography, the processes used were not suitable for complex Josephson integrated circuits (ICs) of the type described here. This paper first discusses the requirements for an e-beam lift-off process compatible with our present methods of fabricating Pb-alloy Josephson circuits and then describes tests of several resists and processes.

Requirements

The requirements for an e-beam lift-off process for Pb-alloy Josephson junction circuits fall roughly into three categories. First, the proper resist edge profile must be obtained. The process must also be compatible with materials such as the Pb alloys and SiO used in the circuits. Finally, linewidths must be carefully controlled.

An idealized profile for a lift-off stencil is shown in Fig. 1. It is generally easier to obtain undercut with electron exposure than with optical exposure. The electron beam spreads during passage through the resist, and exposure near the substrate is enhanced by backscattered electrons. Assuming that the evaporant follows a straight line path from the source, the width w controls the size of the deposited pattern. The undercut u must be approximately $0.2\text{ }\mu\text{m}$: large enough to ensure complete lift-off while small enough to permit closely spaced lines and small resist islands. The amount of undercut can also determine critical pattern dimensions. For example, when SiO is evaporated, a thin layer of the insulator is found under the overhang up to the point where the resist foot touches the substrate [5]. The lip thickness t_1 should be about $0.3\text{--}0.4\text{ }\mu\text{m}$ to allow for erosion during plasma oxidation, while t_2 must be large enough to permit depositions of the desired thickness.

The materials used in Josephson ICs impose process requirements different from those imposed in other technologies. For circuits fabricated using Pb-alloy metal-lurgy, the resist baking temperature is limited to about 70°C to minimize stress relaxation in the films [19]. Resist processes calling for significantly higher temperatures [8, 9] are thus unsuitable. In addition, the techniques used in other technologies to promote adhesion of the resist to the substrate have not always been applicable for the Pb-alloy and evaporated SiO surfaces used here.

Deviations in pattern dimensions from the design values cause undesirable changes in circuit electrical parameters, with consequent reductions in performance and yield. Linewidth errors of several types are observed for e-beam lithography. The first is an overall linewidth bias, which can sometimes be corrected by adjusting the design dimensions. Since lines generally become wider than the width exposed, only a limited amount of correction can be applied before the exposed width becomes vanishingly small. For $1\text{-}\mu\text{m}$ dimensions, a bias of approximately $0.2\text{ }\mu\text{m}$ per edge is the maximum that can be tolerated. Pattern-dependent linewidth variations are also observed. The resist develops more rapidly over underlying Pb patterns than over Si or SiO due to the larger number of backscattered electrons produced by materials of higher atomic mass. In addition, electrons may be scattered from one shape to an adjacent one, leading to linewidth changes depending on the proximity of one shape to another (proximity effects). These errors can be reduced by proximity correction techniques [20]. Other linewidth errors include random variations from wafer to wafer and between sites on the same wafer. These errors can be caused, for example, by changes in resist thickness or properties, baking conditions, and development conditions. Reasonable processing variations must not cause excessive linewidth changes.

In addition to these specific requirements for the Josephson process, a resist with high electron sensitivity is desirable to increase wafer throughput.

Resists investigated

• Poly(methylmethacrylate)

Poly(methylmethacrylate) (PMMA) has been widely used as an electron resist for many years [8]. It is a positive resist; *i.e.*, electron exposure reduces the average molecular weight of the polymer and increases its solubility in the developing solvent. The resist film is generally baked before exposure at about 160°C to drive out the solvent and reduce the development rate of the unexposed resist. Under proper exposure and development conditions, an undercut profile is obtained, reflecting the exposure profile.

The PMMA was evaluated using wafers coated with resist and baked at 70°C for 90 min. All experiments used du Pont TMElvacite 2041 PMMA dissolved in diglyme as a casting solvent. The resist was exposed at several doses with electrons accelerated to different energies. Development was carried out in a 1:2 mixture of methylisobutylketone and isopropanol. With the $20\text{--}25\text{-keV}$ ($\approx 3\text{--}4 \times 10^{-15}\text{ J}$) electron energies usually used in our exposure systems, no undercut could be obtained at any electron

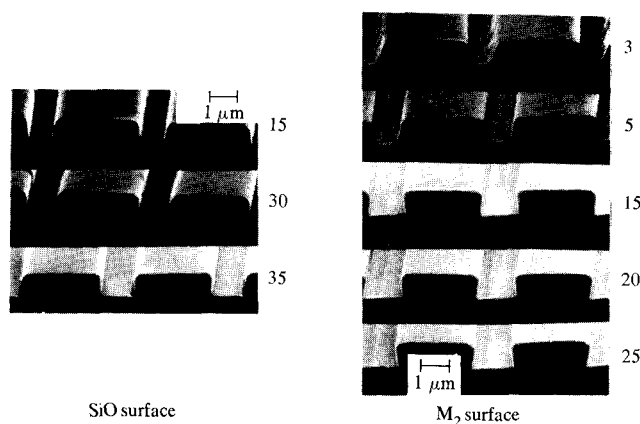


Figure 2 PMMA profiles after various development times (in seconds) for resist on SiO and Pb-In-Au-alloy (M_2 layer) surfaces exposed with 1.5×10^{-4} C/cm² at 15 keV (2.4×10^{-15} J).

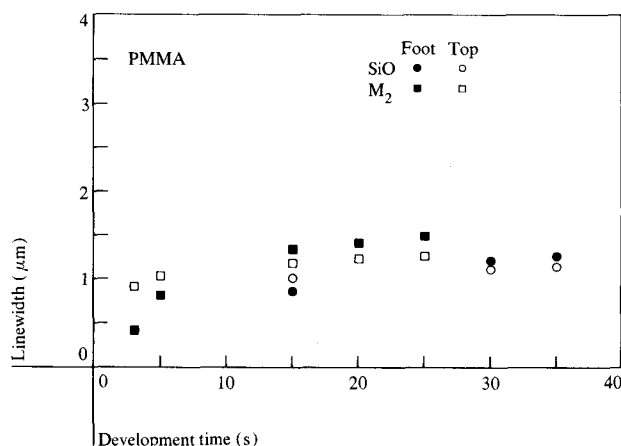


Figure 3 PMMA linewidth vs. development time for 1-μm-wide lines.

dose. Nearly vertical walls were obtained at about 1.8×10^{-4} C/cm². Reducing the electron energy to 15 keV (2.4×10^{-15} J), however, did produce undercut profiles [21]. The lower-energy electrons are scattered more easily in the resist, leading to greater undercut. Resist baked at 160°C showed significant undercut at 25 keV (4×10^{-15} J), indicating that the lower baking temperature degrades the contrast of the resist.

In order to determine the optimum development time and the sensitivity to changes in development, a series of 1-μm-wide lines were written in the resist and developed for various times. Tests were made both on wafers coated with SiO and with Pb-In-Au alloy [13] (M_2 layer) films, the types of surfaces found in Josephson circuits. The wafers were exposed with an electron dose of 1.5×10^{-4} C/cm²

at 15 keV (2.4×10^{-15} J) in a Vectorscan [22] exposure machine. Figure 2 shows scanning electron microscope (SEM) pictures of the lines after development times of 15–35 s for the SiO wafers and 3–25 s for the Pb-In-Au wafers.

The resist profiles should be suitable for lift-off, though they were more rounded than profiles obtained for higher baking temperatures. The line edges on the patterns were very smooth compared to those for some of the diazo resists tested. In some cases, however, cracking of the resist during development was observed at the corners of exposed shapes.

The profiles shown in Fig. 2 were measured to determine the linewidth as a function of development time, with the results shown in Fig. 3. Linewidths produced by removal of the exposed resist were measured both at the narrowest part near the top (top width) and at the substrate (foot width). The resist developed more rapidly on the Pb-alloy surface due to the larger number of backscattered electrons. The optimum development time was about 25 s, by which time undercut was obtained on the SiO surface. After 25 s of development, the top linewidths on the SiO and Pb-alloy surfaces were ≈ 1.1 and $1.25 \mu\text{m}$, respectively, significantly greater than the exposed width of $1.0 \mu\text{m}$. In order to write 1-μm devices with reasonably accurate linewidths, substantial corrections would have to be applied to the pattern data. These corrections would be difficult to apply because they depend on the underlying material.

An experiment was performed to evaluate linewidth variations across a wafer for patterns written in PMMA. Test patterns were written on two 25-mm wafers, one coated with SiO and the other with a Pb-alloy (M_2) film. The wafers were exposed with a 4×4 array of 2-mm-square test chips. Each chip pattern contained 60 2.5-μm-wide by 2-mm-long lines separated by various spacings, 100 1.0-μm-wide lines 2 mm long with various spacings, and an array of 10^4 2.5-μm-square resist islands. Figure 4 shows examples of the line and island measurement sites. These are representative of many of the shapes that appear in Josephson devices.

After development, scanning electron micrographs (SEMs) were taken of several 2.5-μm islands and 2.5-μm-wide lines on each of four chips spaced in a row across the wafer near its center. The photographs were then measured, using the period of the lines as a length scale. The measurement accuracy was estimated to be $\approx 0.03 \mu\text{m}$. The sizes of the 2.5-μm resist islands were measured both at the widest part and at the substrate; the 2.5-μm line openings were measured only at the narrow-

est point. In each case, roughly 80 sites were measured. Table 1 contains the mean linewidths and standard deviations for all types of sites. The resist islands, as expected, were substantially smaller than the nominal 2.5- μm size. Likewise the 2.5- μm line openings were wider after development than the exposed dimension. The standard deviations are small, comparable in this case to the measurement uncertainty. This simple test is not adequate, however, to determine linewidth control on actual device wafers with complex patterns and topography from underlying layers. More detailed measurements on a larger number of wafers would be required to determine practical process tolerances.

The sites used for linewidth tolerance measurement also provide a method for testing adhesion of resist to the substrate. For both the closely spaced lines and the islands, the resist area in contact with the substrate is quite small, and loss of adhesion for these features is easily observed. A sensitive though qualitative measure of adhesion is obtained by observing missing resist islands or lifted resist strips between closely spaced lines. By using PMMA on either SiO or Pb-alloy surfaces, wafers with 1.6×10^5 resist islands could be made without loss of any islands. The smallest island to be made in large arrays had a width measured at the substrate of about 1.6 μm . Small numbers of islands below 1 μm were made without apparent adhesion problems.

These results indicate that PMMA could possibly be used in the fabrication of Josephson circuits. The low baking temperature required, however, degrades resist contrast and introduces a large process bias. In order to produce true 1- μm lines, a width of roughly 0.5 μm would have to be exposed. This factor, along with the low sensitivity of the resist and the problems with cracking during development, led to the consideration of alternate materials.

• PMMA-terpolymer double layer resist

A resist system used successfully in patterning FET memory and logic chips [9] consists of a layer of PMMA covered by a thin layer of a copolymer resist [23]. In the process used for silicon circuits, a baking temperature of 160°C is used. The required electron dose is $\approx 1 \times 10^{-5}$ C/cm². The ability to develop the two resist layers separately in different solvents leads to several potential advantages [24]. High resolution is possible because the image is defined in the thin upper resist layer, which is not attacked by the solvent used to develop the PMMA layer and produce the undercut. The amount of undercut may be controlled by the time in the second developer. On wafers already patterned with layers of different thicknesses, the lower resist layer planarizes the surface, mini-

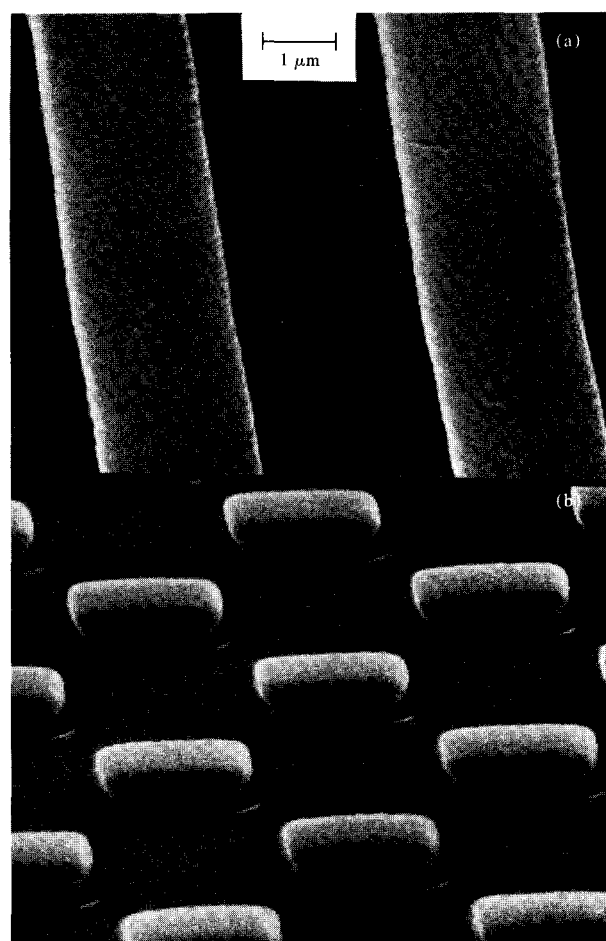


Figure 4 Examples of 2.5- μm line (a) and island (b) test sites for linewidth control measurements on PMMA.

Table 1 Linewidth control data for PMMA and ®AZ-1350J resists.

Resist	Thickness (μm)	Substrate	Site	Mean (μm)	Standard deviation (μm)
PMMA	0.7	SiO	island top	2.16	0.03
			island foot	1.66	0.03
	0.7	M_2	line top	2.78	0.04
			island top	1.99	0.03
			island foot	1.69	0.04
			line top	2.89	0.03
®AZ-1350J	0.7	Si	island top	2.50	0.04
			island foot	1.68	0.07
			line top	2.67	0.04
	0.7	M_2	island top	2.49	0.04
			island foot	1.79	0.06
			line top	2.58	0.03
®AZ-1350J	1.4	Si	island top	2.52	0.04
			island foot	1.42	0.23
®AZ-1350J + oil ^a	1.4	Si	island top	2.52	0.03
			island foot	1.82	0.19

^aUnion Carbide L-45 silicone fluid; 20 ppm.

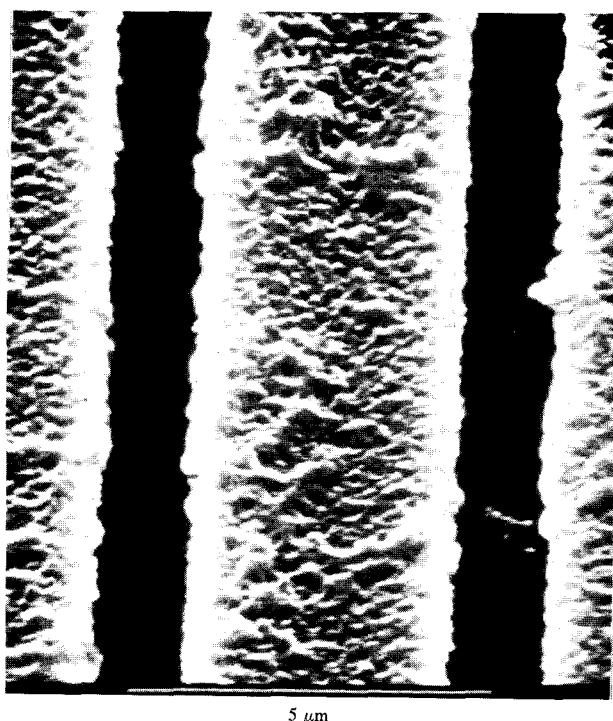


Figure 5 PMMA-terpolymer double-layer resist which shows coarse grain and rough line edges; scale bar is 5 μm .

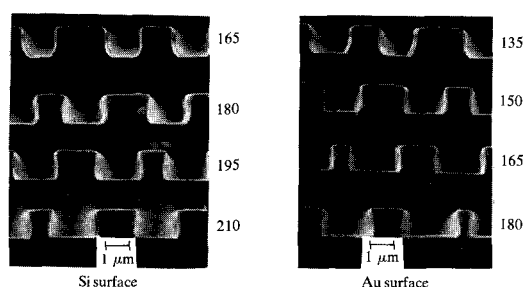


Figure 6 AZ-2400 profiles after various development times (in seconds) for resist on (bare) Si and Si on which a film of Au has been evaporated; exposure of $4 \times 10^{-5} \text{ C/cm}^2$.

mizing thickness variations in the upper image-forming layer. The amount of undercut, however, will vary depending on the lower resist thickness.

We performed a series of experiments using an underlying film of $\text{TMElvacite 2041 PMMA}$, which was baked at 70°C after application. In hope of obtaining some of the benefits observed with high-temperature baking, we used

copolymer resist that had been converted to terpolymer [25] by baking the powder at $200\text{--}230^\circ\text{C}$. A solution of the resist was dropped onto the surface of a spinning wafer to prevent the dissolution of the PMMA by the copolymer solvent. After again baking at 70°C , wafers were exposed at doses from 1×10^{-5} to $3 \times 10^{-5} \text{ C/cm}^2$. The copolymer was then developed in a mixture of ethyl TM Cellosolve [2-ethoxyethanol (trademark, Union Carbide Corp.)] and isopropanol. After a rinse in isopropanol, the PMMA was developed in chlorobenzene.

The results obtained for this process were much inferior to those observed with a 160°C baking temperature. As shown in Fig. 5, the surface of the terpolymer resist became very grainy during development, leading to ragged line edges. Cracking of the resist near the corners of developed shapes was also observed. In addition, a granular residue, which appeared to form at the interface between the two resist layers, adhered to the substrate after development and could not be removed by either developer. These problems caused us to abandon this resist system.

• *Diazo-type resists*

Diazo-type resists, which include AZ-1350J and AZ-2400 , are widely used for optical lithography and perform well with low prebake temperatures. These resists are also known to be sensitive to electrons [26, 27]. Both optical and electron exposures destroy the photoactive compound, leading to more rapid removal of the resist in an alkaline developer. Development rates for electron exposure are generally lower than for optical exposure, often requiring the use of strong developers and long development times. This can lead to loss of adhesion between the resist and the substrate.

AZ-2400

The first diazo resist to be examined was AZ-2400 . After the application of hexamethyldisilazane (HMDS) [28] as an adhesion promoter, the resist was spin-coated onto the wafers and baked for 30 min at 70°C . Patterns were exposed, usually at a dose of $4 \times 10^{-5} \text{ C/cm}^2$, and the resist was developed in a mixture of 1 part AZ-2401 developer to 4.75 parts water.

Patterns of parallel lines were written in AZ-2400 and developed to determine linewidth and edge profile as a function of development time. Exposures were carried out in a different machine than was used previously, resulting in lines with nominal widths of $1.5 \mu\text{m}$. Figure 6 shows resist profiles after various development times for AZ-2400 exposed at $4 \times 10^{-5} \text{ C/cm}^2$ on a bare Si substrate and on a substrate coated with an evaporated Au film. The linewidths were measured as a function of de-

velopment time for both substrate materials with the results shown in Fig. 7. In order to obtain an undercut on the Si substrate, a development time of about 210 s was required. At this time the linewidth on the Si substrate was $\approx 1.8 \mu\text{m}$, indicating a large process bias. On the gold surface, the lines were so broadened by this time that it was impossible to write $1\text{-}\mu\text{m}$ lines with a $1\text{-}\mu\text{m}$ separation. The difficulty in obtaining an undercut profile is an indication of poor contrast between the exposed and unexposed resist. Significant variations in resist contrast, as measured by the ability to produce undercut profiles, were observed between different lots of the resist.

Adhesion tests were also made for AZ-2400 using the line and island test sites described previously. The resist was found to adhere well to SiO_2 . Variable results, however, were seen on Pb-alloy surfaces. Adhesion was often adequate, but on certain wafers the narrow resist lines buckled and the small islands were lost. In view of the poor contrast, marginal adhesion, and lot-to-lot variability, work on this resist was abandoned in order to concentrate on the more promising AZ-1350J .

AZ-1350J with chlorobenzene soak

An optical lift-off process using AZ-1350J has been described, in which the resist is soaked in chlorobenzene to produce an undercut edge profile [6, 7]. The chlorobenzene soak reduces the development rate near the resist surface and provides a reproducible undercut under a wide range of processing conditions. This approach has been used to develop a process for fabricating Josephson integrated circuits [13]. We have attempted to improve the resolution of the process by substituting electron exposure for optical exposure. Our experience with AZ-1350J makes the use of the same resist for e-beam exposure very attractive, since this material is known to be suitable for all steps in the Josephson process. The procedure used here for applying and processing the resist was based on previous experience with optical exposure [6, 7, 29]. The process used was similar to that just described for AZ-2400 , with the introduction of the chlorobenzene soak after completion of part of the 70°C bake.

The evolution of the resist profile as a function of development time was studied for two wafers, one covered with an SiO_2 film and the other with a Pb-In-Au alloy (M_2) film. A pattern of $1\text{-}\mu\text{m}$ parallel lines was exposed at $4 \times 10^{-5} \text{ C/cm}^2$ and developed in undiluted AZ developer. Before development the wafers were split into several pieces, each of which was developed for a different time. Figure 8 shows the resist profiles after various development times on the two surfaces. The profiles appeared to be determined primarily by the soak process

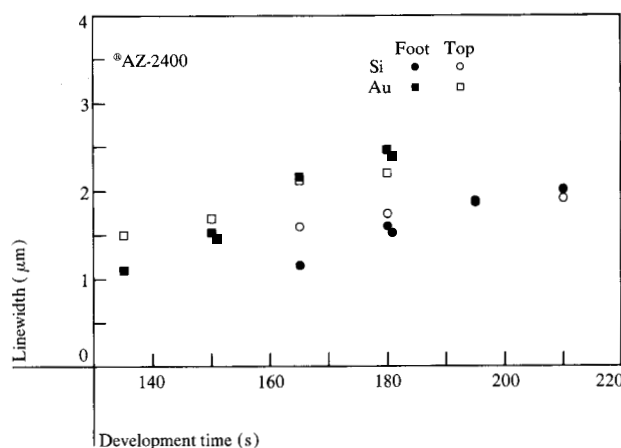


Figure 7 AZ-2400 linewidth vs. development time (in seconds) for nominal $1.5\text{-}\mu\text{m}$ -wide lines.

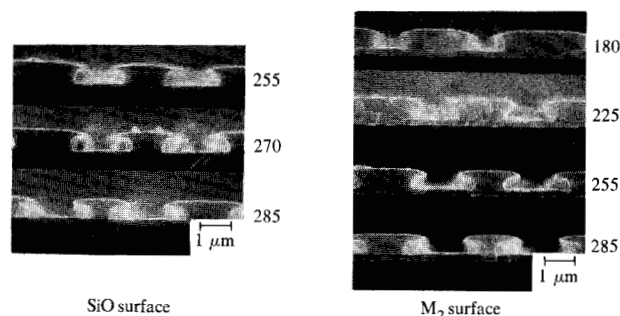


Figure 8 AZ-1350J profiles after various development times (in seconds) for resist on SiO_2 and M_2 surfaces exposed at $4 \times 10^{-5} \text{ C/cm}^2$; standard 70° bake.

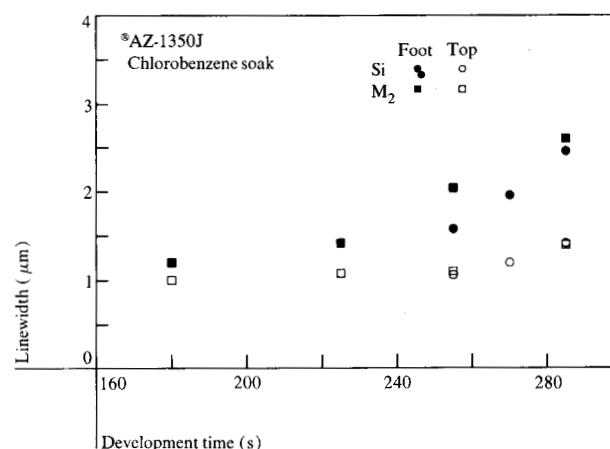


Figure 9 AZ-1350J linewidth vs. development time (in seconds) for $1\text{-}\mu\text{m}$ -wide lines.

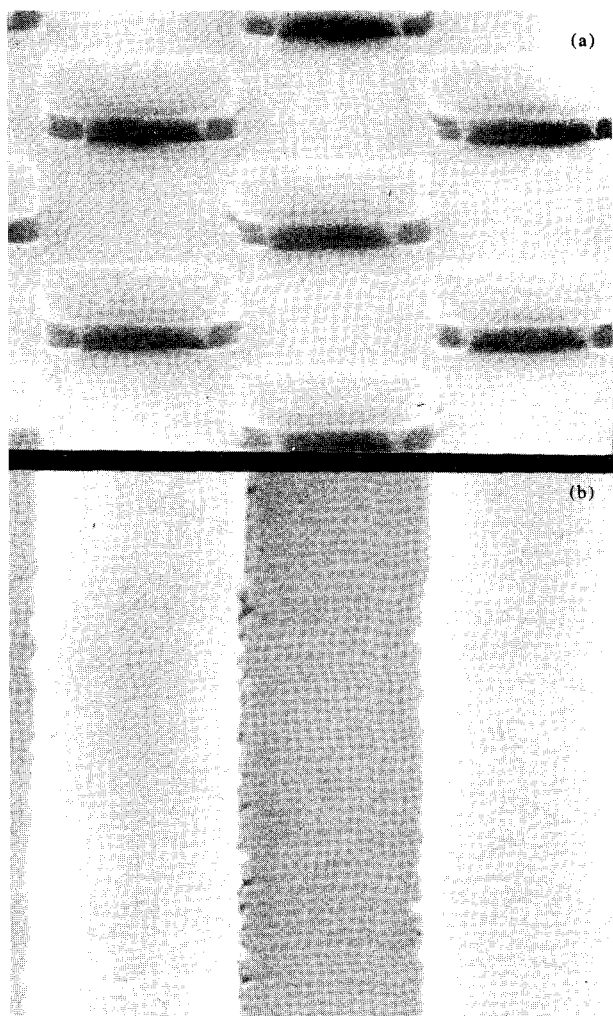


Figure 10 Examples of 2.5- μm island (a) and line (b) test sites for linewidth control measurements on AZ-1350J .

and to be relatively unaffected by the backscattered electrons from the substrate. The linewidths did not change greatly from heavy to light atomic weight substrates. This was different from processes not involving surface treatment, for which the undercut profile mirrored the exposure profile. The thickness of the lip was also independent of resist thickness, which may minimize any linewidth changes occurring across the underlying vertical structure on the wafer.

The linewidths at the top and the foot were measured as a function of development time; the results are shown in Fig. 9. The lateral development rates for the line tops were quite small compared to the rates at the substrate, leading to the large undercut seen in the photographs. In order to obtain an undercut on the SiO surface, a develop-

ment time of about 250 s was required. By this time the resist on the Pb-alloy surface showed an undercut of about $0.5\ \mu\text{m}$, which limited the minimum spacing between exposed lines to $\approx 1.5\ \mu\text{m}$. Thus, $1\text{-}\mu\text{m}$ resist islands could not be written. It is probable that some variations of the soak process could be developed that would not retard the development rate in the top layer of the resist as strongly while maintaining the present lip thickness. Such a modification would be necessary to write circuits with $1\text{-}\mu\text{m}$ spacing between features, though isolated structures below $1\ \mu\text{m}$ in size can be written.

The adhesion of AZ-1350J to both SiO and Pb-alloy surfaces was tested by developing patterns of closely spaced lines and islands as described above. On a wafer with 1.6×10^5 resist islands $\approx 1.7\ \mu\text{m}$ wide as measured at the substrate, a few were typically missing, generally near visible dirt on the wafer. A few smaller islands with widths $< 1\ \mu\text{m}$ at the substrate were written without adhesion loss.

Measurements of linewidth variation from place to place on a wafer were performed for AZ-1350J as described above for PMMA. Patterns were written and measured on two wafers, one of bare Si and the other coated with M_2 . The bare Si wafer was developed for a longer time than the other. About 80 $2.5\text{-}\mu\text{m}$ resist islands and a similar number of $2.5\text{-}\mu\text{m}$ -wide lines were measured across each wafer. Figure 10 shows examples of the line and island test sites. These photographs show a pronounced roughness at pattern edges characteristic of the chlorobenzene-soaked resist. This roughness has a period much smaller than the width of the lines written here, but it could contribute to linewidth variations for narrower lines.

The average linewidth and standard deviation for all sites are included in Table 1. The pattern dimensions at the top of the resist corresponded to the design dimensions within $0.02\ \mu\text{m}$. The linewidth variations measured at the resist surface were comparable to measurement uncertainty, while the variation at the substrate was larger. This may reflect the difference in lateral development rates pointed out above. If development occurs more rapidly in one region than another, the increased development will cause less change in the linewidth at the top than at the substrate. Linewidth did not appear to vary systematically across the wafer, as might be caused by changes in resist thickness. The mean linewidths at each of the four chip sites did not vary significantly.

One possible cause of undercut variation is radial striations visible in the developed resist films as seen in Fig. 11(a). These appear to result from some periodic variation

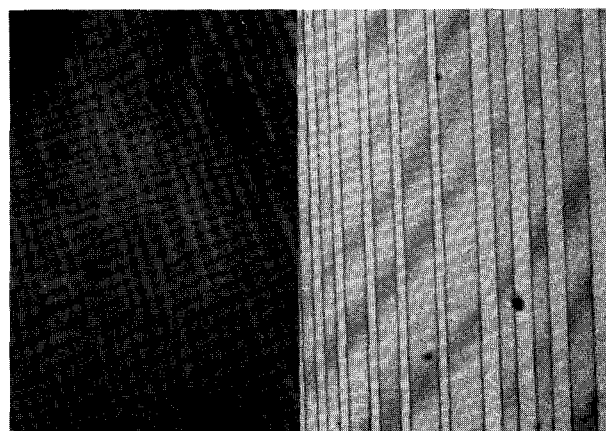
in the resist film with a period of 30–50 μm . An attempt was made to determine the importance of striations by reducing their magnitude through the addition of silicone oil to the resist [30]. Adding about 20 ppm of Union Carbide L-45 silicone fluid to the resist did appear to reduce the magnitude of striations, as shown in Fig. 11(b). Line-width variation measurements were then made to determine whether any improvement could be detected. Resist films 1.4 μm thick were used to magnify the effect of striations on linewidth. The sizes of 2.5- μm islands were measured for resist with and without silicone oil. The standard deviations for the foot sizes were much larger than for the 0.7- μm -thick resist. In spite of the apparent reduction in striations, there was little difference between the standard deviations for wafers with or without silicone oil, suggesting that striations may not be the dominant cause of linewidth variation.

In view of these results, the cause of the observed linewidth variations is not understood. Observations on the development uniformity of blanket resist films suggest that some variation is inherent in the wet-development process. An investigation of such nonuniformities and their causes would be of interest.

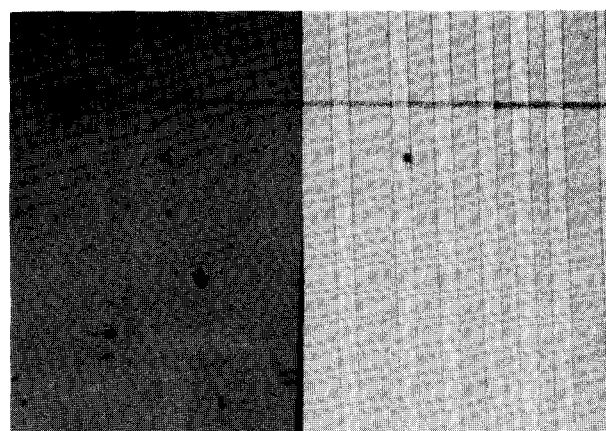
Conclusions

The requirements for this lift-off process for Pb-alloy Josephson devices and integrated circuit configurations have been examined, and several resists and processes have been studied in relation to these requirements. The desired resist must be compatible with the materials used in Josephson circuits and must provide reproducible lift-off profiles with good linewidth control. This preliminary evaluation suggests that ®AZ-1350J with chlorobenzene soak can meet many of these requirements.

With this process, ®AZ-1350J performs well at the baking temperatures used and provides reproducible profiles. Adhesion to Pb-alloy and SiO_2 surfaces is good. The required exposure of $4 \times 10^{-5} \text{ C/cm}^2$ is about a factor of three lower than that necessary for PMMA. The linewidth measured at the lip near the top of the resist accurately reproduces the exposed width, and linewidth variation measurements suggest that tight control of this dimension is possible. Greater variation is seen in widths measured at the substrate. Thus, pattern dimensions for SiO_2 layers may be more poorly controlled than those for evaporants traveling in a straight line from the source. The most serious disadvantage of the process is the large undercut of about 0.5 μm . This presently limits the minimum distance between developed pattern shapes to $\approx 1.5 \mu\text{m}$. It may be possible to change the soak process to produce a smaller undercut as well as to reduce the roughness of line edges.



(a)



(b)

Figure 11 Striations in ®AZ-1350J (a) without silicone oil and (b) with silicone oil.

Poly(methylmethacrylate) baked at 70°C and exposed with 15-keV ($2.4 \times 10^{-15} \text{ J}$) electrons also has a reproducible lift-off profile, and the undercut is less than that obtained with ®AZ-1350J ; it also adheres very well to the substrates used. However, the resist contrast is degraded by the low baking temperature, causing exposed and developed features considerably wider than the designed dimension. The amount of broadening depends on the substrate material. An exposure of about $1 \times 10^{-4} \text{ C/cm}^2$ is required, and the resist is prone to cracking during development. For these reasons ®AZ-1350J appears preferable at this time to PMMA for the e-beam patterning of Josephson devices and circuits.

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