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A Charge Injection Transistor Memory Cell

In this paper, two versions of an experimental bipolar dynamic memory cell are described. The memory cell consists of one p-channel MOSFET and a bipolar npn transistor with extensive node sharing. The MOSFET device controls the charge injection into the floating base of the npn transistor, and the bipolar device provides amplification for the stored charge during read operation. For memories, this cell offers performance associated with bipolar technology and chip density comparable to MOSFET memories.

Introduction

In LSI high-density main memory technology, the single-device capacitive storage metal-oxide-semiconductor field effect transistor (MOSFET) has been dominant. However, bipolar dynamic random access memories (RAMs) have also been developed [1-2]. The basic difference between the MOSFET RAM and the bipolar RAM, besides the technologies, is that the bipolar RAM cell has a built-in individual amplification mechanism. In the bipolar dynamic RAMs in [1] and [2], the stored charge is controlled by a lateral pnp bipolar transistor. Another experimental bipolar dynamic RAM cell using a different approach [3], also with built-in amplification, is described in this short paper. In the new charge injection transistor memory (CITM) cell, charge injection into the storage node of the memory cell is controlled by a p-channel MOSFET device. In the read/write operations of one memory cell, voltage-level shifting of the bit line will have a substantially less disturbing effect on the stored charge of adjacent cells (those cells sharing the same bit line) in the CITM than in the previous bipolar dynamic RAMs. The cell configuration and the write/read operation of the CITM are discussed, and hardware test sites and test results are shown.

Memory cell and test site description

Two versions of an experimental CITM cell have been fabricated. One has two metal lines (write and read), and the other has one metal line, the write line and the read line merging into a single word line. In each memory cell, a p-channel MOSFET device is provided to control the injection of charge into the floating base of a bipolar npn transistor, which amplifies the charge during the read operation. Due to the sharing of many electrodes typified by the merged transistor logic approach (MTL or I^2L) [4], each CITM cell occupies a silicon area substantially less than that of a single conventional bipolar npn transistor with isolation walls and three leads. The base of the npn is floating, so no outside contact or lead is required. Device cross-sections and circuit configurations of these two versions are shown in Figs. 1 and 2.

During write operations, a negative voltage is applied to the write line in Fig. 1 or to the word line in Fig. 2. The p-channel MOSFET device is turned on. Writing a *one* or a *zero* is determined by whether or not there is a positive voltage applied to the bit line. This voltage, in turn, controls whether or not a finite amount of positive charge, Δq, is injected into the storage capacitor. The capacitor is formed by the base-collector junction of the npn transistor. During a read operation, the read line in Fig. 1 or the word line in Fig. 2 is pulled downward. If a *one* is stored in the cell, the npn transistor will be turned on and a sense signal containing a charge of $\beta\Delta q$ will show up in the sense line. If a *zero* is stored in the cell, there will be no sense signal except for some coupling noise.

In the two-metal-line version, no dc current flows through the cell during any phase of operation. In the one-

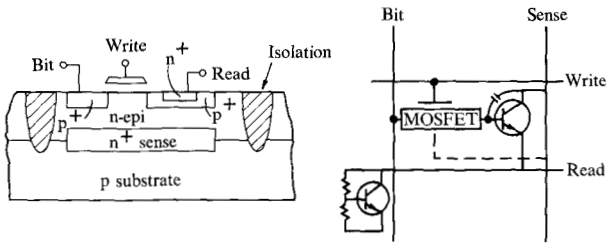


Figure 1 Two-metal-line CITM and circuit configuration.

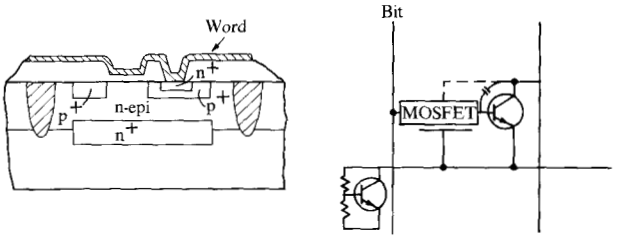
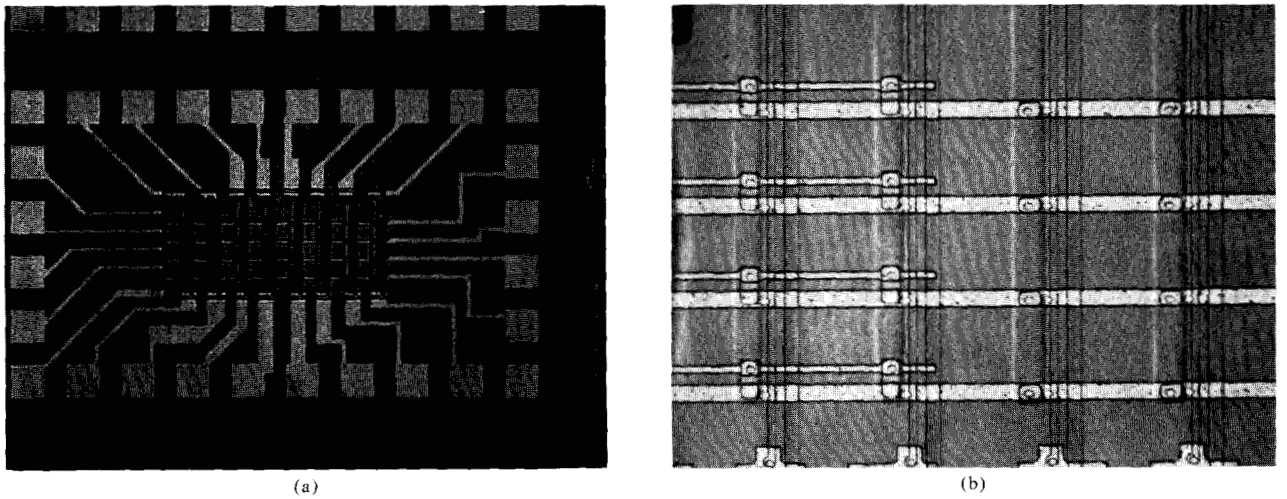


Figure 2 One-metal-line CITM and circuit configuration.



(a) (b)

Figure 3 (a) A 4 × 8 CITM array of memory cells. (b) Expanded view of part of an array.

metal-line version, a controlled dc current flows during the Write/1 operation. During the Read/1 operation, the stored charge in the npn base has two outlet paths. One path is through a forward-biased npn base-emitter junction, which results in an amplified signal at the sense line; the other path is through the conducting p channel of the MOSFET, back to the bit line, and is unused. Because of the vast difference of the *RC* time constants of these two paths, the first path will be selected and the second ignored. Both computer simulation and bench tests substantiate this.

The CITM cell consumes no power in its quiescent state. In each read or regeneration, it consumes an average of approximately $\Delta q(\Delta V_B = \beta \Delta V_S)/2$ joules, where ΔV_B is the bit line voltage swing and ΔV_S the sense line voltage swing. It is assumed that the probability of storing a *one* or *zero* in a cell is equal.

Each test site consists of a 3 × 3 matrix, and each element in the matrix is a 4 × 8 array of memory cells with 28 I/O pads. The cells were laid out with three different ground rules of from 2.5 to 5 μm minimum linewidth or spacing. One element of a matrix (70×) and the expanded view of part of an array (700×), populated equally with the one-metal-line and the two-metal-line cells, are shown in Fig. 3. The gate oxide of the p-channel MOSFET was formed with 70 nm thermal oxide and 15 nm PSG. The CITM may be processed in any standard bipolar technology with one additional step for the processing of the thin gate oxide. The gate oxide is visible under the metal line in the expanded view of Fig. 3.

Test results

The test results for the two-metal-line and the one-metal-line versions are shown in Figs. 4 and 5, respectively. Most of the Read/0 signal results from the coupling of probe leads. Other probe lead coupling that can be seen in Figs. 4 and 5 is between the bit and sense lines. In both versions, the signal ratio between a Read/1 and a Read/0 signal in the sense line is greater than 50. This Read/1 to Read/0 ratio is much greater than that of a single-device MOSFET cell. A simpler sensing circuitry and a faster access time are the results.

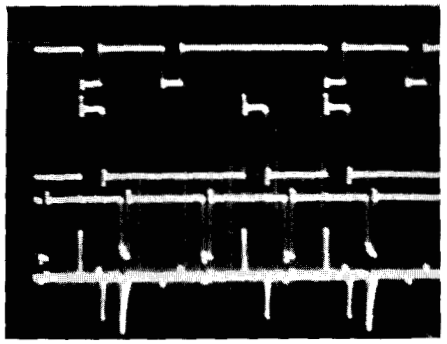


Figure 4 Waveforms showing test results of a two-metal-line CITM.

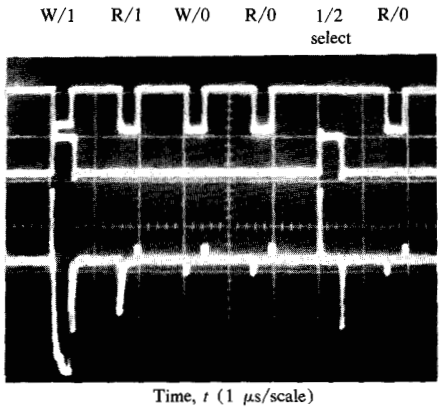


Figure 5 Waveforms showing test results of a one-metal-line CITM.

One of the most important factors for dynamic memory performance is the information retention time at an elevated temperature. The retention time is determined by total leakage current flowing into or out of the storage node (the floating base) during the quiescent state. Test results at 85°C for both the one- and two-line versions show that one second after a Write/0, a Fat/0 reading with about half the charge of a Read/1 signal appears in the sense line.

Characteristics of the CITM

Bipolar memory cells, operating on a charge or current injection principle, utilize a forward-biased pn junction to control the injection (such as the emitter-base junction of a bipolar pnp transistor in the memory cells shown in [1] and [2]). Two-dimensional isolation or a guard ring is generally provided to guide the injected charge toward its destination. In a CITM cell, a p-channel MOSFET is used for injection control. The pn junction of the p bit line and the n-epi will always be reverse-biased, and the injection is guided by a conducting channel during the write operation. The charge will go only to the designated place. Hence, the CITM memory array needs only one-dimensional isolation. A conventional semi-recessed oxide isolation wall or a deep diffusion isolation takes up a silicon area of approximately $2D + W_{min}$, where D denotes the thickness of the epitaxial layer and W_{min} denotes the minimum width allowed by a specific layout rule. The spacing between two adjacent CITM cells, on the other hand, can be as close as W_{min}, limited only by the punchthrough voltage. A two-metal-line CITM, therefore, can have a packing density comparable to that of an I^3L dynamic RAM cell [2]. In addition, a one-metal-line CITM may have roughly twice the density of its two-metal-line counterpart in the array area.

A p-channel MOSFET has a rather large turn-on resistance R_p. However, because the injecting charge is stored in a very small capacitance C_s, with proper design this R_pC_s time constant, during the write operation, may be only a few ns. If desired, the time constant of the p-diffusion bit line may be reduced by adding a second-level-metal line which runs parallel to and makes contact periodically with the p diffusion. During the read operation, the sense current flows through a high-performance bipolar npn transistor. A read-operation RC time constant, determined by the sense line capacitance and the sensing circuit resistance, can, therefore, be even smaller. This small sensing time constant and a large sense signal enable the CITM to have a very fast access time.

In either the two-metal-line or one-metal-line CITM cell, only one metal-to-semiconductor contact per cell is required. In comparison, an I^3L cell requires two contacts. Since the charge is stored in the floating base of an npn transistor, a CITM cell is not very sensitive to pipe defects, which are resistive shorts between the emitter and the collector of the npn transistor. A CITM cell could operate with some degradation of current gain with a high-resistance pipe, assuming that the sensing circuit impedance is at least one or two orders of magnitude smaller.

In CITM cells, a negative power supply will be required to turn on the p-channel MOSFET device. For an epitaxial doping of approximately 2×10^{16}, with a Q_{eff} of 2×10^{11} and an oxide thickness of 50 nm, the calculated threshold voltage will be -3 V at zero substrate bias. (An ion-implantation surface treatment, a slight reduction of epi doping, or some reduction of Q_{eff} could lower the threshold voltage to -1.5 or -2 V for more desirable power and performance considerations.) Another possible concern with CITM cells is the punchthrough voltage between the

p-region injector and the floating p base. At 2×10^{16}, the depletion width at the epitaxial region will be approximately one micrometer at 14 V reverse bias.

Conclusion

The CITM cell uses a p-channel MOSFET to control charge injection. The processes are those of a standard bipolar process with an oxide-gate step added. As a result, the CITM cells do not require two-dimensional isolation for density improvement and are free from the write-disturb problem of the I^3L memory cell. With an amplified signal during the read operation, the sensing circuitry of the CITM is simpler, and a faster access time results. The CITM cell has the advantage of high performance associated with bipolar technology while offering a chip density comparable to that of single-device MOSFET dynamic memory cells. No substantial penalty in power dissipation is expected.

References

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