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Implanted Source/Drain Junctions for Polysilicon Gate Technologies

Shallow (<1.0-μm) n^+-p junctions are required for dense dynamic FET memory. Ion implantation is a natural technology to fulfill the geometric requirements of shallow highly doped n^+ regions in a dual polysilicon gate IGFET technology. However, implantation of ^{31}P and ^{75}As at high dose levels severely damages the crystal lattice and subsequently is difficult to anneal. This tends to make implanted junctions more leaky than their diffused counterparts and causes them to have lower apparent reverse breakdown voltages. The detrimental effect of residual end of process damage, resulting from the implantation, is correlated to the electrical characteristics of the n^+-p junction. A junction process technology is described that can provide leakage levels of less than 0.25 fA/μm^2 (25 nA/cm^2), sharp reverse I-V characteristics, and junction depths of 0.25 to 1.0 μm.

Introduction

Traditionally n-channel IGFET source/drain junctions have been formed by normal thermal diffusion techniques using various doping sources. Recent trends in silicon integrated circuits to smaller horizontal geometries have also required vertical scaling of the device [1]. VLSI-type IGFET devices require p-n junction depths of 0.2 to 1.0 μm [2]. Ion implantation with its control of impurity type, concentration, vertical profile, and lateral extent becomes the preferred technology. Because ion implantation is a damage-producing technique due to the impinging energetic ions, annealing the crystal becomes of prime importance and often is not complete [3]. Remaining or residual damage, when made electrically active by precipitation effects (for example, see [4]), can enhance the reverse leakage current if these defects lie near the p-n junction depletion region.

Michel *et al.* [5] investigated a combined diffused and implanted junction (phosphorus, arsenic, and boron) emphasizing the effects of annealing temperature. Shallow (0.2-μm) arsenic-implanted p-n junctions were compared to similar 0.5-μm diffused devices by Kircher [6]. The reverse leakage levels for the implanted devices were comparable to the deeper diffused case. This paper presents experimental results for implanted phosphorus and arsenic junctions (0.25 μm to 1 μm) fabricated using an annealing procedure in conjunction with a dry-wet-dry oxidation cycle. Traditionally thin screening materials are used as a safeguard against implant-introduced surface contamination. Mader and Michel [7] have studied the residual damage for high-dose arsenic implants through thin SiO_2 films. This work shows that proper annealing procedures do eliminate deleterious leakage effects. The results pertain to fully integrated devices as applied to a dual polysilicon gate technology. Using the combined thermal cycle, implanted n^+-p junctions are possible with very low leakage levels, sharp *I-V* characteristics, and adequate reverse junction breakdown voltages.

Three process technology issues dealing with implanted n^+-p junctions are discussed: 1) arsenic *vs* phosphorus [8] as the donor dopant, 2) the effect of various screening materials, and 3) scaling to reduced junction depths. Each topic is separately highlighted with the experimental procedure and results indicated. Arsenic was found to be the preferred specie, based on microstructural analysis, and yielded equivalent results for various screening materials. Shallow junction (0.25 to 0.5 μm) results suggest that the residual lattice change associated with implants through SiO_2 can be contained and

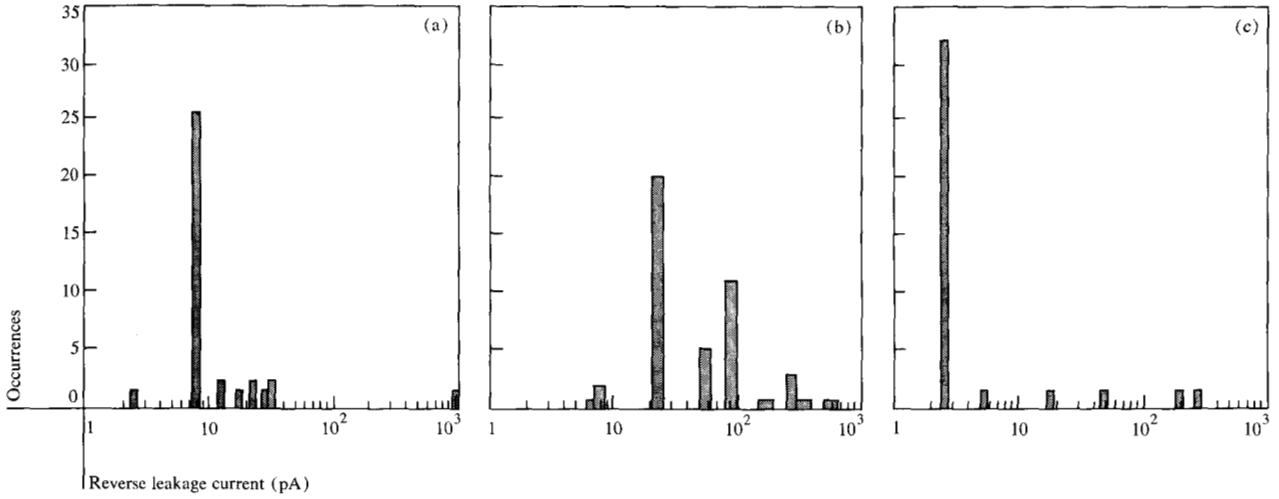


Figure 1 Histograms of reverse leakage current for (a) $POCl_3$-diffused, (b) phosphorus-implanted ($^{31}P^+$, 50 keV, 8×10^{15} ions/cm^2), and (c) arsenic-implanted n^+-p junctions ($^{75}As^+$, 100 keV, 8×10^{15} ions/cm^2). For all histograms, $V_R = -8$ V, $V_G = 0$ V.

minimized with proper thermal wet oxidation and annealing. Wet oxidation was found to be a beneficial anneal for n^+-p-implanted junctions as well as p^+-n devices [9].

Arsenic- *vs* phosphorus-implanted junctions

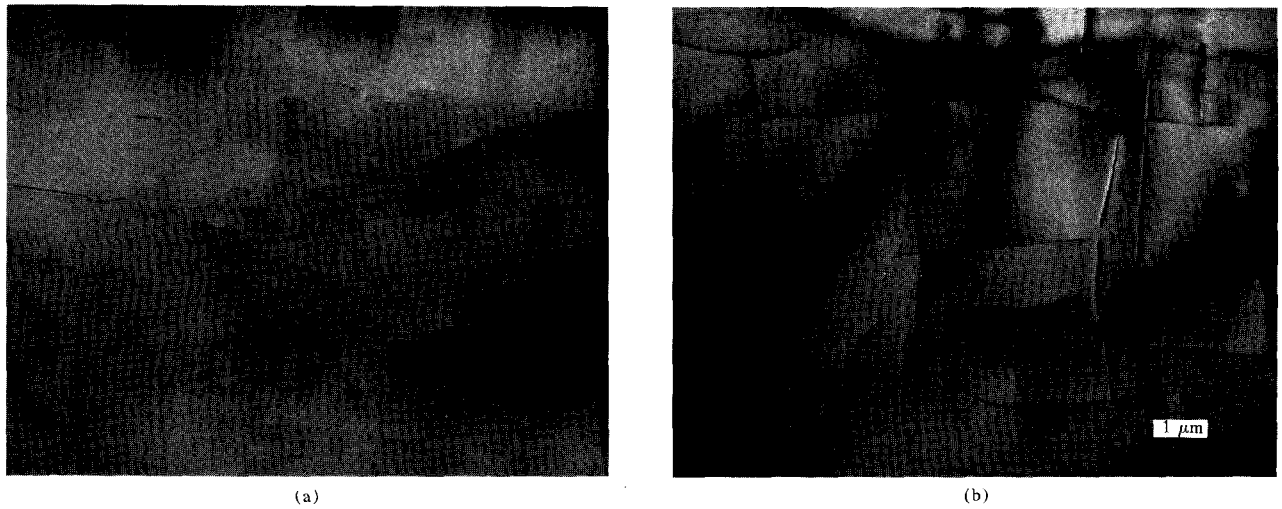
• *Experimental procedure*

The selection of arsenic as the preferred n-type dopant was based on experimentally comparing implanted gated diode structures. Devices were fabricated in a typical IGFET technology using two Ω-cm p-type ⟨100⟩ Si wafers. A field isolation of approximately 750 nm SiO_2 was grown at 1000°C in a conventional manner employing a boron implant for thick oxide threshold enhancement. An optional screen oxide of 20 nm was grown using dry oxygen at 1000°C in the source/drain regions. $^{31}P^+$ and $^{75}As^+$ were implanted at 50 and 100 keV, respectively, to a dose level of 8×10^{15} ions/cm^2 with the wafers mounted 7° off axis. Ion beam current levels were selected to ensure no significant wafer heating during ion implantation. Next, a post-implant cleaning procedure consisting of an oxygen plasma ash followed by a basic-acidic-chemical cycle was used to remove any residual hydrocarbon buildup. Certain wafers had the screen oxide (20 nm) removed chemically, whereas the other wafers had the screen oxide remaining during subsequent processing. Pyrolytic silicon dioxide deposited at 700°C served as a capping film to prevent the loss of the n-type dopant during subsequent annealing for the screened implant samples which were etched prior to the anneal. A preoxidation inert anneal in either N_2 or Ar at temperatures from 900 to 1100°C was investigated. The source/drain reoxidation was a standard dry-wet-dry-inert cycle at 1000°C. Exact times at temperature were varied to provide a final junction depth of 1 μm with sheet resistivities of 10 to 15 Ω/□. Al-Si was applied directly to the n^+ regions without the use of a barrier metallurgy.

Gated diodes [10, 11] (1.94×10^5 μm^2) designed to investigate junction leakage mechanisms were employed for electrical characterization with channel enhancement threshold implants of 10^{12} to 10^{13} ions/cm^2. Thin foils, for analysis by transmission electron microscopy (TEM), were prepared by chemical jet polishing with $HF\text{-}HNO_3$ from the back side of the devices. Argon ion milling at 3 to 4 keV was used to thin the devices from the front side to permit analysis of the defect structure near the 1-μm metallurgical junction.

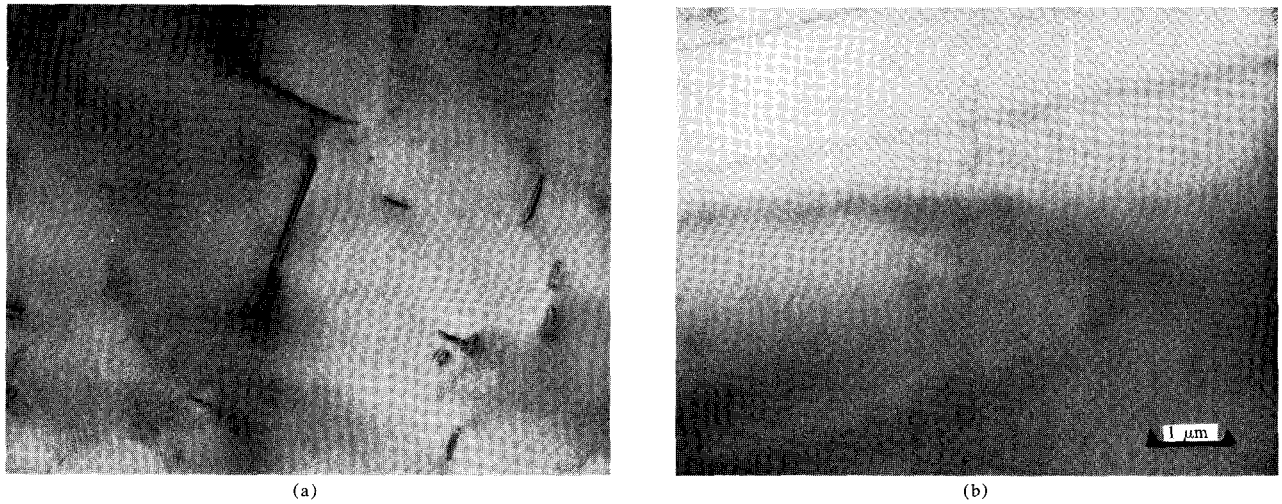
• *Results and discussion*

Histograms of the reverse leakage current for $POCl_3$-diffused, phosphorus-implanted, and arsenic-implanted wafers are shown in Fig. 1. The $POCl_3$-diffused case [Fig. 1(a)] serves as an experimental control for a phosphorus n^+-p junction. However, the junction depth was 1.3 μm compared to 1 μm for the implanted device [Fig. 1(b)]. The preoxidation anneal was performed in N_2 at 1000°C and represents the best consistently obtained result with a screen oxide in place for ion-implanted phosphorus devices. Figure 1(c) is for an arsenic device with screen oxide having received a preoxidation N_2 anneal at 1100°C. With zero volts applied to the gate, these devices have the gated region in depletion; therefore, the reverse leakage is due to the junction and surface components. The implanted arsenic devices were approximately three times better than the 1.3-μm $POCl_3$-diffused control, whereas



(a) (b)

Figure 2 TEM micrographs of phosphorus-implanted device showing dislocations (a) at the surface (0–200 nm deep) and (b) near depletion region (700–900 nm deep) of junction.



(a) (b)

Figure 3 TEM micrographs of arsenic-implanted device showing dislocations (a) at the surface (0–200 nm deep) and (b) near depletion region (800–1000 nm deep) of junction.

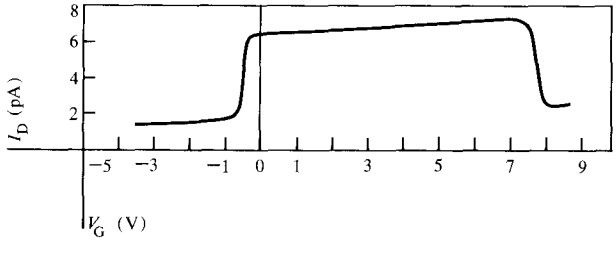


Figure 4 I_D *vs* V_G for arsenic (8×10^{15} ions/cm^2 at 100 keV) implanted through a screen oxide. $J_{JUNC} = 0.009$ fA/μm^2. $J_{SURF} = 0.1$ fA/μm^2.

the implanted phosphorus devices were considerably worse than the diffused control. As typified in Fig. 1(b), implanted phosphorus devices always showed a rather large tail in the leakage distribution at leakage levels above 25 pA. These devices with the higher leakage levels also exhibited softer reverse *I-V* characteristics.

TEM analysis showed a significant difference in the microstructure for arsenic- *vs* phosphorus-implanted devices. Micrographs for the phosphorus n^+ regions at two

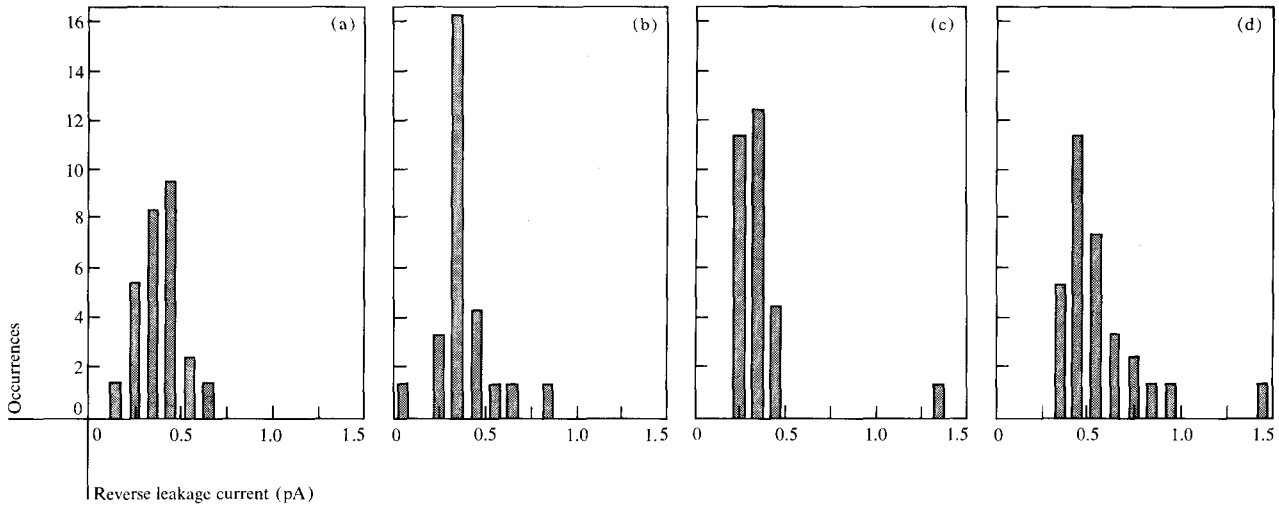


Figure 5 Histograms of reverse leakage current for implanted arsenic junctions (7×10^{15} ions/cm^2 at 250 keV). (a) 38 nm SiO_2/20 nm Si_3N_4, (b) 3 nm SiO_2/49 nm Si_3N_4, (c) 70 nm SiO_2, and (d) no screen. For all cases $V_G = -1$ V and $V_D = 10$ V.

depth ranges (0 to 0.2 and 0.7 to 0.9 μm) are shown in Fig. 2. There is a high dislocation density of type $a/2$ ⟨110⟩ throughout the entire implanted silicon volume. Similar micrographs for the arsenic-implanted devices, depicted in Fig. 3, have an overall lower defect density and a complete absence of dislocations near the metallurgical junction (0.8 to 1.0 μm). The n^+ region of the $POCl_3$-diffused control had a microstructure similar to that of the arsenic case with the addition of a low background misfit dislocation density [10]. Devices with reduced phosphorus doses (4 to 7×10^{15} ions/cm^2) had a similar defect density throughout the n^+ volume. Therefore, we attribute the resulting larger defect density for implanted phosphorus, as compared to arsenic, to the implantation process itself and not to just the differences in the lattice misfit coefficients.

Residual defects presumably caused by recoil implantation of oxygen when the primary implantation was done through a screen oxide have been observed for arsenic [12, 13] and phosphorus [14]. In the case of arsenic, the residual defect region shown in Fig. 3 was confined to within approximately 200 nm of the Si-SiO_2 interface. Preoxidation annealing of up to 60 minutes at 900 to 1100°C in an inert atmosphere did not eliminate this defect region. During the subsequent source/drain reoxidation, the residual defects coalesced and propagated both vertically and horizontally. Unlike the results observed by Natsuaki [14], the "anomalous residual defects" observed for the implanted phosphorus devices remained even after being oxidized in excess of 100 nm by a dry-wet-dry process.

On the basis of these results for implanted source/drain applications, arsenic is the preferred specie for junction depth of approximately 1 μm. The larger damaged volume for phosphorus and its propensity to getter metallic impurities [15, 16] constitute leakage yield detractors. Although the arsenic devices exhibited a residual damaged region, its extent was only about 200 nm, and it was sufficiently removed from the depletion region so as not to contribute to the bulk junction leakage. However, the near-surface region of the n^+-p junction would be detrimentally affected. Acceptable device leakage levels of 0.009 and 0.1 fA/μm^2 (0.09 and 10 nA/cm^2) for the junction and surface components are easily obtained with implanted arsenic at 100 keV, 8×10^{15} ions/cm^2 (see Fig. 4).

Implanted junctions with screens

- *Experimental procedure*

Effects of implanting through a screen material during implantation of arsenic were further investigated at a reduced junction depth. Gated diodes and IGFETs were fabricated in a manner similar to the 1-μm-deep devices described above. Four screening material cases were considered; they included 1) 38 nm SiO_2/20 nm Si_3N_4; 2) 3 nm SiO_2/49 nm Si_3N_4; 3) 70 nm SiO_2, and 4) no screen. $^{75}As^+$ was implanted at 250 keV with a dose of 7×10^{15} ions/cm^2. The high energy was selected to place virtually all the implanted arsenic in the silicon bulk and to provide a high degree of recoil implantation. After removal of the implant screen, further hot processing consisted of a drive-in anneal at 1100°C, and a source/drain reoxidation at 1000°C. Thermal conditions were selected to provide a

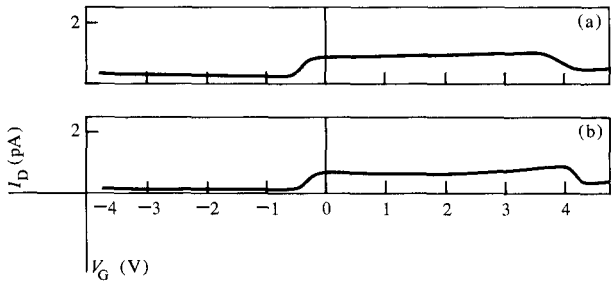


Figure 6 I_D *vs* V_G for arsenic (7×10^{15} ions/cm^2 at 250 keV) implanted into (a) bare silicon and (b) through 38-nm SiO_2/20-nm Si_3N_4 screen. For both cases $V_{SUB} = -3$ V.

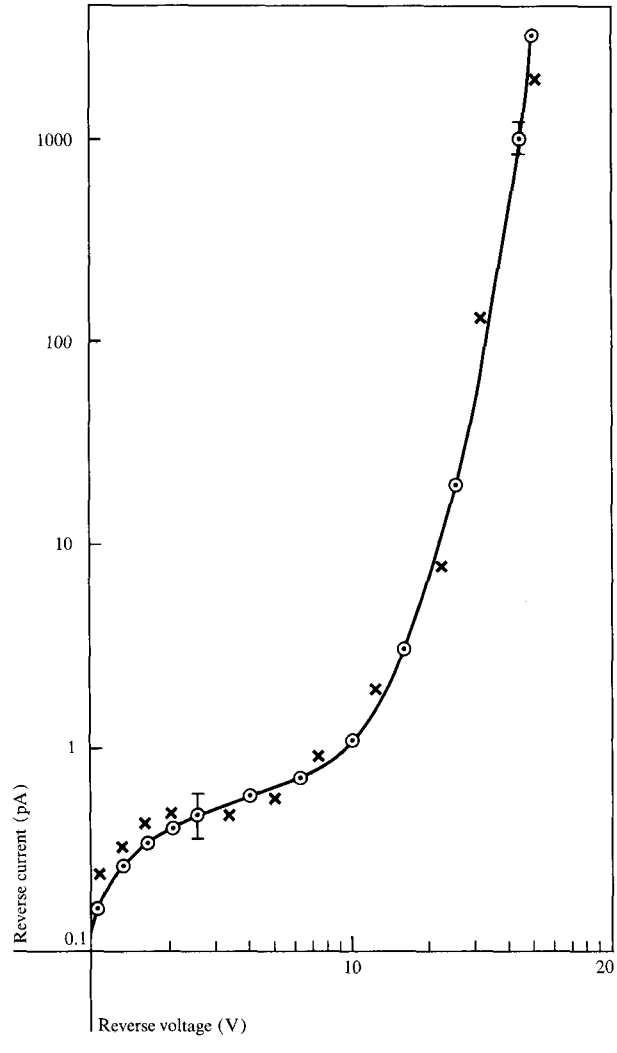


Figure 7 Reverse *I vs V* for arsenic (7×10^{15} ions/cm^2 at 250 keV) implanted into bare silicon (×) or through 38-nm SiO_2/20-nm Si_3N_4 screen (⊙).

final junction depth of approximately 0.75 μm at 10 to 20 Ω/□. As measured by spreading resistance, the resulting junctions were 0.7 μm deep with a sheet resistivity of 15.5 Ω/□.

• *Results and discussion*

Individual typical wafer histograms of reverse leakage current for the four different screen cases studied are shown in Figs. 5(a–d). Measurement conditions used for the 1.94×10^5 μm^2 gated diode device, *i.e.*, $V_G = -1$ V and $V_D = 10$ V, have the gated surface in accumulation, and therefore only the junction component was measured. The average reverse leakage currents for the 38-nm SiO_2/20-nm Si_3N_4, 3-nm SiO_2/49-nm Si_3N_4, and 70-nm SiO_2 cases were 0.435, 0.430, and 0.410 pA, respectively. An average of 0.61 pA was obtained for arsenic implanted into bare silicon. At a 95% confidence level, the differences in means for the SiO_2/Si_3N_4; Si_3N_4 (3 nm SiO_2), and SiO_2 cases were not statistically significant. The slightly higher mean for the unscreened or bare silicon case can be attributed to a higher probability of having contaminants driven into the near-surface region during the implantation process. However, the low leakage values obtained indicate this effect to be of secondary importance.

Typical Grove curves (I_D *vs* V_G) for the no-screen and 38-nm SiO_2/20-nm Si_3N_4 cases are shown in Fig. 6. The devices are virtually identical for the surface leakage component as indicated for gate potentials of 0 to 3 V. Reverse *I-V* characteristics for these two cases are shown in Fig. 7. Each data point represents the average of ten devices on the wafer at a given reverse bias. No discernible difference was found as to the sharpness of the curve or the breakdown voltage (16.5 V at 1 nA).

The electrical effects of implanting through SiO_2, Si_3N_4, and SiO_2/Si_3N_4 on the underlying junction were found to be insignificant at a junction depth of 0.7 μm. Arsenic junctions were fabricated through a screen oxide using a combined inert anneal, followed by a dry-wet-dry reoxidation. This annealing sequence has been successfully used for bipolar base formation by Seidel *et al.* [15]. These devices had leakage levels slightly better than those implanted into bare silicon. Junction and surface leakage densities as low as 0.001 fA/μm^2 (0.1 nA/cm^2) and 0.013 fA/μm^2 (1.3 nA/cm^2), respectively, were achieved. At these junction depths, it is possible to confine the residual damage to an inactive device region by proper selection of the post-implant thermal cycles.

TEM analysis of the microstructure confirmed the previous results for arsenic implanted through an SiO_2 screen. A residual defect region extending 250 nm into

the bulk was observed for SiO_2 but not for Si_3N_4 screens. Virtually defect-free recrystallization of the n region was possible using a preoxidation anneal at 1100°C in N_2 followed by the source/drain reoxidation at 1000°C.

Shallow implanted junctions

• *Experimental procedure*

In extending the results described above to an implanted junction technology suitable for VLSI applications, a few changes were necessary. Basically, with a desired junction depth of 0.25 to 0.5 μm and a corresponding IGFET design, process temperatures above 1000°C must be avoided. In addition, a single source/drain reoxidation cycle becomes desirable. The circuit requirement to keep the sheet resistance below 30 Ω/□ makes phosphorus even less desirable than before. In a standard, self-aligned, dual polysilicon gate technology, the second gate insulator is naturally in place over the source/drain regions just prior to implant. Removing this SiO_2 screen, which would be desirable from a defect viewpoint, raises a reliability concern about undercutting the second gate region adjacent to the source/drain. For junction depths of 0.4 to 0.5 μm, selection of a suitable thermal cycle should confine residual damage due to the screen to the inactive junction region. However, at 0.25 μm the above results suggest this approach would be at best marginal.

With these design considerations, various process approaches and their effects were considered, such as effects of low-*vs* high-energy-implanted arsenic, location of the maximum implant-induced damage, degree to which the crystal is rendered amorphous, stress and strain as related to the topology and films present, etc. The experimental junction technology investigated (0.4 to 0.5 μm) will now be discussed using 12-Ω-cm ⟨100⟩ silicon.

Gate insulators and polysilicon electrodes were arranged with a 45-nm SiO_2 screen oxide directly over the self-aligned source/drain regions; 80 keV was selected to place the damage peak in the screen oxide and not the bulk silicon. A dose of 8×10^{15} $^{75}As^+/cm^2$ provided a very high percentage of electrically active donors while minimizing arsenic precipitation effects. A post-implant cleaning procedure was employed without removing the screen oxide. Dry-wet-dry oxidation immediately followed at 1000°C with a controlled insert and withdrawal from the furnace hot zone. Time conditions were selected to provide annealing of the implant damage, a nominal 0.4-μm junction depth, and an adequate source/drain passivation oxide. An implant modeling design system discussed elsewhere [17] was used to numerically calculate the concentration profile as a function of depth. To extend the junction depth of 0.4 to 0.5 μm, an *in situ* inert N_2 anneal at

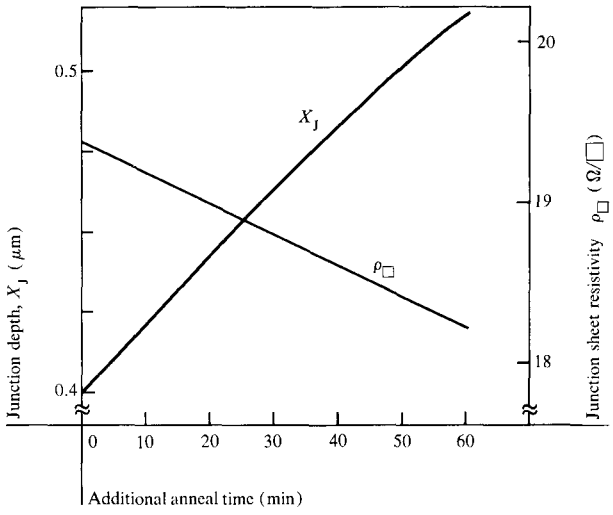


Figure 8 Junction depth and sheet resistivity as a function of post-oxidation annealing time at 1000°C N_2 (8×10^{15} $^{75}As^+/cm^2$, 80 keV, 12 Ω-cm).

1000°C was added after the reoxidation. The effect on junction depth and sheet resistivity as a function of anneal time is shown in Fig. 8. Adding 48 minutes at 1000°C gives the final junction depth of 0.5 μm and 18.44 Ω/□. Therefore, the technology can be easily tailored for a range of junction depths depending on the specific application.

• *Results and discussion*

Junctions fabricated as just described at depths of 0.4 to 0.5 μm exhibited leakage levels comparable to those obtained for the deeper junctions discussed previously. The gated diode characteristics were typical, yielding junction leakage values of 0.003 to 0.0043 fA/μm^2 (0.3 to 0.43 nA/cm^2) for 0.5-μm-deep devices. Reverse *I-V* characteristics for 0.5-μm junctions were very sharp, but naturally the breakdown voltage was a function of the acceptor concentration surrounding the device. In a dual polysilicon gate technology with semi-recessed oxide isolation and shallow junctions, the limiting breakdown factor often is the field isolation doping level. Gated thick oxide junctions typically had breakdown voltages of 17 and 21.3 V (1 nA) at field enhancement implants of 2×10^{13} and 1×10^{13} ions/cm^2, respectively. Other contributing factors are junction depth, background doping level, channel acceptor doping level, and shape of the metallurgical junction region.

Microstructural analysis illustrated the critical relationship between the annealing procedure and the ion implanter tool. Figure 9 shows TEM micrographs of (a) an adequately annealed device having a very low defect den-

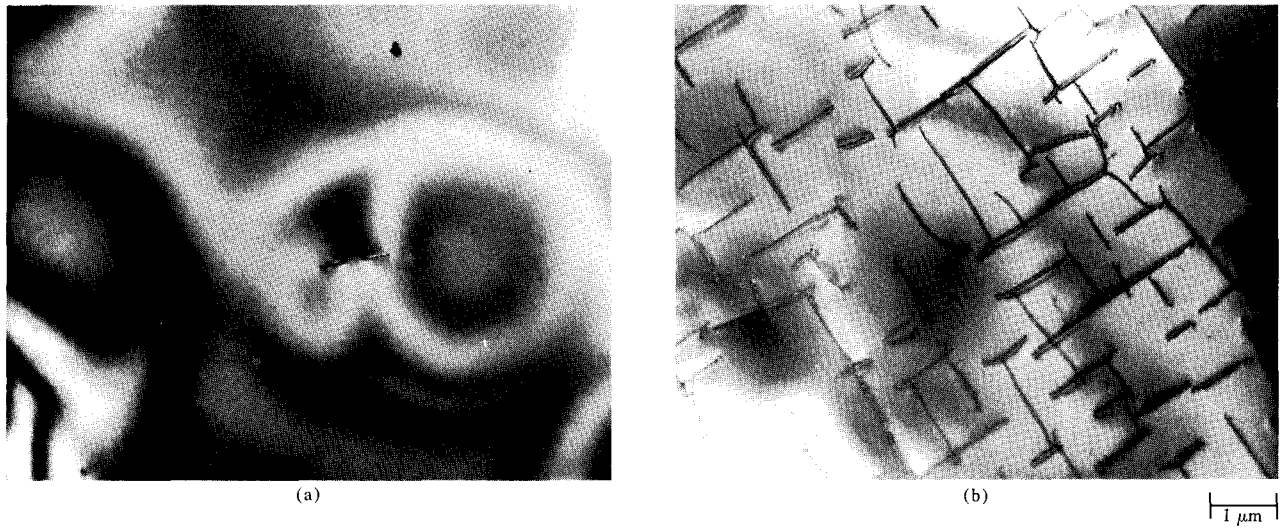


Figure 9 TEM micrographs of the resulting microstructure for (a) adequately and (b) inadequately annealed arsenic 0.5-μm implanted junctions (8×10^{15} $^{75}As^{+}/cm^2$, 80 keV, 45-nm screen).

sity, and (b) an inadequately annealed device with a correspondingly high defect density. The microstructure in Fig. 9(a) shows the result for a particular reoxidation-anneal optimized to produce a minimum defect density. Figure 9(b) shows the results of the same thermal cycle applied in a controlled manner to wafers implanted to the same conditions (80 keV; 8×10^{15} ions/cm^2) on a different tool. The ion implanter in case (b) utilized a different wafer support system and higher effective beam currents. Therefore, the selection of a reoxidation anneal cycle must be closely coupled to the particular implant tool characteristics such as beam current, wafer temperature, dosimetry technique, beam purity, etc. Further inert isothermal annealing did not dramatically alter the microstructure.

Summary and conclusions

The annealing behavior of implanted arsenic and phosphorus for n^+-p junctions suggests arsenic to be the more desirable specie. When preoxidation inert anneals for up to 60 minutes at 900 to 1100°C followed by a source/drain reoxidation were studied, arsenic devices had significantly lower junction leakage and fewer residual defects. The end of process residual defect structure for arsenic implanted through SiO_2 was in agreement with other results [12]. However, this defect network can be confined to within ≈200 nm of the silicon surface and does not contribute to the electrical behavior of the metallurgical junction.

At a reduced junction depth of 0.7 μm, the interaction of implanted arsenic through various screen combinations (SiO_2, Si_3N_4, SiO_2/Si_3N_4 and bare Si) on electrical junction characteristics was studied. Even when high energies (250 keV) were used, the effect of screening material on junction leakage and breakdown voltage was insignificant; n^+-p junctions 0.7 μm deep with 15.5 Ω/□ exhibited 16.5-V (1-nA) breakdown voltages and junction leakage levels of 0.001 fA/μm^2 (0.1 nA/cm^2).

When the junction depth decreases to the 0.5-μm range, a change in the thermal annealing cycle becomes advantageous. As with MacIver and Greenstein's [9] results for implanted BF_2 diodes, a wet oxidation cycle followed by an inert anneal can reduce the implant-induced defect density. The *in situ* N_2 anneal after source/drain reoxidation was used to adjust the junction depth from 0.4 to 0.5 μm as desired. This may be used, for example, to provide a slightly higher breakdown voltage when bootstrapping is required for special circuit applications. As with the deeper junctions, the residual change resulting from arsenic implanted through SiO_2 can be contained away from the active junction region.

The principles for minimizing end of process implant-induced damage and the consequential leakage discussed here have been applied to 0.25-μm n^+-p-implanted junctions [18]. However, at such shallow junction depths, the effects of high arsenic concentrations in the field region become significant and have parasitic device ramifications [19].

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