A. Tzou
Y. Gopalakrishna
E. Blaser
O. Bar-Gadda
R. Carballo

A 256K-Bit Charge-Coupled Device Memory

This paper describes the design of an experimental 256K-bit serial-access memory using VLSI fabrication technology and low-power dynamic circuits. The memory array chip is implemented with a double polysilicon process and uses charge-coupled devices (CCDs) grouped in 64 blocks of 4K bits each. Operation is typically at a 300-ns-per-bit cycle for both read and write modes, with operating voltages of +8.5, +5.0, and −2.2 volts, and with 310 mW of power dissipation. All inputs and outputs, with the exception of a chip enable and two system clock lines, are TTL-level compatible. The unique design features and the organization of the 256K CCD chip are discussed; the array organization, the chip layout, the peripheral circuitry, and the buried-channel CCD device design are described; and test results obtained on experimental hardware are presented.

Introduction

At the end of 1977, two 64K-bit CCD designs emerged in the industry [1, 2], both fabricated with buried-channel technology. With these designs, the computer industry was, for the first time, presented with large-scale CCD memory. Both designs operated at up to 5 MHz with standard power supplies and limited system-supplied clocks.

Up through 1976, CCD designs appeared to be continuing at the yearly doubling of bit density that began with MOS RAMs in 1968 [3]. Although in the last few years there has been a slowdown in both CCD and RAM packing density improvements from the earlier doubling rate, CCD designs still provide a considerable density advantage over RAM memories, with a CCD density factor over RAM of two to three times projected [2, 4].

Our designs for CCDs and RAMs in double polysilicon technology indicate that a CCD density factor of 2.5 times over RAM can be achieved at a cost of one extra mask [5]. This higher packing density can be achieved mainly because of the following:

1. Reduced number of sense amplifier circuits in CCD designs due to serial *vs.* random access organization.
2. Smaller CCD storage cell area, typically one-half of RAM cell area, for a common set of design ground rules.
3. Reduced number of contacts for CCD arrays, typically an order of magnitude less than RAMs.
4. Defect leakage averaging with CCD storage, not possible with RAMs.
5. Less overhead for CCDs in peripheral circuits, *i.e.*, address buffers and decoders.

An experimental 256K-bit CCD chip, intended for low-cost memory, has been designed and tested, and is the subject of this paper. The chip is organized so that it can be used in either a 256K × 1 or a 64K × 4 mode. The chip employs two levels of metal; the array portion of the chip uses both first-level polysilicon (poly 1) and second-level polysilicon (poly 2) devices, whereas the support circuit section uses primarily poly 1 devices [6].

The design incorporates several unique features. The array is designed using multiple 4K-bit serial-parallel-se-

rial (SPS) loops. The chip is partitioned with the loops forming eight octants, each having separate clock drivers to enable the usage of chips with a nonfunctional octant. An extra 4K loop is used to provide the reference charge for the sense amplifier [2], so that the reference charge tracks with the charge variation in the actual data loops, thus allowing the chip to operate over wide temperature and power supply limits and rendering the chip less sensitive to process variations.

Two additional design features used in the chip are control of the overdrive at the charge output of the 4K-bit SPS loop by using a dc voltage generator, and the use of delayed clock timing for charge transfer at the end of the output shift register to enhance charge sensing by the sense amplifier.

An additional important feature, the ability to switch to 64K × 4 mode of operation, is provided to reduce the overall chip test time.

This paper will describe the design of the 256K-bit CCD memory. In the sections following this introduction the chip organization, chip functionality, chip layout, and design of peripheral circuits will be described, including details of the chip architecture, characteristics of chip operation, and key circuits used. Following this, the array organization and the CCD design fundamentals are presented. These sections will examine the various tradeoffs in the CCD array architecture and the device characteristics of the buried-channel charge-coupled devices. Test data are given in the last section, which also contains a preliminary operating characterization of the chip as well as a close examination of leakage effects and characteristics of the 4K-bit SPS loop.

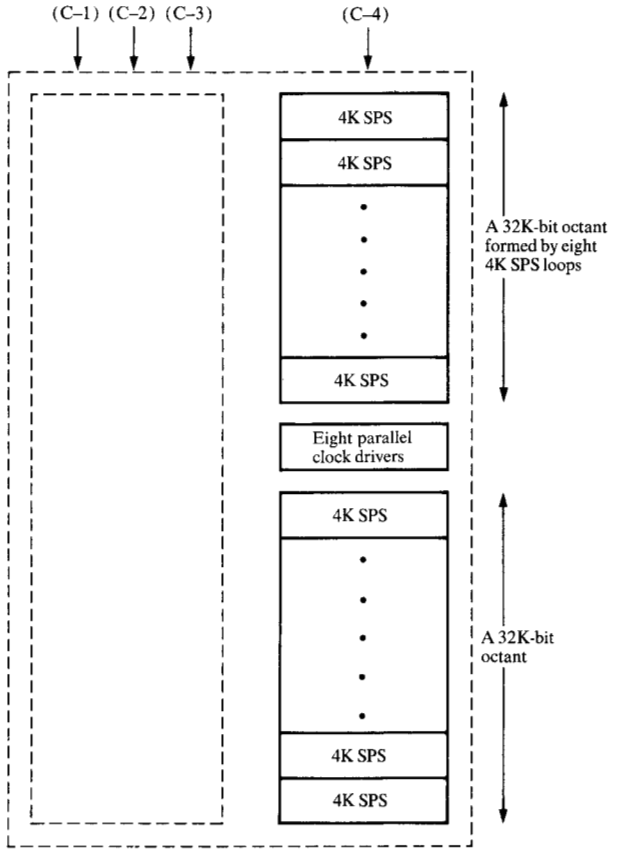


Figure 1 Organization of the 256K-bit CCD chip. Each octant is a 32K-bit array and is driven by one side of the dual-output parallel clock drivers. The four columns are indicated by C-1 to C-4.

Chip organization

The 256K-bit chip is organized as four columns of sixteen loops (Fig. 1), with each loop containing 4K (4096) bits of storage. Each column contains 64K bits of storage and is divided into two halves or octants of 32K bits each by a strip of eight parallel clock pre-drivers. The pre-drivers provide the clock signal to the parallel clock drivers of the array, and each driver has a separate output to the top and to the bottom of each column. This arrangement is used to ensure that if a problem exists in the top half of a column the bottom half will still function. This organization provides eight separate octants of 32K bits of memory on the chip and reduces the loading on each parallel clock driver. This enhances performance and also reduces any coupling which could otherwise cause charge to be lost or transferred prematurely. In addition, this arrangement isolates the eight octants so that if there are any problems in one octant (*e.g.*, shorts between first and second polysilicon gates) the other octants will not be affected. This allows the usage of fractionally good chips such as one-quarter, one-half, three-quarters, or seven-eighths.

Separate data-in and data-out buffers are used for each column, thereby allowing the chip to be tested in a 64K × 4 mode in order to reduce test time. Also, applications which require a 64K × 4 organization, rather than 256K × 1, can make use of the chip in this manner.

Functionality description

For the 64K × 4 organization, there will be a total of 24 active chip input/output (I/O) connections (Fig. 2). These include the four power supply connections of V_{DD}, V_{CC}, V_{SX}, and V_{SS} (GND). All inputs except *chip enable* (*CE*) and the two *system clocks* (ϕ_1 and ϕ_2) required to operate the chip are TTL-compatible. All support circuit timing signals, namely the read and write timing clocks, are gen-

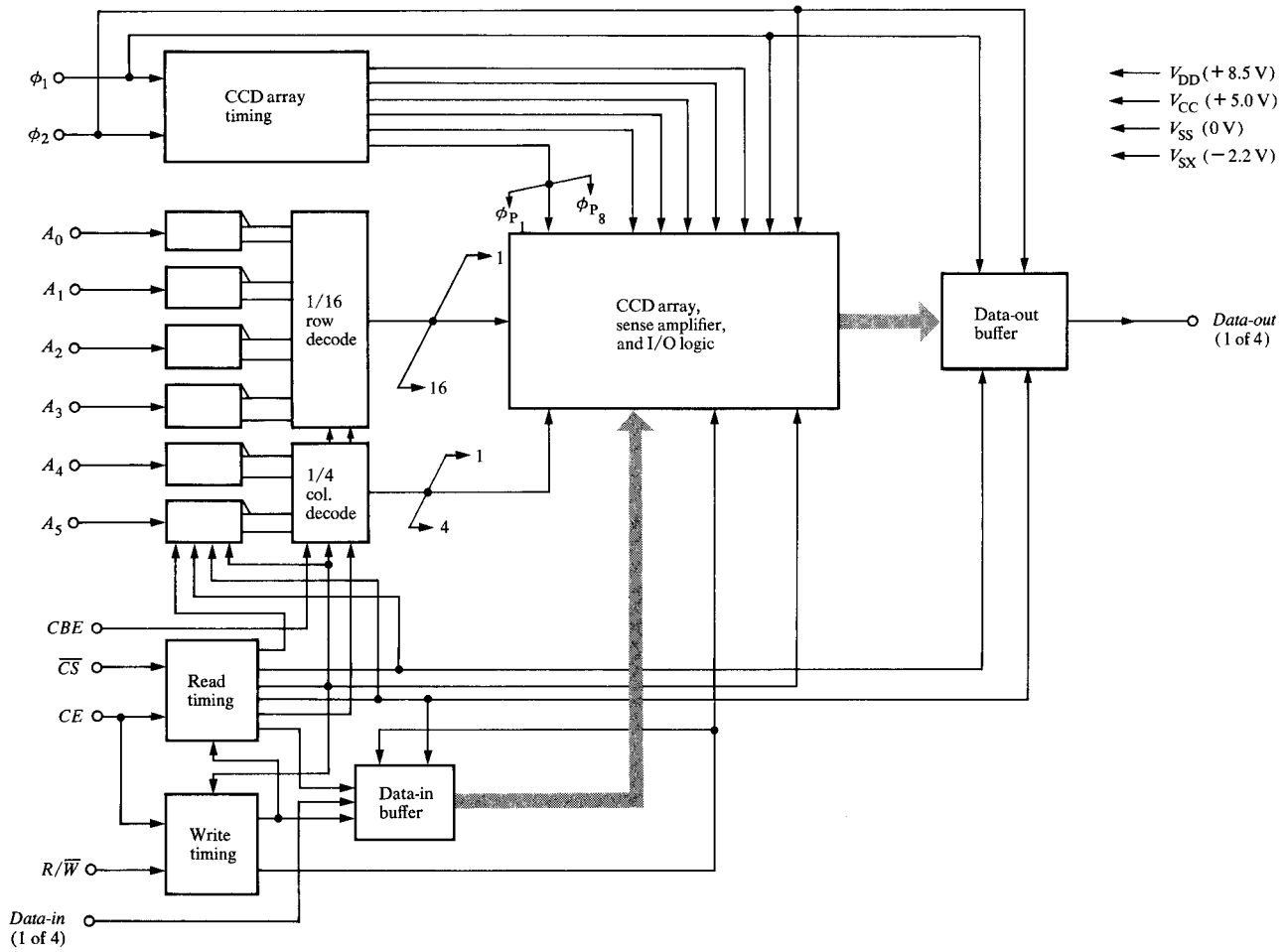


Figure 2 Functional block diagram of the 64K × 4 CCD memory chip.

erated on chip by using the *CE* and $R/\overline{W}$ inputs. The CCD array timing is also generated on chip by using the ϕ_1 and ϕ_2 clocks. The ϕ_1 and ϕ_2 signals are nonoverlapping clocks, which together with *CE* provide the base timing for the entire chip logic.

The chip can be operated in *read, write*, or *recirculate* modes. When the chip enable signal is deactivated (low, or down, state) no read or write operation is allowed; in this condition the chip is in the *recirculate* mode.

The *chip select* signal ($\overline{CS}$) enables both the data-in and data-out circuits when it is deactivated. To select the chip, $\overline{CS}$ must be deactivated before the activation of the *CE* input. To select a read or a write operation, the $R/\overline{W}$ input is used and must be timed appropriately with the *CE* signal and the input address bits.

A unique feature is the *column block enable* control (*CBE*), which is used to reduce the overall chip testing time. The *CBE* pin is either tied to V_{DD} or to ground, at the module level, to select the appropriate chip organization. When *CBE* is set high, four 4K SPS loops corresponding to a given row address are enabled. The four data-input and data-output buffers are logically isolated for this condition and data can be written or read four bits at a time; thus, the chip functions in the 64K × 4 mode. When *CBE* is set at ground level, the chip operates in the 256K × 1 mode, in which case the four data inputs and outputs can be shorted together.

Chip layout and peripheral circuits

• *Chip layout*

The chip is laid out by using a set of 2.0-μm minimum-feature-size photolithographic design rules. In order to simplify fabrication of engineering parts, this design was scaled up by a factor of 1.2 to 2.4 μm. The chip uses a total of 11 mask levels and has an active area of 43 mm^2, of which 70% is array.

• *Peripheral circuits*

Sense amplifier

The sense amplifier is a three-stage, balanced, cross-coupled latch. The first stage is a pre-latch which is set by the CCD input from the 4K loop and also by the reference generator. The function of the pre-latch is to prevent the CCD output node from discharging. To bring any CCD output node to V_{SS} would cause errors in the array, since the node could act as a source, allowing charge to transfer back into the last storage location in the array. This problem is overcome by the pre-latch; however, the small gain of such a latch and the small charge levels that are detected are insufficient to achieve the necessary chip voltage levels. Therefore, the pre-latch is followed by an amplifier and transfer stage which provides additional amplification as well as isolation between the pre-latch and the final latch to prevent signal mixing. This is necessary because one bit is entering the sense amplifier at the same time the previous one is being gated out; therefore, the bits must be isolated between these stages. The final latch stage gives some more amplification and standardizes the outputs to acceptable MOS signal levels.

Input/output decoding, write, and recirculate circuits

The basic block decoder circuit, which functions as the row decoder, is shown in Fig. 3. This decoder, in conjunction with the column decoder, selects the particular block that is to be addressed. The data reading and writing scheme utilized is illustrated in Fig. 4. When data are recirculating, the read/write clocks and the address bits will not be active and the data will pass through the circuit to the CCD input. In order to write data, a block selection is made by the address bits and the ϕ_{W2} (write) clock. The information on the *data-in* node is then presented to the gate of the device that drives the CCD input. During the ϕ_2 clock time, the information is gated to the CCD input circuit (launcher). In order to read data, the address bits allow the information coming from the sense amplifier to be presented to the *data-out* bus as the complement of the data from the sense amplifier.

Parallel clock generator

The parallel clock timings are derived from a clock generator containing a divide-by-32 counter which provides the input to the parallel clock decoders and drivers. All circuits are synchronized with the ϕ_1 and ϕ_2 clocks to eliminate clock skews between the serial and parallel section. Each eight-phase parallel clock runs at 1/32 of the system clock frequency, and stays active for two cycles and inactive for thirty cycles of the main clocks.

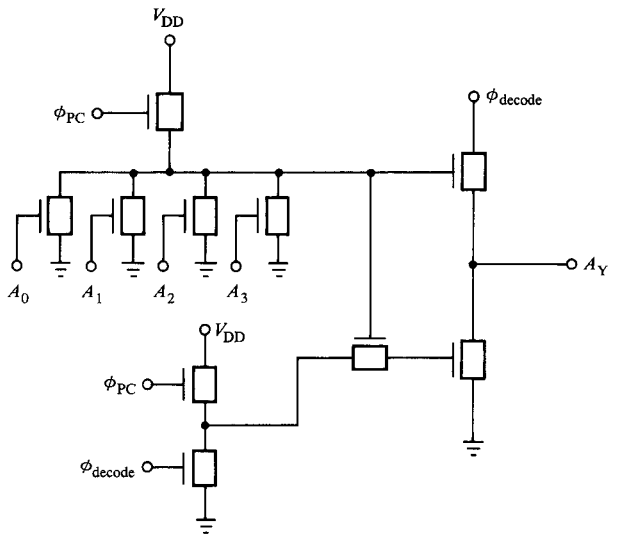


Figure 3 Basic block decoder circuit.

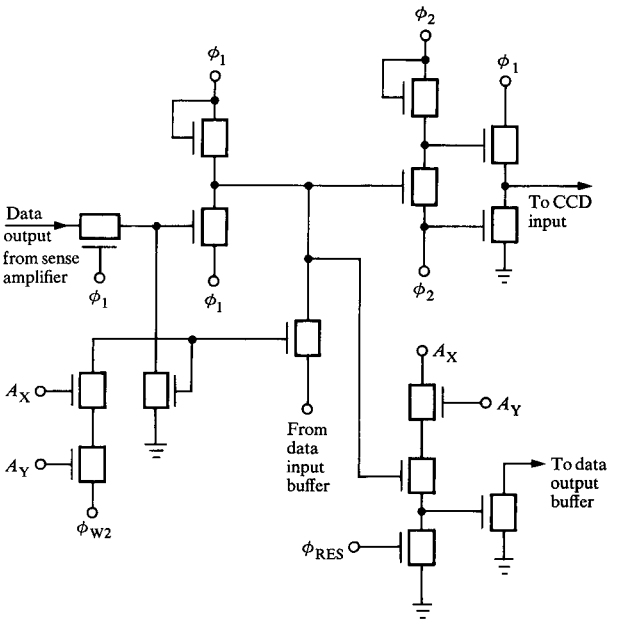


Figure 4 Data read and write circuit.

Array organization

The CCD array consists of 64 4K-bit SPS loops, in which the 4K loop organization formed is based on the latency of the loop operation, which is the average time to locate a particular bit in a given loop and is dependent on the mode of system operation. Furthermore, the maximum number of bits in a loop is a function of the maximum allowable latency. At a given frequency, the larger the loop size the longer the latency, and thus the greater the process and package constraints.

In addition, other performance considerations must be included in structuring the loop organization. The loop

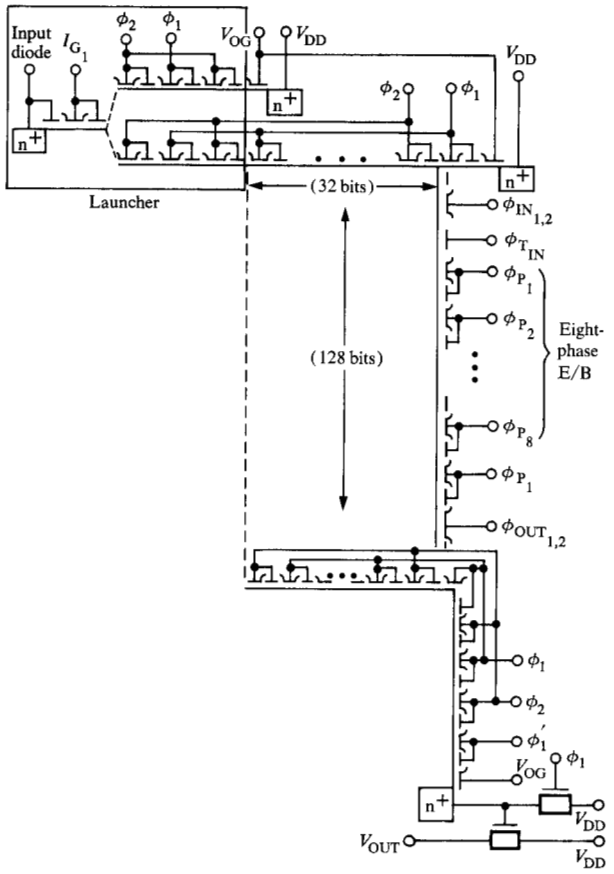


Figure 5 Circuit schematic of the 4K SPS CCD loop, including the launcher.

Table 1 Dependence of total loop area A_T on 4K SPS loop organization.

Array organization	*16 × 256*	*32 × 128*	*64 × 64*
No. of serial bits	16	32	64
Total loop area A_T (mm^2)	18.5	19.2	20.4

Table 2 Dependence of 256K CCD chip area on 4K SPS loop organization.

Array organization	*16 × 256*	*32 × 128*	*64 × 64*
No. of serial bits	16	32	64
Total chip area (mm^2)	24.1	22.7	23.0

Table 3 Dependence of on-chip and external-to-chip power dissipations on 4K SPS loop organization.

Array organization	*16 × 256*	*32 × 128*	*64 × 64*
No. of serial bits	16	32	64
Power (mW): Serial register (off-chip)	120	240	480
Power (mW): Parallel register (on-chip)	600	300	150

organization of 32 × 128 that was selected was chosen on the basis of optimum chip area (Tables 1 and 2), power dissipation on and off the chip (Table 3), and the number of charge transfers. This organization provides approximately equal on-chip and off-chip driver power, making the power dissipation uniform within the package.

With this organization there are 32 cells in each of the serial registers (input and output) of the interlaced 4K SPS loop. The 32-cell length of the serial registers lends itself to a practical geometry for the sense-amplifier and I/O circuits placed beside an SPS loop, thereby minimizing the array area for an efficient layout. There is one sense amplifier and I/O data control logic circuit for each 4K SPS loop. The 64 (16 × 4) SPS loops are organized on the chip as 16 high and 4 wide. An off-chip driver driving 32 serial cells in a loop drives the load of the 64 × 64 organization, resulting in faster rise and fall times for the high-frequency operation. The 32 × 128 organization allows efficient timing generation for the eight-phase clocks of the parallel section of the SPS loop. The circuit schematic of the 32 × 128 interlaced SPS loop is given in Fig. 5.

Additional density improvement is achieved by electrode-per-bit (E/B) operation [7] in the parallel section. In the E/B operation, there are n cells driven by n clocks and the information (bit) is stored in $(n - 1)$ cells with one cell empty. The number of cells required in a 32 × 128 organization is $128 \times [n/(n-1)]$ and decreases with increasing number of clocks. The 8/7 value for $n/(n-1)$ gives the best tradeoff for E/B operation considering the timing, the loop area, and the chip real estate to generate and distribute the clocks for the 32 × 128 organization.

Buried-channel CCD design

Certain key CCD design features will be described in this section. These features include 1) the CCD device description, 2) the definitions of buried-channel CCD device design, 3) the poly 1 design criterion, 4) cell charge capacity, and 5) charge transfer efficiency (CTE) and signal swing at the end of the array.

- *CCD device*

The CCD cell is shown in Fig. 6(a). The cell has a dimension of 8.9 × 8.9 μm^2 in the scaled-up design. This is

achieved by using a blockout mask and processing with a unique blockout scheme in the double polysilicon process. There is no contact hole used in the cell, except at the input and output shift registers, and near the extreme edges of the array where contact holes have been shared by a group of eight 4K SPS loops. The poly 1 gate is used for charge storage, and the poly 2 gate is used as a transfer electrode which also serves as a barrier between adjacent charge storage wells. The buried-channel ion implant (blanket n-doping) sets the poly 1 well potential, and the barrier ion-implant (p-doping under poly 2 only) defines the poly 2 barrier potential. In Fig. 6(b), the potential levels V_{M2} and V_{M1} represent the rest channel potentials, under poly 1 and poly 2 respectively, for the applied gate voltage inactive ($V_G = V_{GL}$). The channel potentials of V_{M4} and V_{M3} with the gate voltage active ($V_G = V_{GH}$) on poly 1 and poly 2 gates are also shown in Fig. 6(c), which illustrates the case when a charge transfer is taking place.

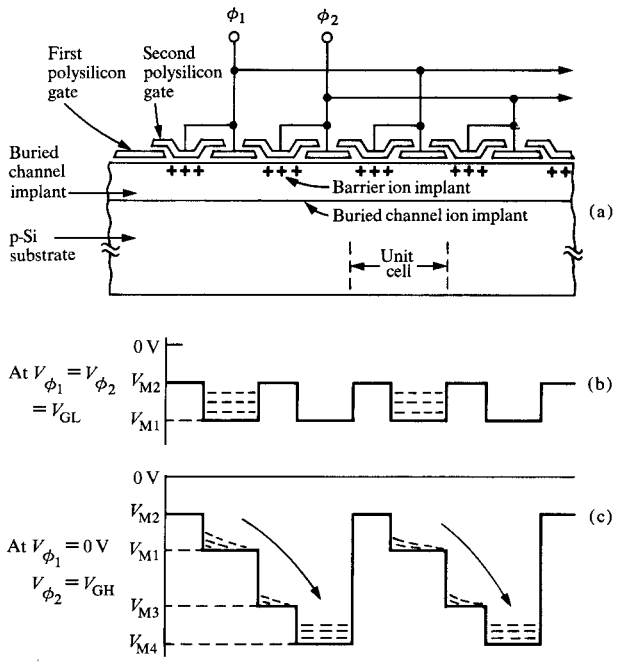


Figure 6 Channel potentials for the buried-channel CCD: (a) a CCD cell and a two-phase linear shift register; (b) the rest potentials V_{M1} and V_{M2} at $V_G = V_{GL}$; and (c) the active potentials at $V_G = V_{GH}$.

- *Buried-channel device design*

Buried-channel CCD device design demands a knowledge of the channel potential as a function of process variables and circuit design constraints. A fundamental design curve is the channel potential V_M *vs.* gate voltage V_G [8]. This curve is obtained by solving Poisson's equation. Several techniques are available to do so [9, 10], but an approximate analytical approach will be used here to demonstrate the design methodology. Figure 7 shows the doping and potential profiles. The nonuniform doping profile has been approximated by a staircase profile, where the channel layer has an effective doping N_D and an effective depth $2x_g$, where

$$N_D = \frac{Q_N}{2x_g},$$

$$Q_N = \int_0^{x_\ell} N(x)dx = \text{the effective channel layer dose,}$$

x_ℓ = the junction depth, and

$$x_g = \frac{\int_0^{x_\ell} xN(x)dx}{Q_N}$$

= the centroid of the channel layer doping.

Using this approximation and the depletion approximation, Poisson's equation can be solved in closed form. The results are as follows:

$$V_M = V_G - V_{FB} - V_{BI} + \frac{qN_Dx_1^2}{2\epsilon_{Si}} + \frac{qN_Dx_1t_{ox}}{\epsilon_{ox}}, \qquad (1)$$

where

V_{FB} = the flatband voltage (for a uniform p-Si substrate),
V_{BI} = the built-in p-n junction voltage,

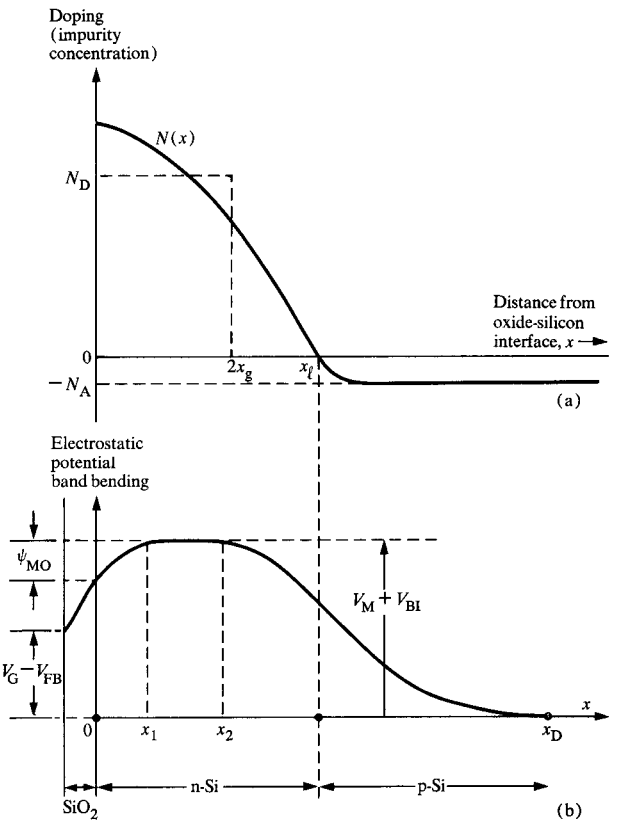
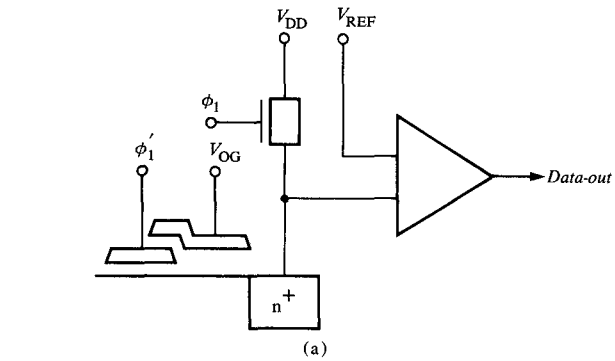


Figure 7 (a) Doping and (b) potential profiles.



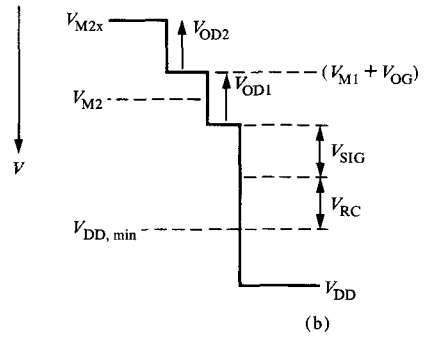


Figure 8 Sense node design specifications: (a) sense node circuit; (b) voltage specifications of the sense node.

q = the electronic charge,
ϵ_{Si} = the dielectric permittivity of the silicon,
ϵ_{ox} = the dielectric permittivity of the oxide,
t_{ox} = the oxide thickness,

and

$$x_D = (b^2 + c)^{1/2} - b,$$

$$x_2 = \frac{Q_N - N_A x_D}{N_D},$$

$$x_1 = x_2 - \frac{Q_{CH}}{qN_D},$$

where

$$b = x_\ell + \frac{\epsilon_{Si}}{\epsilon_{ox}} t_{ox} - \frac{Q_{CH}}{qN_D},$$

$$c = \frac{2\epsilon_{Si}(V_G - V_{sx} - V_{FB})}{qN_A} + \frac{Q_N^2}{N_D N_A}\left(\frac{2\epsilon_{Si} N_D t_{ox}}{\epsilon_{ox} Q_N} + 1 - \frac{Q_{CH}}{qQ_N}\right)\left(1 - \frac{Q_{CH}}{qQ_N}\right),$$

and Q_{CH} = the total charge per unit area in the channel. These equations approximate the channel potential as a function of gate voltage, channel charge, oxide thickness, substrate doping, and channel layer doping. Numerical solution of the exact Poisson equation can be used for fine tuning of these parameters. One can then obtain the rest potentials (V_{M1} and V_{M2}) and the transfer potentials (V_{M3} and V_{M4}) by using Eq. (1), with $Q_{CH} = 0$ and appropriate process parameters for the well and barrier.

These, in turn, specify the following:

barrier height = $\Delta V_{M,L} = V_{M1} - V_{M2}$, and

overdrive = $\Delta V_{M,OV} = V_{M3} - V_{M1}$.

The storage charge capacity is determined by the condition $V_{M,well} > V_{M,barrier}$. The maximum channel charge is therefore given by

$$V_{M,well}(V_{GL}, Q_{CH,max}) = V_{M2}. \quad (2)$$

Using Eqs. (1) and (2) one can calculate $Q_{CH,max}$.

For a given drive voltage, selection of the barrier height determines the charge storage capacity and overdrive. There is a tradeoff between barrier height and overdrive; high overdrive gives faster transfer speed at the cost of lower charge capacity. The choice of the channel potential and storage capacity is constrained by sense amplifier requirements on minimum senseable charge and maximum senseable potential. The overdrive is constrained by the maximum clocking frequency.

In addition to the foregoing circuit design constraints, there are also layout constraints. Since the array constitutes a large portion of the chip area, one seeks to minimize the cell dimensions. Doing so will affect all the design variables previously discussed; in particular, narrowing the channel width reduces the channel potential and charge capacity [11]. When

$$W_{eff} \lesssim 2\left(x_D + \frac{\epsilon_{Si}}{\epsilon_{ox}} t_{ox}\right),$$

two-dimensional effects will decrease the potentials. Tables 4 and 5 show the results of a numerical simulation performed for this structure using a computer program. Table 4 shows the charge capacity per unit area dependence on barrier height, and Table 5 indicates the potential lowering as a function of width. Comparison of the one-dimensional (1-D) and two-dimensional (2-D) data shows that narrow-width devices have a charge capacity 60–70% of that expected for an infinite-width device.

- *Poly 1 design criterion*

The criterion for the poly 1 potential well is determined by the following relationships (sense node design specifications are given in Fig. 8.):

$$V_{M1} = V_{M1x} - V_{L,\Phi 1'}, \quad (3)$$

$$V_{M1} \lesssim V_{M2} + V_{OG} - V_{OD2}, \text{ and} \quad (4)$$

Table 4 Dependence of charge capacity density Q_{CH} on barrier height ΔV_M. (Modeled and measured under following conditions: $V_G = 0$, $V_{SX} = -2.2$ V, $T = 25°C$.)

ΔV_M (V)	2.0	3.6	5.5
Q_{CH}, 1-D, calculated (fC/μm^2)	0.57	1.13	1.98
Q_{CH}, 2-D, calculated (fC/μm^2)	0.30	0.70	1.48
Q_{CH}, measured (fC/μm^2)	0.30	0.75	1.38

Table 5 Dependence of channel potential V_M on effective device width W_{EFF}, for the first polysilicon gate device. (Same conditions as listed in Table 4.)

W_{EFF}, 2-D (μm)	4	5	6	7	∞ (or 1-D)
V_M (V)	5.1	5.8	6.3	6.7	7.0

$$V_{M2} + V_{OG} \leq V_{DD,min} - V_{RC} - V_{SIG} - V_{OD1}, \quad (5)$$

where

V_{M1} = rest potential of the poly 1 gate,
V_{M1x} = rest potential of the last storage gate of the SPS loop driven by the ϕ_1' clock,
V_{OG} = gate voltage (dc) on the poly 2 gate,
$V_{L,\phi 1'}$ = Lowest gate voltage of ϕ_1' (below ground) (*i.e.*, $V_{SX,min}$ approximately),
$V_{DD,min}$ = minimum power supply voltage,
V_{RC} = voltage coupling to the sense node when the precharge device turns off,
V_{SIG} = signal swing due to charge on the sense node,
V_{OD1} = overdrive from the V_{OG} output transfer gate to the sense node,
V_{M2} = rest potential of the poly 2 gate, and
V_{OD2} = overdrive from the last poly 1 gate to the poly 2 V_{OG} gate.

The poly 2 channel potential is determined by the charge capacity of the CCD cell. The charge capacity of the CCD cell as a function of the barrier height has been tabulated in Table 4 for the one- and two-dimensional analyses. The dc voltage V_{OG}, applied to the last poly 2 transfer gate before the sense node, is chosen to satisfy Eq. (5).

There are two sense nodes in the sense amplifier. The one facing the 4K SPS is to be precharged to the V_{DD} level at each clock cycle, whereas the reference sense node is to be precharged to V_{REF} at the same time. The V_{REF} level is defined at the midpoint of the signal charge swing, and is provided by a V_{REF} generator which utilizes a reference charge from a dummy 4K SPS loop [2]. This reference

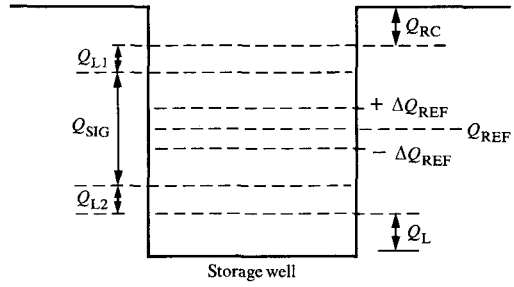


Figure 9 Charge capacity and signal charge specifications, in which:
Q_{L1} = leading-edge CTE charge loss,
Q_{L2} = trailing-edge CTE charge loss,
Q_{SIG} = signal charge,
Q_{RC} = charge loss due to coupling,
Q_{REF} = reference charge = 1/2 Q_{IN},
ΔQ_{REF} = tolerance of the reference charge, and
Q_L = charge loss due to leakage.

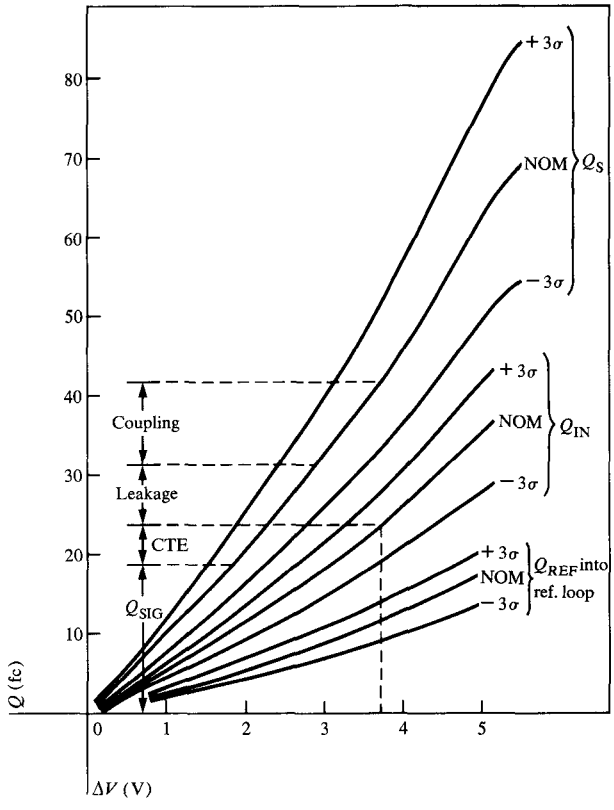


Figure 10 Charge storage Q_S, launched charges of Q_{IN}, and Q_{REF} *vs.* barrier height ΔV, based on a one-dimensional model.

charge is one-half the signal charge by way of input charge metering, and undergoes an identical leakage mechanism as the signal charge. Therefore, the reference and the signal charges track with each other, compensating for average process and temperature variations.

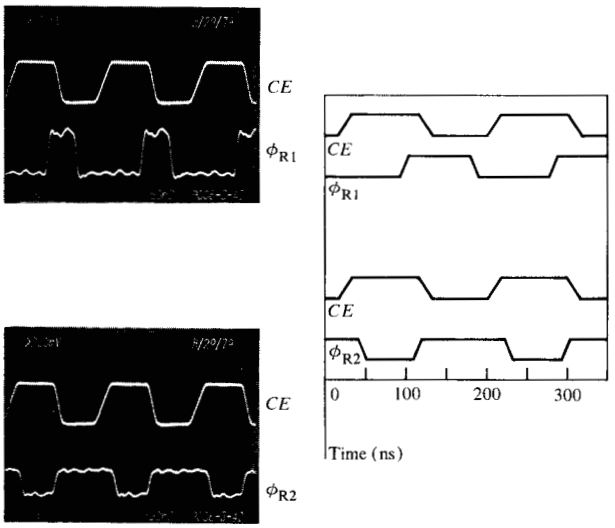


Figure 11 The two primary read clock pulses of ϕ_{R1} and ϕ_{R2}: (a) measured *vs.* (b) simulated waveforms.

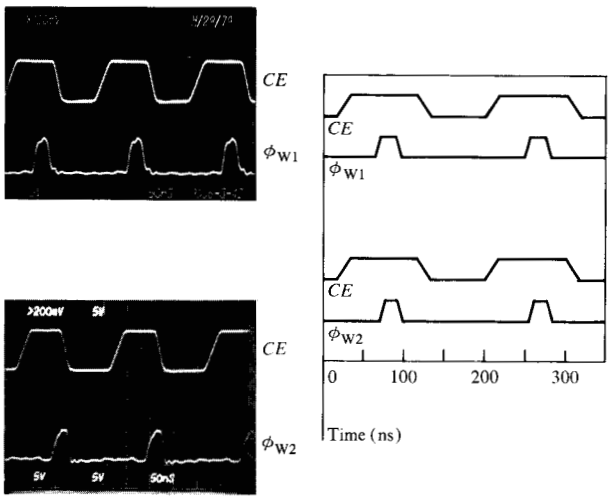


Figure 12 The two primary write clock pulses of ϕ_{W1} and ϕ_{W2}: (a) measured *vs.* (b) simulated waveforms.

• *Cell charge capacity*

Figure 9 defines the charge capacity and signal charge parameters corresponding to the buried-channel CCD. The stored charge capacity takes into account four main factors: coupling, leakage, charge transfer efficiency (CTE), and signal charge.

The worst-case coupling is due to voltage coupling of one clock phase to an adjacent clock phase in the parallel section of the array for the condition of minimum storage capacity. The serial section CCD cells are designed to have a larger storage area, resulting in larger storage capacity, and hence are less sensitive to charge loss due to coupling. However, this has to be carefully balanced against the charge input to minimize rise and fall time penalties.

The leakage, or dark, current is a function of the temperature and lowest operating frequency of the loop, and is allowed to be up to 20% of well capacity.

• *Charge transfer efficiency and signal swing*

The charge transfer efficiency (CTE) is given by $Q = Q_{IN}(1 - \alpha)^n \approx Q_{IN}(1 - n\alpha)$ for small α, where

Q_{IN} = charge input to the SPS loop,
n = number of shifts through the SPS loop, and
α = fractional charge loss per shift.

The effective signal at the sense node is $Q_{OUT} = Q_{IN}(1 - 2n\alpha)$. The loss in the leading *one* and the gain in the trailing *zero* reduce the net signal handling capacity by 20% due to CTE loss (see Fig. 10). For a 4K loop organization, the fewer the total number of shifts, the smaller the transfer loss (Table 6), especially in the serial registers.

The net charge coming out of the 4K SPS loop is transferred to a precharged sense node. The sense-node capacitance C_{SN} is minimized to obtain the maximum sense-signal swing V_{SIG},

$$V_{SIG} = \frac{Q_{OUT}}{C_{SN}} \approx 400 \text{ mV}.$$

The CCD loop and the senseable output charge are designed (Fig. 10) to operate at higher temperatures and at 3σ device limits.

Test results

The 256K CCD chip has been tested for peripheral circuits, the chip functionality, and the array. The peripheral circuits consist of four major groups, namely the read, write, and CCD timing chains, plus the I/O control circuits. For the array testing, a comprehensive characterization has been performed for the 4K SPS loop which is used in the 256K CCD array.

The read-timing chain provides ϕ_{R1} and ϕ_{R2} clocks, which in turn control the address input and the data output buffers. The inputs to the chain are *CE* and $\overline{CS}$. The measured data and the computer-simulated waveforms are shown in Fig. 11.

The write-timing chain generates ϕ_{W1} and ϕ_{W2}, which together with the address timing drive the I/O logic circuits. *CE* and $R/\overline{W}$ are the inputs for the chain. When *CE*

Table 6 Dependence of charge transfer efficiency on 4K loop organization.

Array organization	*64 × 64*	*32 × 128*	*16 × 256*
Total no. of shifts in the 4K loop	145	186	316
Charge transfer efficiency (%)	86.0	82.5	69.0

Table 7 Typical output charge leakage dependence on temperature for the 4K SPS loop, at 1 MHz frequency, and with V_{clock} = 8.5 V and V_{SX} = −2.2 V.

Temperature (°C)	*40*	*45*	*55*	*64*	*73*	*82*
Typical output charge leakage (fC)	0.12	0.20	0.39	0.82	1.55	3.00

is activated and $R/\overline{W}$ deactivated, data are written in the assigned 4K loop. Figure 12 shows the measured data and the computer-simulated waveforms of both output pulses, ϕ_{W1} and ϕ_{W2}, respectively.

The data output is shown in Fig. 13, in which the $R/\overline{W}$ timing has been extended for a period of five 4096-bit cycles of read time. From these data it is clear that the same information is recirculated during the extra read cycles and comes out at the data output buffer. The eight parallel clocks are shown in Fig. 14, in which each clock must remain activated for two cycles and deactivated for 30 cycles of the main clock.

The CTE data of the 4K-bit loop are shown in Fig. 15 as a function of the number of zeros. The test was done at a clock frequency of 5 MHz and at nominal dc voltage conditions. A charge packet size of 15 to 20 fC is normally measured at the output of the SPS. The leakage current for the SPS loop is given in Table 7. This measurement was performed by writing empty charge packets at a clock frequency of 1 MHz. The data indicate that the leakage builds up to an average level of 1 fC at 65°C and its level doubles for every 8.5°C.

Summary

A 256-bit CCD memory chip has been designed which uses buried-channel CCD technology for both yield and performance enhancements. The chip operation and characteristics have been described, and test results obtained on experimental hardware have been demonstrated.

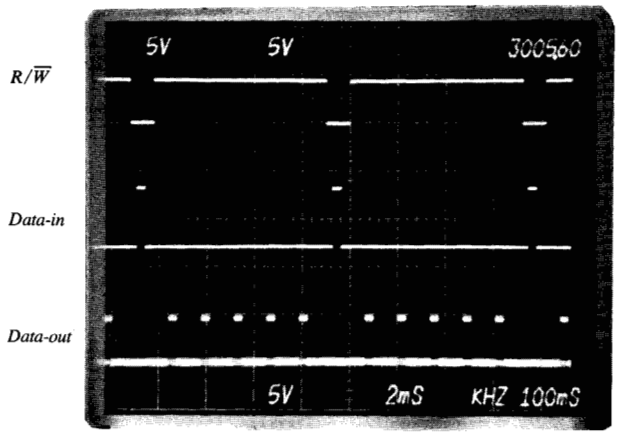


Figure 13 Data output under the conditions of extended read in five 4096-bit cycles, with nominal applied voltage conditions and frequency equal to 3 MHz.

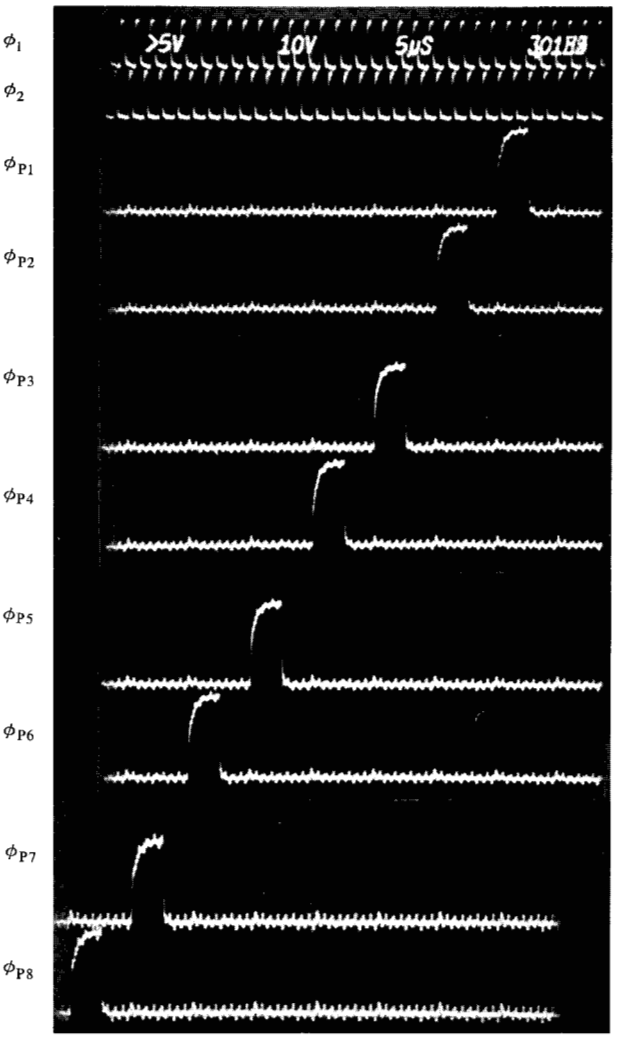


Figure 14 The eight parallel clocks for the 4K SPS array, with nominal applied voltage conditions.

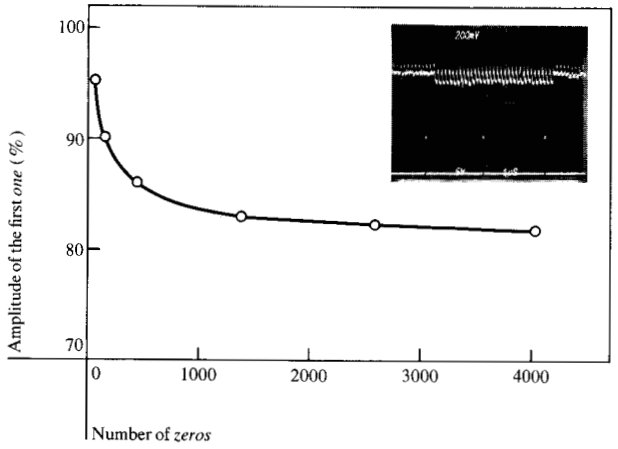


Figure 15 The CTE of the 4K SPS loop. The data show a typical output of 32 *zeros* followed by 32 *ones*, measured at 5 MHz.

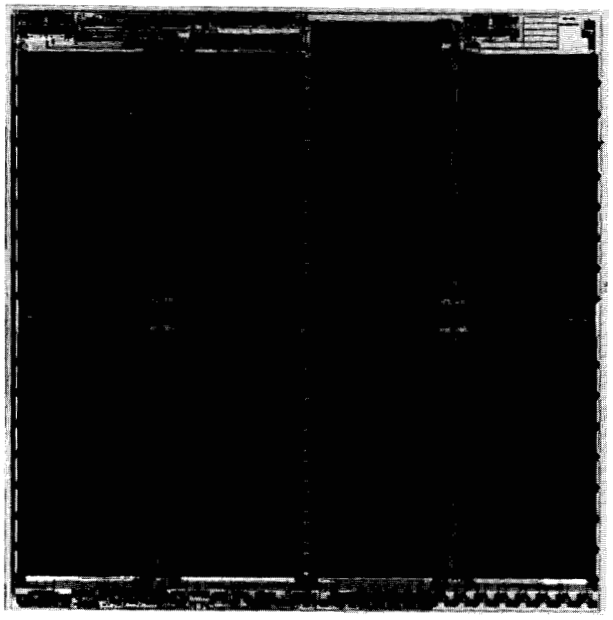


Figure 16 Photomicrograph of the 64K × 4 CCD memory chip.

A photomicrograph of the chip is shown in Fig. 16. Power consumption is minimized by the use of dynamic logic for the peripheral circuits, and chip testing time has been reduced by the use of the column block enable feature. The array area has been reduced to less than 30 mm^2 through interlacing of the data and by using an 87.5% electrode-per-bit technique in the 4K SPS octants.

Applications for CCDs were originally viewed as being in direct competition with dynamic RAMs. As familiarity with the design grows, many cost-effective new applications are seen, including the benefits of RAM and CCD combinations.

Acknowledgments

The authors thank J. A. Palmieri for management support and technical discussions, and M. Ghafghaichi for support and review of this work. We are especially grateful for technical consultations, during the early phase of the project, from L. M. Terman and from H. S. Lee and L. G. Heller.

References

1. "F464, 65 536 × 1 Dynamic Serial Memory—Fairchild Charge-Coupled Device," *Data Sheet* (August 1977); R. C. Varshney and K. Venkataswaran, "A Block-Organized 64K-Bit CCD Memory," *IEEE J. Solid-State Circuits* **SC-13,** 681 (1978).
2. J. B. Barton, A. F. Tasch, Jr., and T. E. Hasty, "A Cost-Effective 64K CCD Memory," *Electo '77, Professional Program Proceedings, Section 13, CCD Memories: The Take-Off Year*, New York, April 13-21, 1977, Session 19/1, p. 1.
3. L. M. Terman and L. G. Heller, "Overview of CCD Memory," *IEEE Trans. Electron Devices* **ED-23,** 72 (1976).
4. J. E. Carnes, W. F. Kosonocky, and D. J. Sauer, "Fundamental Packing Density Limitations of CCD and RAM Memory," *Electo '77, Professional Program Proceedings, Section 13, CCD Memories: The Take-Off Year*, New York, April 13-21, 1977, Session 19/4, p. 1.
5. T. C. Lo, R. E. Scheuerlein, and R. Tamlyn, "A 64K FET Dynamic Random Access Memory: Design Considerations and Description," *IBM J. Res. Develop.* **24,** 318-327 (1980, this issue).
6. A. M. Mohsen and T. F. Retajczyk, Jr., "Fabrication and Performance of Offset-Mask Charge-Coupled Devices," *IEEE J. Solid-State Circuits* **SC-11,** 180 (1976).
7. "Electrode-per-bit Clocking," *Charge-Coupled Devices and Systems*, M. J. Howes and D. V. Morgan, Eds., John Wiley & Sons, Inc., New York, 1979, p. 201.
8. Carlo H. Séquin and Michael F. Tompsett, "Charge Transfer Devices," *Advances in Electronics and Electron Physics, Supplement 8*, Academic Press, Inc., New York, 1975, p. 10.
9. W. H. Kent, "Charge Distribution in Buried-Channel Charge-Coupled Devices," *Bell Syst. Tech. J.* **52,** 1009 (1973).
10. H. El-Sissi and R. S. C. Cobbold, "One-Dimensional Study of Buried-Channel Charge-Coupled Devices," *IEEE Trans. Electron Devices* **ED-21,** 437 (1974).
11. K. Venkataswaran, "Effects of Channel Potential Modulation in Narrow Channel CCD Shift Registers," *IEDM Tech. Digest*, 620-623 (1978).

Received May 17, 1979; revised December 12, 1979

The authors are located at the IBM Data Systems Division laboratory, East Fishkill (Hopewell Junction), New York 12533.