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Reduction of Leakage by Implantation Gettering in VLSI Circuits

Damage introduced by ion implantation on the back side of the wafer is used to reduce the MOS transient (relaxation) and junction leakage; the technique is applied to dynamic memory cells. Conditions necessary to ensure efficient gettering by various species (B, Ar, Kr, and Xe) are established based on achieving a sufficient density of $\mathbf{b} = \frac{1}{2}\langle 110 \rangle$ *dislocations. When the implantation occurs through a screen oxide, dose levels of less than* 3×10^{14} *ions/cm*^{2} *for Ar were found to be suitable. Equivalent leakage reduction was obtained for all species. Specifically, B at* 5×10^{15} *ions/cm*^{2} *was as effective in reducing relaxation leakage as was* 1×10^{15} *ions/cm*^{2} *of Ar for the particular thermal history of the investigated process.*

Introduction

Functional yield in high density IGFET dynamic random access memories is often limited by leakage at the storage node and source junction. Experimental evidence confirmed by transmission electron microscopy (TEM) analysis, depicted in Fig. 1, has shown that single-cell leakage failures often coincide with defect(s) in the active region of the device. Cu precipitation on the defect sites was verified by the Moiré fringe spacing and energy dispersive analysis. These defects can be electrically active generation-recombination sites within the active region, and thus increase leakage current.

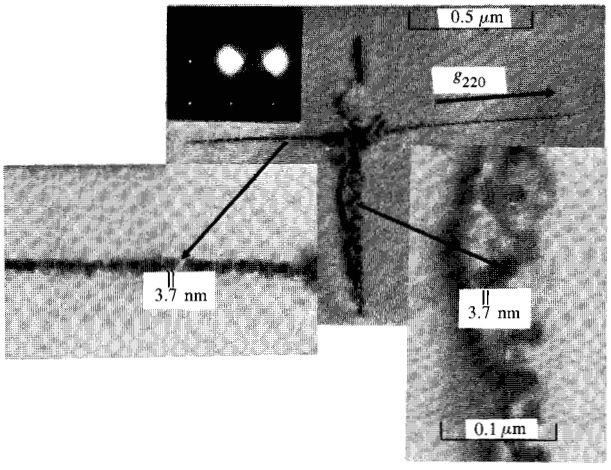

Figure 1 TEM micrograph of defect causing memory cell failure. Note chains of precipitates running in parallel ⟨110⟩ directions. Moiré fringe contrast is perpendicular to $\mathbf{g} = 200$, having a spacing of 3.7 nm, and is consistent with Cu precipitation.

A variety of techniques for gettering (the removal of deleterious metallic contaminants from the active region) have been demonstrated. Impurities can be inherent in the starting wafer or introduced by the processing itself. Their removal to the back of the wafer by various techniques has been observed and studied, *i.e.*, mechanically introduced damage [1, 2], phosphorus diffusion [3, 4], and ion implant damage [5–7]. Ion implant-induced damage is particularly amenable to VLSI semiconductor processing. An increase in the generation lifetime, measured using MOS capacitors, from virtually 0 to as high as 200 μs, has been observed using both implanted O and Ar [8]. By following the implantation of arsenic through a screen oxide to form a p-n junction with a dose of 1×10^{16} Ar/cm^2, improved *I-V* characteristics of the device have been obtained [9].

This paper deals with the technique of backside ion implant gettering as applied to reducing relaxation leakage and implanted junction leakage. The paper details the de-

termination of a critical gettering dose for B, Ar, Kr, and Xe for a given thermal process [10, 11]. The effect of the presence of a screen oxide during the backside gettering step is discussed. Equivalent leakage improvement is seen for all investigated species. Optimizing the **b** = 1/2 ⟨110⟩ dislocation density for Ar implanted into Si is shown to be necessary, as in the case of Xe [12].

Dose and specie effects

Experimental procedure

The dependence of gettering efficiency on species and dose and the resulting leakage reduction were determined experimentally. Two-ohm-cm ⟨100⟩ p-type silicon wafers known to have low concentration levels of copper as their principal metallic contaminant were used. Initially, all samples were chemically cleaned using a three-step sequential (basic-acidic-basic) procedure. Half the population received a 50-nm SiO_2 insulator grown at 1000°C in dry O_2 on both sides of the wafer. Each wafer was then implanted on the back side employing a three-quarter wafer silicon mask. The mask was prepared by removing one-quarter (a quadrant) of a silicon wafer by laser cutting. This provides four separate quadrants per wafer. The backside gettering implant consisted of either (a) the same specie at three dose levels or (b) three species at a single dose level. In the latter case various energies (135–300 keV) were used to evaluate variations in the volume of the ion-damaged region. In all cases one of the quadrants did not receive a backside gettering implant and, therefore, served as an experimental control. Dose levels of 10^{13} to 6×10^{15} ions/cm^2 at 175 keV for ^{11}B, ^{40}Ar, ^{84}Kr, and ^{132}Xe were used for case (a). In case (b) ^{11}B, ^{40}Ar, and ^{132}Xe at dose levels of 10^{14} to 8×10^{15} ions/cm^2 at energies of 135 to 300 keV were utilized. However, results are presented only for the subset implanted at 175 keV. Immediately after backside implant, the 50-nm SiO_2 screen was removed from the appropriate wafers. All wafers received a pre-oxidation cleaning similar to that initially given to the wafers. A dry O_2 gate oxide (with HCl) was then grown at 1000°C, followed by an *in situ* N_2 annealing. The approximate time at elevated temperature was 80 minutes, which was sufficient in all cases to induce recrystallization of the ion-implanted region. The wafers were then metallized through a mask so that Al dots were formed on the front side. Blanket Al was evaporated on the stripped back side to complete the electrical contacts for the MOS capacitor structures.

The resulting MOS capacitors were characterized by pulsing the device from accumulation into deep depletion, as depicted in Fig. 2(a), which indicates the transient capacitance response. The equivalent leakage current, for the relaxation of capacitance (from C_S to C_E) as a function

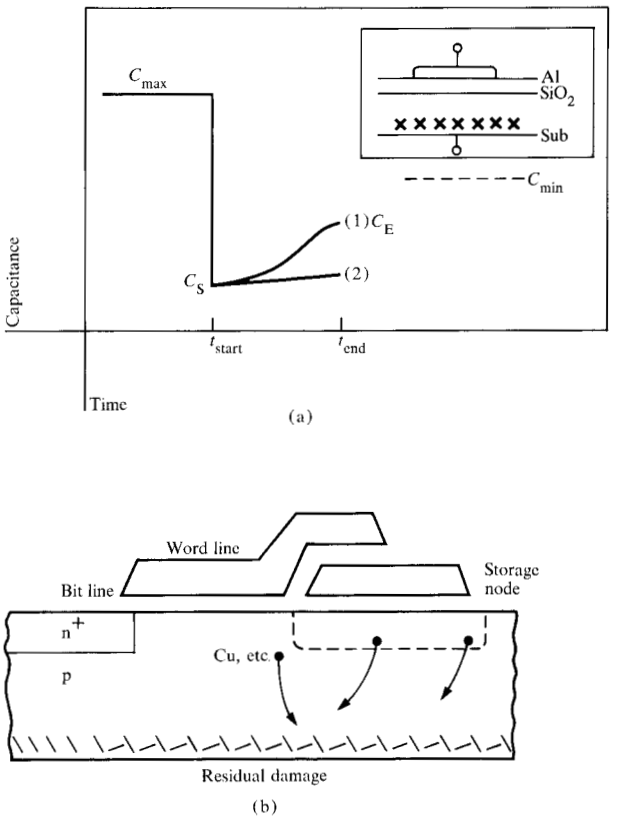

Figure 2 (a) Capacitance as a function of time when pulsed from accumulation to deep depletion. This characteristic is used to calculate relaxation leakage current. (b) Representation of removal of metallic contaminants by residual backside damage for a one-device memory cell.

of time to a quasi-equilibrium value after a fixed time, was calculated [13, 14]. Decreasing values of relaxation leakage current indicate a reduction in the number of generation sites within and near the depletion region. This relationship provides a measure of the efficiency of gettering metallic contamination to the back of the wafer and out of the active storage region of the device, as indicated schematically in Fig. 2(b). Heavy metals diffuse during processing to the damaged region and become trapped. Note that this structure and measurement display the dominant leakage mechanism for the storage node of a one-device dynamic memory cell.

Transmission electron microscopy was used to study the microstructure associated with backside ion implant gettering. Samples were prepared by chemically jet thinning from the front side with HF-HNO_3. In some cases, the gettering centers were delineated, after electrical characterization, by diffusion of Cu into the implanted region. Diffraction contrast conditions were selected to characterize the resulting dislocations in the conventional manner.

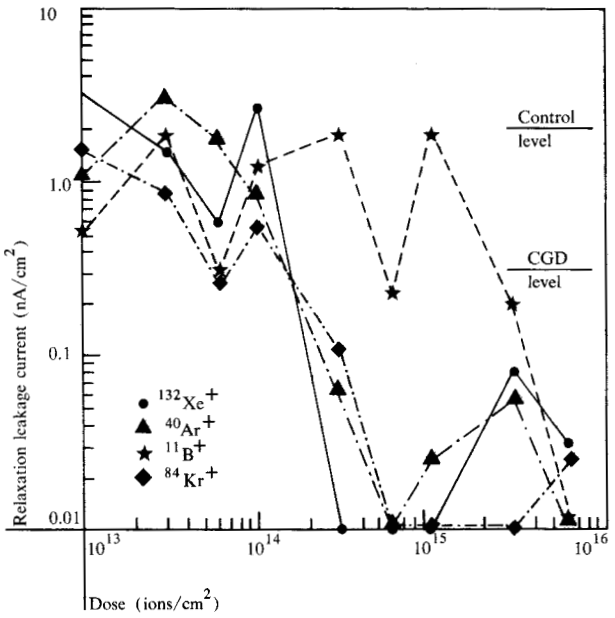

Figure 3 Relaxation leakage current as a function of dose for ^{11}B, ^{40}Ar, ^{84}Kr, and ^{132}Xe implanted into bare silicon on the back side of the wafer.

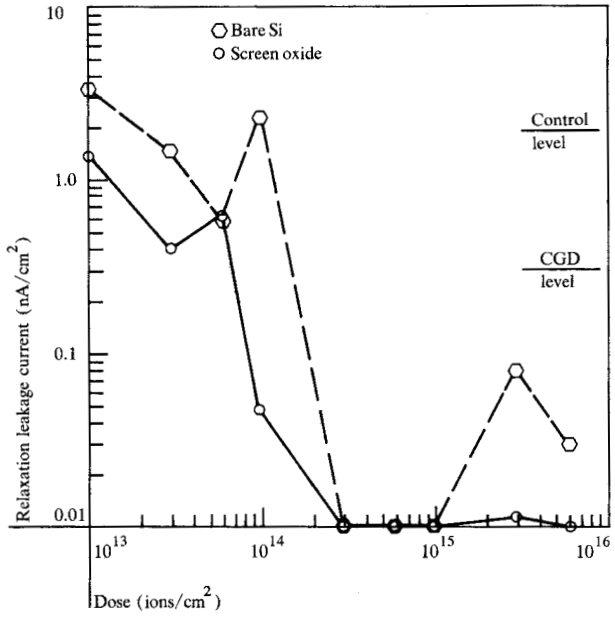

Figure 4 Relaxation leakage current as a function of dose for ^{132}Xe at 170 keV implanted either into bare silicon or through an SiO_2 screen.

• *Results and discussion*

Gettering efficiency, as determined by an average relaxation leakage current for various species at a fixed energy of 170 or 175 keV without a screen oxide, is shown in Fig. 3. (Xe was implanted at 170 keV due to a limitation on the mass energy product of the analysis magnet.) The indicated control level of 2 nA/cm^2 represents the statistical nongettered leakage level for the entire experimental population. For test structures of this nature, leakage levels of approximately 0.3 nA/cm^2 are adequate for device performance. Therefore, for comparative analysis, the implant dose corresponding to this level of leakage is henceforth referred to as the critical gettering dose (CGD).

Heavier ions, such as ^{40}Ar, ^{84}Kr, and ^{132}Xe, show a significant reduction in relaxation leakage for doses greater than 2×10^{14} ions/cm^2. The gettering efficiency also appears to become degraded for ^{40}Ar, ^{84}Kr, and ^{132}Xe at higher dose levels. This region corresponds to the presence of bubbles of the implanted elements in the lattice, which we have observed by TEM micrographs. In contrast, ^{11}B, being a very light ion and having a stopping mechanism that is predominantly coulombic, requires an order of magnitude higher dose to achieve the same leakage levels. Although the critical gettering dose is specie dependent, ultimately the same gettering efficiency was achieved, *i.e.*, relaxation leakage levels of less than 0.1 nA/cm^2.

When the backside implant was done through a 50-nm SiO_2 screen for certain species, a reduction in the critical gettering dose was observed. Figure 4 depicts this result for Xe at 170 keV. Accounting for the transmission coefficient, due to the presence of the screen, the CGD is reduced from 1.8×10^{14} to 6.6×10^{13} ions/cm^2. Table 1 summarizes this effect of the SiO_2 screen for ^{11}B, ^{40}Ar, ^{84}Kr, and ^{132}Xe. The heavier elements, ^{84}Kr and ^{132}Xe, show more than a factor of two reduction in the critical gettering dose. Being the lighter species, ^{11}B and ^{40}Ar do not exhibit this dependency. However, due to scatter in the data for ^{11}B, the value of 2×10^{15} ions/cm^2 with a screen oxide is an estimate.

The reduction of relaxation leakage current has been shown [10, 12] to be coincidental with the formation of a residual defect density of 10^9–10^{10}/cm^2. Furthermore, the ability of $\mathbf{b} = 1/2\langle 110\rangle$ dislocations to getter by precipitation was found to be more favorable than $\mathbf{b} = 1/3\langle 111\rangle$ Frank partials. The resulting microstructures of the residual damaged region responsible for the gettering action of implanted ^{40}Ar at 175 keV are shown in Fig. 5(a) as a function of dose. For doses between 1×10^{14} and 3×10^{14} ions/cm^2 the defect density drastically increases and $\mathbf{b} = 1/2\langle 110\rangle$ dislocations become dominant. The resulting improvement in relaxation leakage current as the $1/2\langle 110\rangle$ perfect dislocation density increases is shown in Fig. 5(b) where relaxation leakage current, total defect density, and dislocation density are plotted as functions

Table 1 Critical gettering doses. (This table was originally presented at the Spring 1977 Meeting of The Electrochemical Society, Inc., held in Philadelphia, PA.)

Specie	*Critical gettering dose* (ions/cm^2)		
	No screen	*Screen*	
		total	in Si
B	3.2×10^{15}	$\sim 2 \times 10^{15}$	$\sim 2 \times 10^{15}$
Ar	2×10^{14}	2.5×10^{14}	2.46×10^{14}
Kr	2.3×10^{14}	5×10^{13}	4.6×10^{13}
Xe	1.8×10^{14}	8×10^{13}	6.6×10^{13}

of dose. Thus, to optimize the utility of gettering metallic contaminants and reducing the relaxation leakage current, one should ensure that the end of process residual backside defect structure is of sufficient density, which is **b** = 1/2 ⟨110⟩ dislocations.

Electrical measurements indicated a significant reduction in the critical gettering dose when the backside Xe implantation was done through a 50-nm screen oxide. In Fig. 6, comparing the bare Si and screen oxide cases, the TEM micrographs show that the residual defects begin to nucleate significantly at a lower dose when implanted through a screen oxide. Presumably, at these dose and energy levels, the heavier ions would cause a significant knock-on reaction with the O_2 in the screen. Thus, the microstructure is due to the accumulative effect of the implanted Xe plus the recoiled O_2.

Even the lightest specie investigated (^{11}B) can be used effectively for gettering metallic contaminants. Figure 7 is the multibeam bright field micrograph for doses of 1×10^{15} $^{11}B^+$ ions/cm^2 at 175 keV into bare Si with the gettering centers delineated by diffusion of Cu. The Cu-rich precipitates, which are relatively opaque to electrons, tend to cluster preferentially on or near the **b** = 1/2 ⟨110⟩ dislocations (D). Frank partial loops (F) with associated stacking faults are not as efficient gettering centers. Others have reported [6] limited or no success using backside-implanted ^{11}B for gettering purposes; however, the results of Fig. 3 are indeed more favorable. Perhaps in this work the thermal conditions were more favorable in forming and maintaining the critical defect structure throughout the entire process sequence. An additional advantage results from using ^{11}B for n-channel processes; the presence of a p^+ region makes an ohmic backside substrate contact more reliable [15]. In light of the memory device requirements, which force the designer to higher resistivity substrates, this can become a significant advantage.

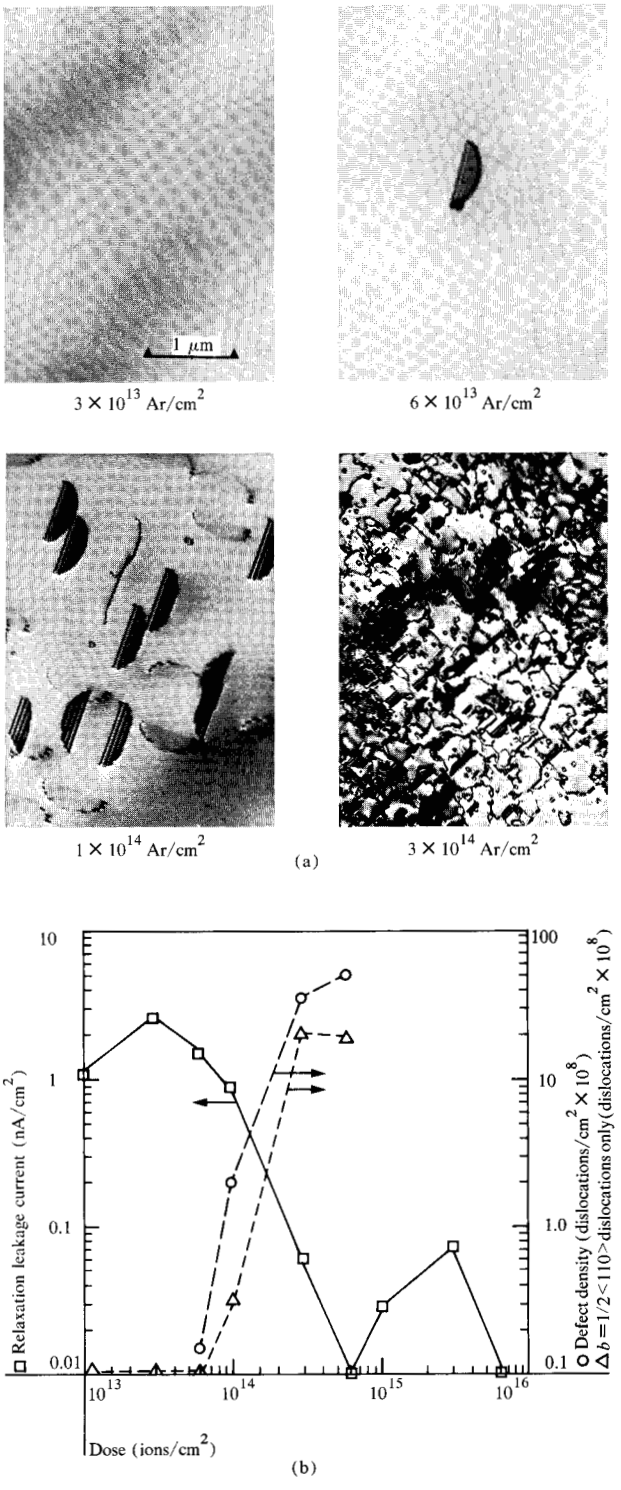

Figure 5 (a) TEM micrographs indicating the microstructural change of the lattice as the ^{40}Ar dose at 175 keV is increased from 3×10^{13} to 3×10^{14} ions/cm^2. Implantation was into bare silicon. (b) Relaxation leakage current, total defect density, and **b** = 1/2⟨110⟩ dislocation density as functions of dose for ^{40}Ar at 175 keV implanted into bare Si. This figure was originally presented at the Spring 1977 Meeting of The Electrochemical Society, Inc., held in Philadelphia, PA.

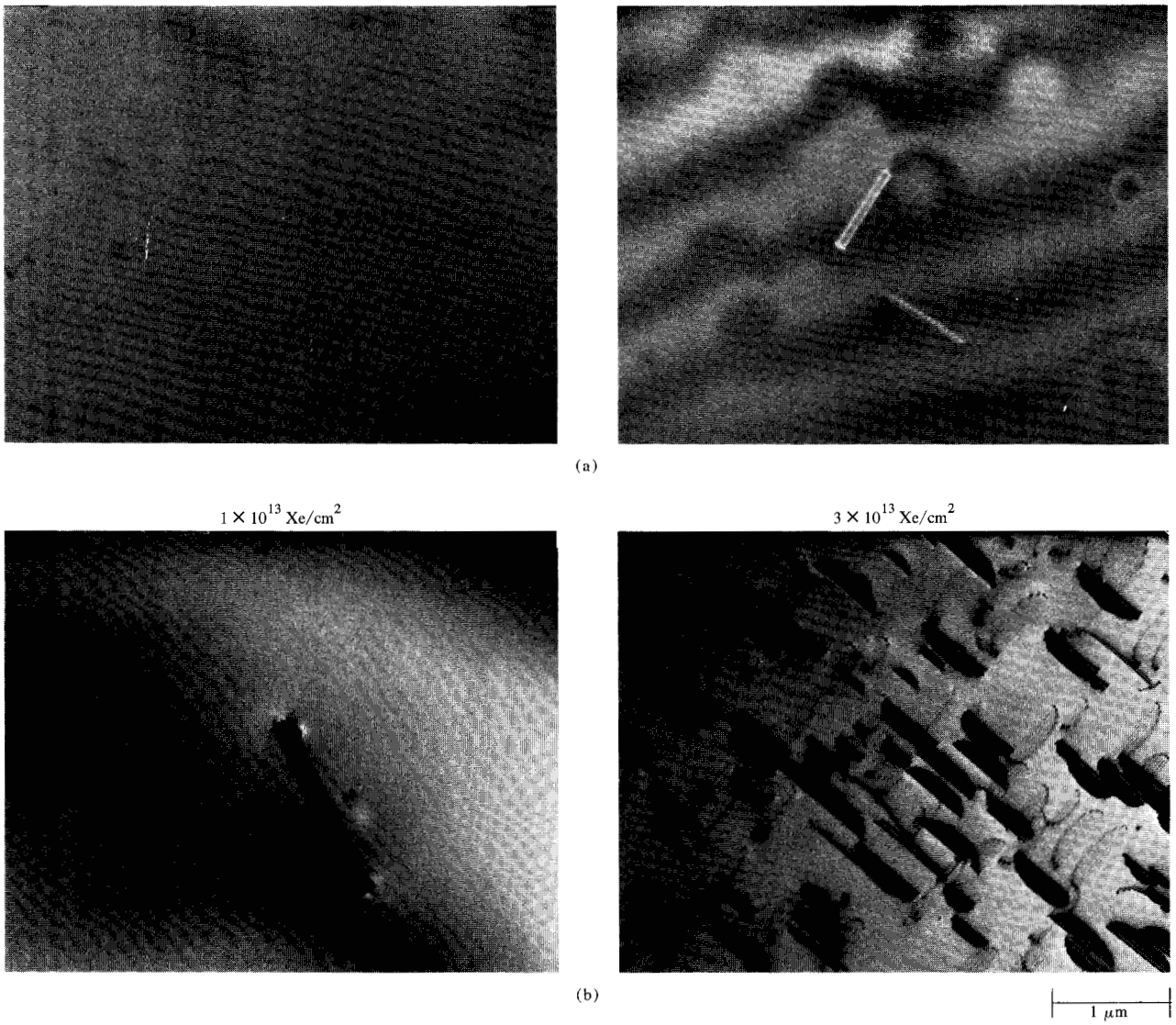

Figure 6 TEM micrographs showing the effect of implanting ^{132}Xe (a) into bare silicon and (b) through a screen oxide at 170 keV.

Applications of backside ion implant gettering

Having established the specie and dose dependence, as well as the mechanism, the technique of leakage reduction by backside ion implantation was applied experimentally to fully processed device structures, such as MOS and MSOS capacitors, gated diodes, and IGFETs. Two different experimental process technologies were investigated: a dual insulator metal gate process and a dual polysilicon gate process. In both cases, preliminary studies were done to establish the optimum gettering introduction point(s) such that three conditions were satisfied: (1) retardation of stacking fault nucleation [16], (2) residual end of process damage consistent with the critical microstructure discussed above, and (3) reduction in the effectiveness of competitive gettering mechanisms that lie in the active region of the device.

Doses of ^{11}B at 5×10^{15} and of ^{40}Ar at 1×10^{15} ions/cm^2, at 175 keV, were investigated for reducing relaxation leakage in an experimental dual insulator metal gate device process. Large area capacitor structures at the wafer level were characterized for leakage and compared to a "pseudo-specification" derived from the total experimental population to establish a yield criterion. Multiple lots were processed at different times with wafer-to-wafer and within-wafer experimental controls. Histograms showing the percent relative frequency of occurrence *versus* the "relaxation leakage yield" for boron, argon, and non-

gettered cases are shown in Fig. 8 for more than 300 wafers with 20 measurements per wafer. The results for the nongettered control case are very broad over the entire yield range, whereas in the gettered cases (^{11}B and ^{40}Ar) tight distributions above 70 percent are obtained. Both boron and argon appear equally effective with cumulative percentages of 81 and 76 above a relaxation leakage yield of 90 percent.

There are technology issues which may influence the choice of gettering element. Argon, being easily ionized, affords high beam currents and, therefore, reduced process time per wafer. However, *in situ* heating at high beam current can dramatically affect its gettering efficiency. Boron, having a much larger range in Si, SiO_2, and Si_3N_4, adds more flexibility by its variable introduction point in the process, and it can ultimately provide a larger volume for gettering metallic contaminants. Therefore, the choice is not clearcut; each utilization of this technique must be viewed with the particular process technology and its accompanying tool set in mind.

Backside implant gettering was also used to reduce the junction leakage of implanted source drains for IGFETs fabricated in a dual polysilicon gate n-channel technology. The n^+-p junctions were formed by implanting $^{75}As^+$ at 8×10^{15} ions/cm^2 through 45-nm screen oxide. This was followed by a re-oxidation/anneal cycle at 1000°C to achieve a junction depth of 0.4 μm. Argon ($^{40}Ar^+$) at 175 keV with a dose level of 1×10^{15} ions/cm^2 was implanted on the back side through a screen oxide (30 nm) early in the process for gettering mobile metallic contaminants. Large area gated diodes [17] were characterized, permitting the separation of the junction and surface leakage mechanisms. Results of a controlled experiment comparing only the effects of backside argon (Ar) gettering on gated junction leakage are shown by the comparative histograms in Fig. 9. A 3-volt reverse bias was applied with the gate at -1 volt (accumulation); therefore, the measured leakage is that of the junction alone. The gettered population had effectively one-tenth the junction leakage of the ungettered sample. Although a distinct difference in junction leakage was observed, the level of metallic contamination was sufficiently low so as not to affect the breakdown voltage of the two groups. Typically, the breakdown voltage was 14–15 volts with sharp *I-V* characteristics. Furthermore, TEM analysis did not show a reduction in the residual damage that occurs when arsenic is implanted through a screen oxide [9].

Summary

Inert elements such as Ar, Kr, and Xe have been shown to be equally effective in decreasing relaxation leakage in silicon when ion-implanted into the wafer back side. The critical gettering dose of these species is almost an order of magnitude lower than that of B when implanted into bare silicon. However, as in the case of boron, it appears not to be necessary to render the material amorphous. A further reduction in the critical gettering dose to less than 1×10^{14} ions/cm^2 occurs for Kr and Xe when implanted through a screen oxide.

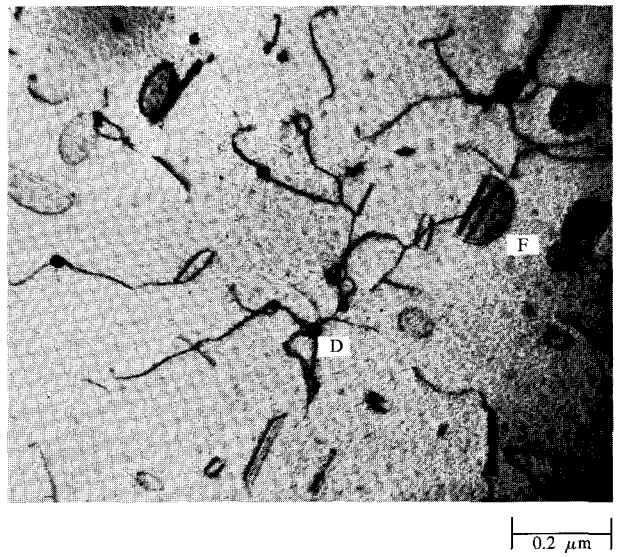

Figure 7 Multibeam bright field micrograph of 1×10^{15}-ion/cm^2 doses of ^{11}B implanted at 175 keV, Cu decorated, and annealed. The Cu-rich precipitates preferentially cluster on the $\mathbf{b} = 1/2\langle 110\rangle$ dislocations (D) as compared to the Frank partial loops (F).

Reduction of relaxation leakage current with dose is coincidental with the formation of $\mathbf{b} = 1/2\langle 110\rangle$ perfect dislocations with a density of approximately 10^9/cm^2. Leakage reduction is believed to be due to the adsorption of mobile metallic contaminants preferentially by these dislocations as compared to $\mathbf{b} = 1/3\langle 111\rangle$ Frank partials. Therefore, in applying this technique, the exact thermal history and its consequences on the end of process residual disorder are of prime importance. Also, competitive gettering centers in the active regions of the device must be considered. Process temperatures that exceed the activation energy for release of these gettered impurities must be avoided.

Backside implant gettering was applied to two experimental device process technologies. The use of B or Ar increased the cumulative percentage of relaxation leakage yield greater than 90 percent from 12 to at least 76 percent. Boron can be just as effective as an inert specie, such as Ar, provided its critical gettering dose is exceeded and the thermal process history provides suf-

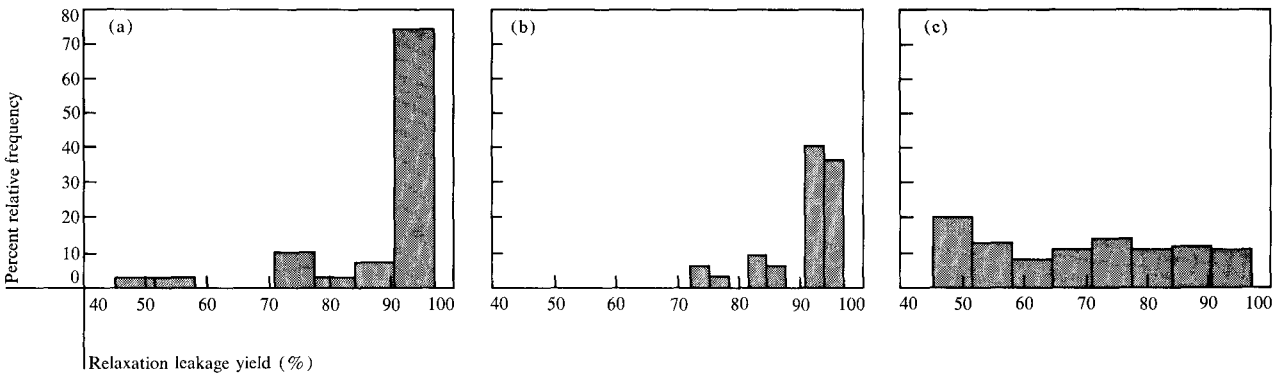

Figure 8 Histograms of percent relative frequency for relaxation leakage yield for gettered [(a) boron and (b) argon] and the non-gettered control (c).

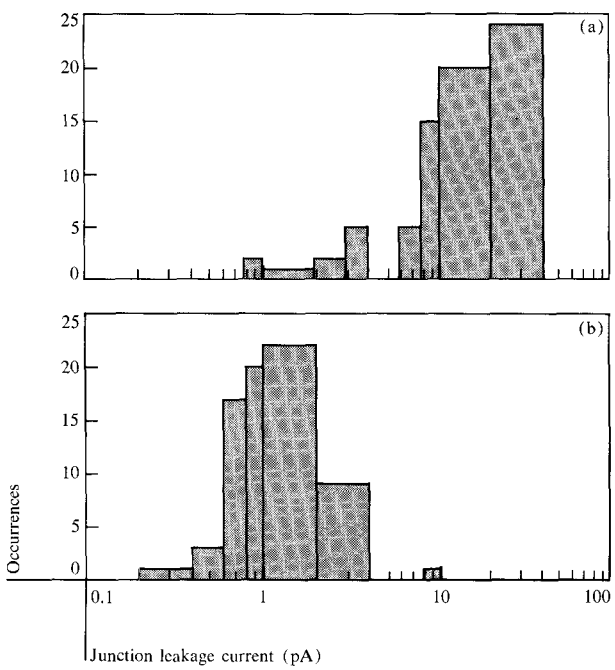

Figure 9 A comparison of the distributions for junction leakage current using a gated diode configuration, with $V_D = 3$ V, $V_G = -1$ V, and area = 1.93×10^{-3} cm^2. (a) ungettered experimental control; (b) n^+-p junction gettered with an ^{40}Ar dose of 1×10^{15} ions/cm^2 at 175 keV.

ficient residual defect density. Reverse bias junction leakage for ion-implanted arsenic devices was decreased by gettering metallic impurities from the active region using backside-implanted argon. At a dose of 1×10^{15} ions/cm^2 of Ar, the junction leakage was reduced an order of magnitude to 0.2–4.0 pA (0.1–2.1 nA/cm^2). An improvement in breakdown voltage was not observed.

Implantation of certain elements and the consequential residual damage has been shown to reduce two leakage mechanisms that are of prime importance for dynamic random access memory. Specifically, the capability of the storage node to retain its programmed information has been enhanced significantly by reducing relaxation and junction leakage.

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