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An Overview of Materials and Process Aspects of Josephson Integrated Circuit Fabrication

Presented here is an overview of materials and process aspects of a method that has been developed for fabricating experimental integrated circuits containing Josephson junctions as active elements. Superconducting Pb-alloy thin films are used for forming the junction electrodes, and a combination of thermal and rf oxidation is used for forming the tunnel barrier oxides. In addition to the junctions, the circuits, which are formed above an insulated, superconducting Nb ground plane, also contain: superconducting Pb-alloy lines, contacts, and transformers; $AuIn_2$ damping and terminating resistors; insulated crossings; etc. Insulation between the ground plane and overlying conducting layers is achieved through use of a combination of Nb_2O_5 and SiO. The latter is also used to achieve insulation between overlying conducting layers and as a final protective coating. Photoresist processes are used for layer patterning.

Introduction

This paper provides an overview of the materials and process aspects of a method for fabricating experimental integrated circuits that use Josephson junctions as active elements. Specifically considered are photolithographic patterning of layers, junction electrode strength, and tunnel barrier oxide formation. Other relevant materials and process studies are discussed in the accompanying paper by Greiner *et al.* [1] and its cited references.

An initial description of the method used in this laboratory for fabricating experimental Josephson integrated circuits is contained in the paper by Greiner *et al.* [2]. That paper also reviews previous, related efforts. A description of the method, as it is presently being practiced, is contained in the accompanying paper by Greiner *et al.* [1]. Experimental circuits which have been fabricated through its use, together with device and circuit design aspects, are reviewed in the accompanying paper by Matisoo [3]. Adaptations of the method which have been used in other laboratories have been described by others [4]. In the circuits, Josephson tunneling devices are used mainly to achieve current steering and, thereby, memory and logic circuit function implementation. The motivation for investigating such circuits is primarily the promise they hold of high speed at low power in computer applications [5].

Circuit fabrication begins with the formation of a superconducting Nb ground plane. The Nb is deposited as a 300-nm-thick film either by means of rf sputtering or vacuum evaporation onto an oxidized silicon wafer and is patterned by etching in the presence of a photoresist layer; the Nb is next anodized by liquid anodization in order to form an overlying Nb_2O_5 insulation layer. Overlying superconductive and resistive layers are formed by vacuum deposition of alloy films up to about 800 nm in thickness consisting of two or three of the materials: Pb, In, Au, and Bi. Associated insulation layers are formed by vacuum deposition of SiO. A combination of thermal and rf oxidation processes is used in order to form the Josephson tunneling oxides. Optical photolithographic techniques (primarily the so-called "photoresist lift-off" technique) are used for pattern formation, thereby making it possible to fabricate circuit configurations containing minimum dimensions of about 2.5 μm. The configurations thus formed constitute the circuit elements required for formation of integrated logic and memory circuits; *viz.*, Josephson tunneling junctions and associated superconducting controls, lines and contacts, insulated crossings, damping and terminating resistors, etc.—all above an insulated superconducting Nb ground plane. After completion of the circuits, a 2-μm-thick coating of SiO is formed everywhere but over the regions at which solder

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terminals [6] or contact pads are formed. Finally, circuit chip formation is achieved by dicing of the completed silicon wafer into multiple 6.35 $\times$ 6.35 mm^2 chips [2].

An illustrative Josephson device is the logic circuit interferometer [7] shown in Fig. 1. The passage of current through either of the Pb-In(12 wt%)-Au(4 wt%) control lines gives rise to a magnetic field that alters the Josephson current threshold of the underlying junction configuration. The Pb-In-Au ternary consists of the Pb-In solid solution phase with In(13 at%) and second phase particles of the intermetallic compound $AuIn_2$. An SiO layer which contains 5-μm-diameter circular openings ("windows") is used between its Pb-In-Au base electrode (same composition used for the control lines) and the Pb-Bi (ϵ-phase) counter electrode to define the junctions. Circular openings are used in order to favor achievement of minimum junction area variability. To avoid resonances, which arise because of the inherent high Q of interferometer configurations, use is made of several $AuIn_2$ damping resistors which are located directly beneath the base electrode layer and shunt the junctions to each other. Deleterious interdiffusion effects at base electrode-to-resistor contacts are avoided primarily because of the choice of the $AuIn_2$ phase of the base electrode for formation of the resistor [8]. Recently, circuit fabrication has been extended to circuits containing devices with 2.5-μm-diameter junctions. Logic circuit delays thus achieved have been the lowest reported to date: average delays per circuit of 26 and 13 ps for ten-stage, two-input AND and OR circuits, respectively [9].

Generally, as in semiconductor integrated circuits, use is made of the layers used in device formation for forming most of the additional elements needed for circuit formation. For example, the layer with which insulation is achieved between the tunneling junctions and overlying control lines also provides insulation at insulated crossings; the superconducting layers used for formation of the base electrode and control lines are also used for forming x and y lines which interconnect different logic circuits or memory cells. Since the compositions of the latter two are the same, deleterious interdiffusion effects at x and y line contacts are thus avoided.

Photolithographic patterning of layers

In the past, vacuum deposition through metal masks was commonly used to fabricate the configurations used in superconducting thin-film circuits [10]. However, when this approach was used, linewidths were generally limited to about 125-250 μm. Results reported by Matisoo [11] suggested that subnanosecond circuit operation should be within reach through the use of such circuits if they contained Josephson junctions as active elements and could be fabricated with narrower lines.

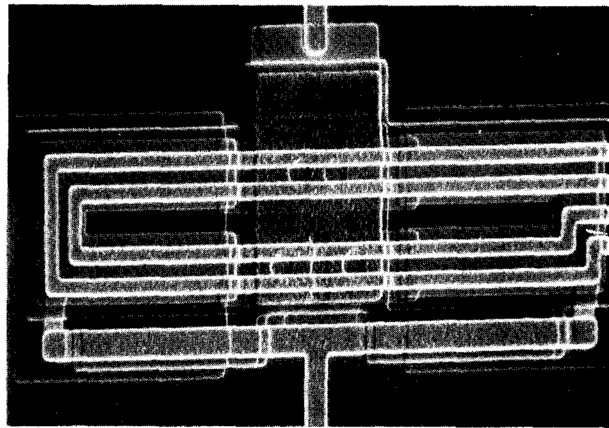

Figure 1 Scanning electron micrograph of a typical logic circuit interferometer (from [7]). Beneath the interferometer is an insulated ground plane and $AuIn_2$ damping resistors (not visible in the micrograph). The interferometer contains four Josephson tunneling junctions, which are formed through the use of a Pb-In-Au base electrode, Pb-Bi counter electrode, and an intervening SiO layer; the latter contains four 5-μm-diameter circular openings ("windows") which define the junction areas. Above the junctions, separated from them by another SiO layer, are two 2.5-μm-wide Pb-In-Au control lines. The functions of two additional, peripheral layers (SiO and Pb-In-Au) are described in the cited reference.

Achievement of the latter required the use of photolithographic processes rather than evaporation through masks for patterning purposes. There were several choices available if such processes were to be used. The one most frequently used involves the use of photoresist as an etch resist. Another, which is more suitable for patterning multilevel thin-film structures and materials that are difficult to etch, is the so-called "stencil lift-off" choice. It involves formation of a photoresist "stencil" on the substrate on which formation of a patterned layer is desired, followed by film deposition and subsequent removal of the stencil (and the portions of the film which have been deposited onto it) by immersion in a suitable solvent. Some degree of agitation is usually needed in order to assure effective removal. Although the approach is quite effective for patterning relatively thin films, it is often difficult to avoid the formation of frayed edges of patterned layers unless the photoresist edges are quite sharp or contain a reverse taper. Studies by Hatzakis [12] indicated that such a reverse taper could be obtained, for example, by electron-beam exposure. Studies by Grebe *et al.* [13] indicated that an equivalent effect, involving instead optical exposure, could be obtained through use of an aluminum-photoresist composite. The latter was used in our initial circuit fabrication work. Two processes, which were subsequently devised for use with optical exposure, involve utilization of a photoresist stencil that is formed in a manner which renders its lower portion

relatively more sensitive to exposure and/or development. The first, which resulted from studies described by Warnecke *et al.* [14], involves use of a composite consisting of a spun-on layer of positive photoresist and an overlying less sensitive, positive photoresist layer that is first formed as a membrane and applied in that manner to minimize solvent intermixing between the layers (which reduces the differential sensitivity of the composite). The second, which resulted from studies by Canavello *et al.* [15] and is presently in use for circuit fabrication, involves use of a single positive photoresist layer that acquires a differential sensitivity after immersion in chlorobenzene.

Whichever process is used, constraints arise that are associated with the particular layer being patterned as well as with those that have previously been formed on the substrate. If the layer being deposited tends to develop a high intrinsic stress upon deposition, as, for example, in the case of vacuum-deposited Nb, use must be made of a sufficiently thin stencil to avoid "tearing" of the stencil upon deposition [16]. Adhesion of the stencil to underlying layers is usually essential. Generally adhesion can be improved by means of additional resist curing or curing at a higher temperature. If, however, curing times and temperatures must be kept below certain levels to avoid possible deleterious effects on underlying layers that arise, *e.g.*, from thermally actuated diffusion processes, it is often necessary to utilize adhesion promoters. Experience with the materials and processes described in this paper has generally suggested that curing times and temperatures should be kept below 1 hour and 80°C, respectively. That restriction has, *e.g.*, caused photoresist stencil adhesion to underlying SiO layers to be marginal at times; it has been improved by deposition of an approximately 1-nm-thick TiO_x layer upon completion of SiO deposition and use of an appropriate photoresist adhesion promoter [1].

Junction electrode strength

Considerations of performance and processing trade-offs have thus far favored the use in the circuit fabrication method under review here of Pb-In-Au films as junction base electrodes. Although the use of Nb might be more favorable on the basis of mechanical strength considerations, junctions fabricated on Nb base electrodes have been found to have capacitances which are higher (by about a factor of three) than comparable junctions fabricated on Pb-In-Au films [16, 17]; thus, slower circuit operation would result [18]. Lower junction capacitances, however, have recently been obtained through the use of Si- or Al-clad Nb or Nb-alloy films [19-21], but more effort would be required on junction fabrication using such films before they could be regarded as viable alternatives.

The choice of Pb-In-Au was an outgrowth of attempts to use Pb as a base electrode material. Junctions fabricated through the use of Pb films develop shorts upon cycling to 4.2 K—most likely as a result of plastic deformation of the Pb and associated rupturing of the tunneling oxide. Such deformation results from the inability of the films to elastically sustain the strains arising from differences in expansion coefficients of the films and their underlying substrates [22]. On a typical glass or oxidized silicon substrate, *e.g.*, because of the relatively large expansion coefficient of Pb ($\approx 30 \times 10^{-6}/°C$), the films experience a tensile stress upon cooling and, unless they are capable of supporting the stress elastically, experience an associated compressive stress upon warming. Comparing calculated strains expected from 4.2 to 350 K if the stress could be supported elastically with those obtained experimentally from *in situ* x-ray measurements of film lattice parameters, Murakami *et al.* [23, 24] found the following for Pb films thicker than about 200 nm which had been deposited onto oxidized silicon wafers: (1) At low temperatures, the relaxation of tensile stress upon cooling and compressive stress upon subsequent warming take place primarily by dislocation glide, and (2) at temperatures above about 50 K, diffusion-related relaxation processes become increasingly evident; the latter appear to contribute, in part at least, to the appearance of nonuniform deformations—such as grain growth, grain rotation, whisker growth, hillock growth, etc.

Initial attempts at strengthening of Pb base electrodes involved the use by Anacker *et al.* [25] of a relatively thin underlayer of In. Since Pb and In interdiffuse rapidly at room temperature ($D \approx 10^{-14}$ cm^2/s), this procedure results in formation of a Pb-In alloy film [26, 27]. Junctions formed through use of the Pb-In(6-10 wt%) base electrode films showed considerably improved resistance to shorting upon cycling to 4.2 K. Subsequent studies by Lahiri [28] of hillock growth upon heating of such Pb-In films to about 75°C (necessary for the photoresist curing steps that would need to follow junction formation in the fabrication of completed circuits), as well as cooling to 4.2 K, indicated that further improvement could be achieved by the addition of several wt% of Au. Similar results obtained in those studies using Au itself as an addition to Pb films led to the subsequent use of Pb-Au(1.7 wt%) films for junction counter electrodes. X-ray diffraction and transmission electron microscopy studies of typical Pb-In-Au films (containing up to about 12 wt% In and several wt% Au) have indicated that such films consist of grains of Pb-In solid solution and interspersed second phase particles of $AuIn_2$ [28, 29].

An illustration of the effect of the additional Au on the ability of Josephson junction devices to survive cycling

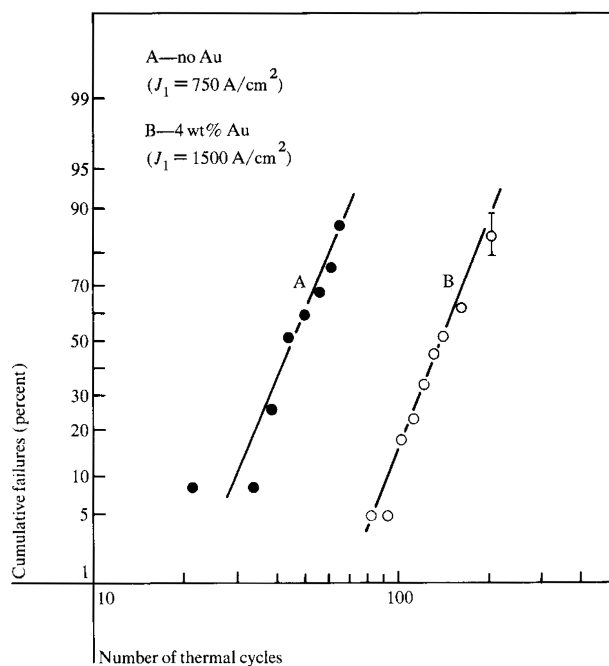

Figure 2 Illustrative cumulative failure data for two sets of junctions as a function of the number of cycles to 4.2 K to which they were subjected (from reference [30]). Companion data indicate that the superiority of set B is due primarily to the addition of 4 wt% Au to the Pb-In base electrodes of the junctions in that set.

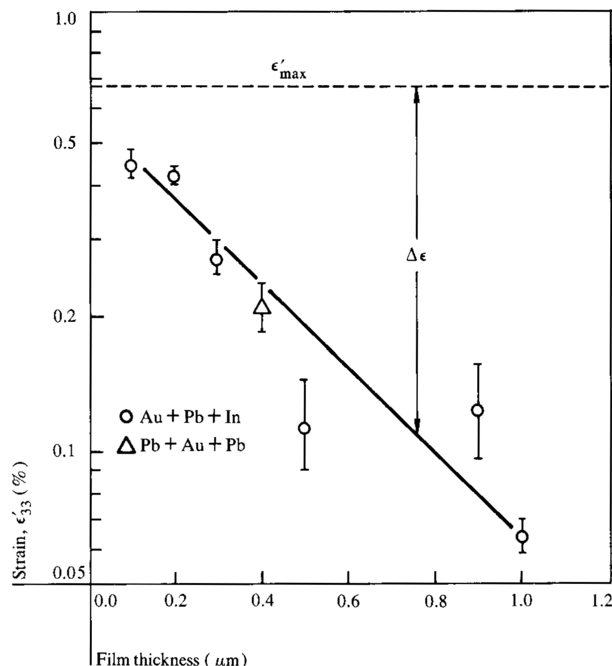

Figure 3 Illustrative thickness dependence of strain at 4.2 K of two types of Pb-alloy films (from reference [34]). The designations Au+Pb+In and Pb+Au+Pb refer to the deposition sequences of the layers from which the alloy films were formed.

from room temperature to 4.2 K is shown in Fig. 2. The data are for two sets of 19 devices and are from a paper by Basavaiah and Greiner [30]. The Josephson devices they used were fabricated using the approach described by Greiner *et al.* [1] and contained 25 × 25 μm^2 junctions and overlying, insulated superconducting controls. For set A, use was made of 400-nm-thick Pb-In(8 wt%) base electrodes; for set B, base electrodes which contained, in addition, 4 wt% Au were used. In both sets, use was made of 500-nm-thick Pb-Au(1.7 wt%) counter electrodes. The cumulative failure level is plotted against the number of cycles to 4.2 K. Using the indicated vertical axis, straight-line behavior implies that the data can be characterized by a log-normal statistical distribution. As can be seen, the addition of the Au reduced the failure level from, *e.g.*, about 90% to 5% after 70–80 cycles. Associated results cited by the authors indicate that the reduction could be attributed primarily to the addition of the Au.

A further improvement—a reduction by about an order of magnitude in the failure level—was obtained by reducing the thickness of the junction electrodes by about a factor of two and making several other changes [31]. It was attributed in part at least to the thickness reduction. Previous studies by Caswell *et al.* [32] of stresses in Pb films at low temperatures and, in addition, more recent studies by Murakami [33] and by Murakami and Kircher [34] have indicated that a thickness reduction should result in film strengthening. Surprisingly, however, the strain levels (as obtained from lattice parameter measurements) that could be supported at 4.2 K by Pb-alloy films of the type used for the junction electrodes were similar to those found for Pb films. In their paper, Murakami and Kircher [34] suggest that this is an indication that the uniformity as well as the magnitude of the resulting plastic deformation in such films needs to be considered in assessing possible causal factors responsible for improved junction "cyclability" [35]. Figure 3 shows their data for Pb-In(12 wt%)-Au(4 wt%) and Pb-Au(1.7 wt%) films on oxidized silicon wafers, illustrating the dependence of the tensile strain ϵ'_{33} at 4.2 K that such films acquire upon cooling to that temperature as a function of film thickness. The indicated values of ϵ'_{33} were calculated from the measured lattice parameter d at 4.2 K using the relation $\epsilon'_{33} = (d - d_0)/d_0$, where d_0 is the strain-free value of d. The dashed line ϵ'_{max} represents the strain level calculated using thermal expansion coefficient data for Pb and Si that would have been expected had no strain-relaxation occurred as a result of the cooling; correspondingly, the

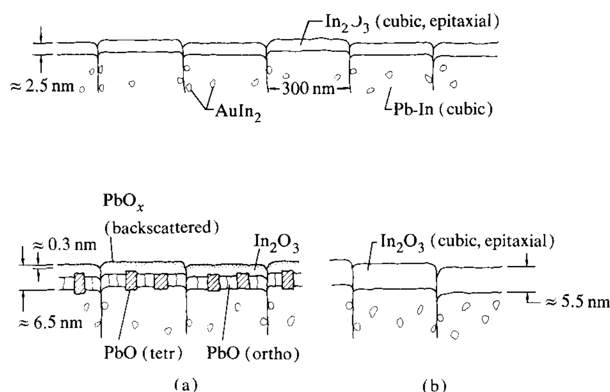

Figure 4 Illustrative states of Pb-In-Au junction base electrode after thermal oxidation and subsequent rf oxidation (from reference [38]). The upper portion depicts its state after thermal oxidation at 75°C. The lower portions depict its state after subsequent rf oxidation at 24°C; portion (a) depicts its state if about 13 at% In is in solution with the Pb and rf oxidation is carried out on a Pb-coated rf electrode; portion (b) depicts its state if about 20 at% or more In is in solution with the Pb and rf oxidation is carried out on an In-coated rf electrode.

amount of strain-relaxation that occurred is given by the quantity $\Delta\epsilon = \epsilon'_{max} - \epsilon'_{33}$. As can be seen, it decreases with decreasing film thickness.

Recently, the use of Pb-Au(1.7 wt%) counter electrodes has been replaced by use of Pb-Bi (ϵ-phase) for that purpose; the latter contains about 29 wt% Bi. The change was made primarily because of the relative superiority of films of the latter type with regard to cycling-induced hillock formation [36], but other advantages also resulted. For example, sharper junction *I-V* characteristics—advantageous for logic circuit design—resulted because of a decrease by about 40% which occurred in the excess junction current at voltages less than the gap voltage [37]. This could be attributed to the fact that the Pb-Bi (ϵ-phase) is a single phase superconductor whereas, in the case of the Pb-Au, excess tunneling currents arose from the nonsuperconducting $AuPb_3$ second phase material which was present in the Pb-Au [28]. The change caused a corresponding improvement by about a factor of three in junction cyclability [37].

Clearly, more work will be needed in order to further elucidate and address the mechanisms responsible for Pb-alloy electrode strain-relaxation and associated deformation. Our hope is that that effort will continue to result in the achieving of improved junction cyclability.

Tunnel barrier oxide formation

Formation of the tunnel barrier oxides of the junctions is carried out in two stages, resulting in a composite oxide which contains In_2O_3 and several types of Pb oxide [38]. Since aspects of this are covered in two companion papers in this issue [1, 38], only a brief overview of it is presented here. First, following vacuum deposition of the alloying constituents of the Pb-In-Au base electrode layer and "annealing" of that layer at room temperature in vacuum for a minimum of 30 minutes to allow completion of its alloy formation, a "thermal" oxide is formed on it as follows: oxygen is admitted into the vacuum chamber in which the base electrode layer has just been prepared and maintained at a pressure of 2.7 Pa for 30 minutes; oxidation is continued at 75°C at the same pressure for an additional 60 minutes. TEM and XPS [38] studies have indicated that this oxidation process leads to formation of a continuous, epitaxial In_2O_3 layer on the surface of each grain of the Pb-In-Au base electrode film, as depicted in the upper portion of Fig. 4. By contrast, exposure of the Pb-In-Au film to an atmosphere of oxygen at room temperature results in formation of a PbO-In_2O_3 composite. Preference for the former is based on the observation that the In_2O_3 which is thus formed has been found to be virtually unaffected by the subsequent air exposure and photoresist coating and developing process steps which are required next in junction fabrication.

The second stage of tunnel barrier oxide formation, which usually takes place after the intervening formation of a window-defining SiO layer, involves use of an rf discharge in oxygen. This so-called "rf oxidation" process gives rise to an oxidation rate which is initially rapid, and, at least for the oxidation of lead, tends toward zero as a function of time, causing a resulting asymptotic oxide thickness to be achieved. AES studies [38] have indicated that the rf oxygen discharge surface cleaning step which is used just prior to rf oxidation results in the removal of any carbon which might have been introduced by the preceding photoresist processing and, other than causing a slight increase in the thickness of the In_2O_3 layer, leaves it essentially unchanged. Subsequent use of the rf oxidation process involves exposure for 30 minutes to an rf discharge at a typical oxygen pressure of 2.7 Pa and a peak-to-peak rf voltage of 360 V. As a result of the TEM, XPS, AES, and ellipsometric studies which have been carried out [38], the following has been inferred regarding the final state of the oxide thus formed (as depicted in the lower left portion of Fig. 4): (1) Its overall thickness appears to be about 6.5 nm; (2) its lower portion appears to consist of crystalline PbO (a mixture of the tetragonal and orthorhombic forms of PbO), the amount of which decreases with an increase in the In concentration in the base electrode; (3) above the crystalline PbO layer appears to lie the initial epitaxial In_2O_3 layer, which is only slightly altered by the rf oxidation process; and (4) its uppermost portion consists of about a monolayer of PbO

which arises from backscattering during the rf oxidation from a Pb-Bi layer which normally would have been deposited onto the rf electrode on which the samples are mounted as a result of its previous use for junction fabrication—*viz.*, deposition of a Pb-Bi counter-electrode layer. Baker [39] has shown that the latter oxidizes preferentially to form PbO, thus accounting for the appearance of that material as a result of backscattering during the rf oxidation process. The lower right portion of Fig. 4 depicts the resulting oxide which is obtained if use is made of a base electrode containing greater than about 20 at% In in its Pb-In phase and the rf electrode is coated with In prior to rf oxidation—conditions which favor supply of In as the dominant oxidizable metallic species to the growing oxide during oxidation.

Although an initial picture of the composite oxide in use for tunnel barrier formation has thus been developed, much remains to be done before an understanding is achieved of associated mechanisms which account, for example, for the following: the relatively large sensitivity of the Josephson tunneling current level to whether Pb or In are backscattered onto the growing oxide during rf oxidation [38]; its insensitivity to the composition of the lower portion of the oxide [38]; and its increase upon annealing (when Pb is the backscattered material) [40].

Concluding remarks

Materials and process studies have constituted an inherent part of the development of the circuit fabrication method to which this overview and the accompanying paper by Greiner *et al.* [1] have pertained. For example, among the studies reviewed here, the photoresist stencil studies have led to the development of lift-off processes suitable for use in circuit layer patterning by means of optical exposure down to the 2.5-μm linewidth and junction diameter levels; the Pb and Pb-alloy thin-film studies have led to the achievement of considerable improvement in the ability of our junctions to survive repeated cycling to 4.2 K without failure; and the tunneling oxide studies reviewed here have led to an improved understanding of the composition and structure of the tunneling oxide and to the introduction of means into circuit fabrication for improving the chemical stability of that oxide during its formation. In addition to their role in advancing the circuit fabrication method to its present level, such studies have also provided important insights regarding possible means to facilitate its further advancement.

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