

The Characteristics of Chip-to-Chip Signal Propagation in a Package Suitable for Superconducting Circuits

We have measured the electrical characteristics of chip-to-chip-carrier connectors ideally suited to high-performance Josephson LSI circuits. Self- and mutual inductances between connectors were measured by incorporating the connectors in a dc SQUID (Superconducting Quantum Interference Device) and confirmed by detailed signal delay and crosstalk measurements made with Josephson logic circuits.

Introduction

Josephson logic circuits are interconnected with lossless, matched, superconducting transmission lines [1-4], as they allow the propagation of very fast rise time signals with a minimum of distortion, reflection, and delay. It is desirable to continue these superconducting transmission lines onto the chip carrier for chip-to-chip communication. In order to exploit the advantages of the superconducting transmission lines on both the chip and the carrier, it is necessary to preserve their favorable qualities at the chip-to-carrier interface. Chip-to-carrier connectors (and connector arrays) should therefore have a) a low resistance compared to the transmission line impedance to minimize losses and distortion; b) a low inductance to minimize signal delay and distortion; and c) a small mutual inductance between neighboring connectors to minimize signal crosstalk.

The connector developed to satisfy these conditions was a modified version of the controlled collapse chip solder joint that had been previously developed for bonding and electrical connection of semiconductor chips to ceramic chip carriers [5]. For this experiment it was chosen to arrange the connectors in a single peripheral row on the chip with a center-to-center distance between connectors of 200 μm . They were fabricated by vapor-depositing equal amounts of superconducting solder on the chip and the carrier at each connector site and then reflowing the solder with the chips placed face-downwards to make the

bond. Special stand-offs at the corners of each chip support the chip during bonding and define the final connector height. Thus, each solder joint makes a flat "pancake" connection approximately 30 μm high and 125 μm in diameter sandwiched between the chip and carrier. Using connectors at regular intervals to short together the ground planes of the chip and carrier effectively reduces the single large peripheral array to a number of smaller, electrically independent arrays of connectors. Independent linear arrays of four, six, and eight connectors between ground connectors were investigated. The work reported in this paper was to characterize these chip connectors in terms of their self- and mutual inductances in the various arrays and to measure the high-speed signal transmission and crosstalk characteristics of these connectors.

The carrier used in this experiment consisted of a 25-mm-diameter silicon wafer onto which were mounted four $6.35 \times 6.35\text{-mm}$ chips. The superconducting transmission lines on both the chips and the carrier were Pb-alloy strip lines (superconducting penetration depth $\lambda = 0.119 \mu\text{m} \pm 0.0075 \mu\text{m}$) over niobium ground planes ($\lambda = 0.086 \mu\text{m} \pm 0.005 \mu\text{m}$).

Self- and mutual inductances of chip-to-chip-carrier connectors

In chip-to-chip communication, a fast rise time signal is sent from a Josephson device on one chip through a chip-

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to-carrier connector, onto a transmission line on the carrier, and through a second chip-to-carrier connector to a receiving device on another chip. This signal path is shown schematically in Fig. 1. Because of the inductive discontinuity at the chip-to-carrier interface, the fast rise time signal on the on-chip transmission line is distorted and reflected at the connector site. To minimize these effects, the impedance of the inductive discontinuity can be matched to the transmission lines ($Z_0 = 6.9 \Omega$) by placing capacitors to ground on each side of the connector with a capacitance of $C_{\text{match}} = L/2Z_0^2$. When this is done, the chip-to-carrier connector appears as a segment of an ideal transmission line provided that the time constant of the incoming signal τ_s is long compared to the delay through the connector τ_π :

$$\tau_s \geq 3\tau_\pi = 3\sqrt{LC}, \text{ with } C = 2C_{\text{match}}.$$

The self-inductance of various connectors in different arrays of four, six, and eight connectors per ground was measured by placing the connector in one branch of a two-junction interferometer (dc SQUID) using the experimental technique originally proposed by W. Henkels [6]. A simplified electrical circuit of such an interferometer is shown in Fig. 2(a). A supply current I_G is applied between points b and d of the interferometer while a control current I_C is applied between points a and b. The periodicity of the resulting diffraction pattern [Fig. 2(b)] is determined uniquely by the inductance L_1 through which the control current flows according to the relationship $\Delta I_C = \Phi_0/L_1$, where $\Phi_0 = 2.07 \times 10^{-15}$ Wb, the quantum of magnetic flux. In this case, the inductance L_1 is the self-inductance of the solder connection including contributions due to both connector pads on the chip and carrier, and L_2 , L_3 , and L_4 are inductances associated with the wiring. The connector solder was deposited directly onto a pad made from the ground plane metallurgy (Nb) and therefore the pad was made as an island separated from and surrounded by the ground plane. The connector pad inductance associated with this coplanar waveguide geometry was measured to be 8.0 ± 1.2 pH for both the chip and carrier pads. This adds to the self-inductance but is not coupled to the other connectors and therefore does not add to the mutual inductance.

Two inductance experiments were performed for connectors in the array of eight connectors between grounds. The first experiment measured the self-inductance of the fourth connector in the array of 8 (see Fig. 1), for which a value of $28 \text{ pH} \pm 2 \text{ pH}$ was found once the connector pad inductances had been subtracted. By applying the control current through connectors 5, 6, 7, or 8, rather than number 4, the mutual inductances between these connectors and connector number 4 were measured. A second exper-

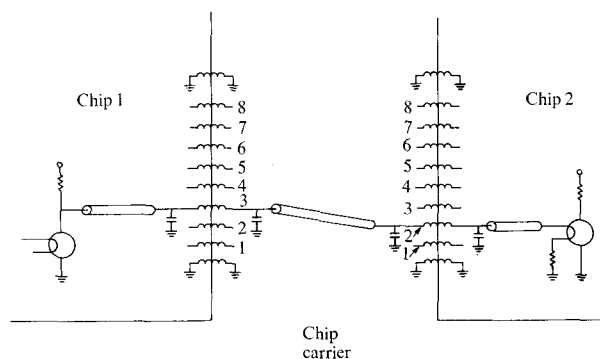


Figure 1 A representation of a chip-to-chip signal path through two sets of chip-to-carrier connectors (represented as lumped inductors). In this example the signal leaves chip 1 through the third connector from the grounded connector and enters chip 2 through the second connector from the grounded connector. The symbol for the Josephson device is taken from Klein and Herrell [4]. Note the use of matching capacitors such that the connector appears as a π -filter.

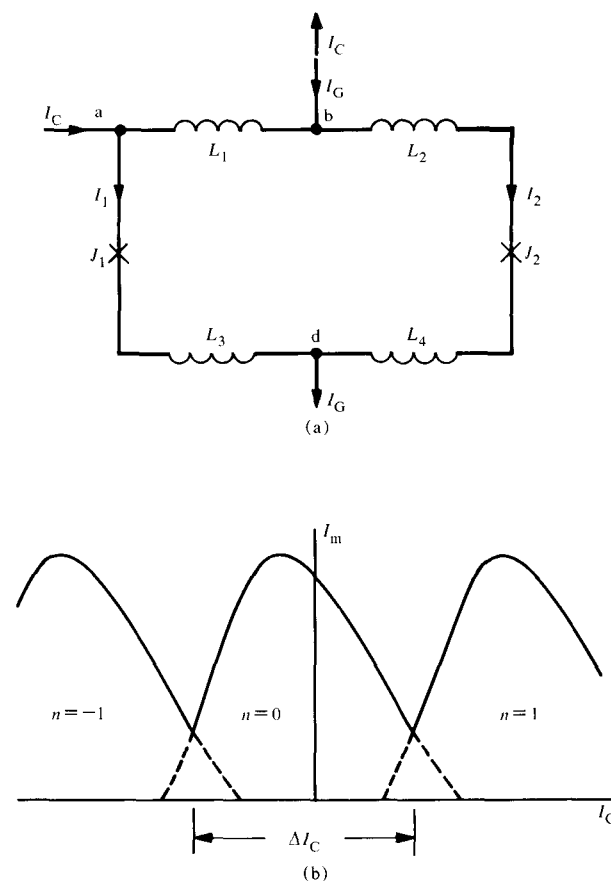


Figure 2 (a) The equivalent circuit of a direct-coupled two-junction interferometer. The supply current I_G is applied between the points b and d and the control current I_C is applied between a and b. (b) A typical threshold curve for a two-junction interferometer where $\Delta I_C = \Phi_0/L_1$.

	1	2	3	4	5	6	7	8
1	13.7	9.3		5.8	4.0	2.0		0.5
2	9.3				7.0			
3					14.5			2.0
4	5.8			27.8	20.0	14.5	7.0	4.0
5	4.0	7.0	14.5	20.0	27.8			5.8
6	2.0			14.5				
7				7.0				9.3
8	0.5		2.0	4.0	5.8		9.3	13.7

Figure 3 The measured inductance matrix for eight connectors between grounds. The diagonal terms are self-inductances and off-diagonal terms are mutual inductances. The self-inductances have an experimental uncertainty of ± 2 pH, primarily due to uncertainties in the pad inductances, whereas the mutuals are accurate to $\pm 2\%$. All values are in picohenries.

	1	2	3	4	5	6
1				5.4		
2				10.7		
3			23.8	16.9	10.7	5.4
4	5.4	10.7	16.9	23.8		
5			10.7			
6			5.4			

	1	2	3	4
1		7.0	6.1	
2	7.0	18.3	12.7	6.1
3	6.1	12.7	18.3	7.0
4		6.1	7.0	

Figure 4 The measured inductance matrices for six and four connectors between grounds. The diagonal terms are self-inductances and off-diagonal terms are mutual inductances. The self-inductances have an experimental uncertainty of ± 2 pH, primarily due to uncertainties in the pad inductances, whereas the mutuals are accurate to $\pm 2\%$. All values are in picohenries.

iment measured the self-inductance of connector number 1 and the mutual inductances between this and four of the seven other connectors. The inductance matrix measured

in this fashion is presented in Fig. 3. Similarly, the inductance matrices for arrays of four and six connectors between grounds were also measured and are shown in Fig. 4.

Using the inductance matrix of Fig. 3, the signal delay and crosstalk of each connector of the array can be calculated. The largest self-inductance for a connector in the array of eight connectors between grounds was measured as 28 ± 2 pH, or a total self-inductance of 44 ± 2 pH when the pad structure inductances are included. The matching capacitors on the chip and the carrier were 1.1 ± 0.25 pF. (It was originally anticipated that the solder height would be $75 \mu\text{m}$ and the total inductance 100 pH, hence C_{match} was chosen as 1 pF.) Using these values we estimate the connector delay τ_π as 10 ± 1.1 ps.

Crosstalk is defined as the transient signal induced in one chip-to-carrier connector due to a signal being applied to an adjacent chip-to-carrier connector. The worst-case crosstalk for each connector in an array is the transient signal induced on that connector due to signals being applied simultaneously to all the other connectors in the array. Noting that the induced voltage V is given by $V = M di/dt$, where M is the mutual inductance, we can estimate the peak amplitude of the crosstalk signal on the j th connector in an array of n mutually coupled connectors as approximately

$$\Delta I_j = \frac{\sum_{i \neq j}^n M_{ij} I_i}{2Z_0 \tau_s} \quad (1)$$

This is done by substituting I_i/τ_s for di/dt , and $V = 2Z_0 \Delta I_j$ since $2Z_0$ is the effective load seen by the j th connector. M_{ij} is the mutual inductance and I_i is the final amplitude of the signal on the i th connector [*i.e.*, $I_i(t) = I_i(1 - e^{-t/\tau_s})$].

For connector 4 in the inductance matrix of Fig. 3, and estimating by linear interpolation M_{42} and M_{43} as 13 pH and 20 pH respectively, we find $\sum M_{ij} = 84.3$ pH, which results in a total worst-case crosstalk ratio $\Delta I_j/I_i$ of 0.17 for simultaneous, 35-ps rise time signals on all of the other connectors. Note that this is the worst-case crosstalk generated by simultaneous signals on all other connectors, and that the maximum single-signal crosstalk between any two connectors can be similarly estimated to be no more than 0.045.

Delay measurement

Noise and trigger jitter of the room-temperature electronics make it difficult to resolve time differences to better than 20 ps, and therefore it was necessary to place at least

Table 1 Components of the measured delay of a signal propagating through 20 connectors.

Delay	Experiment (ps)
τ_{total}	810 ± 20
$\tau_{\text{x-line}}$	595 ± 5
τ_{crossing}	14.3 ± 7
$\tau_{20 \text{ connectors}}$	201 ± 25
$\tau_{\text{connector}}$	10.1 ± 1.3

20 connectors in series in order to accurately measure the average delay. Also, since the rise times of the signals launched out of the dewar are significantly degraded by the cable, it was clear that Josephson devices were necessary to measure the extremely fast waveforms of the interchip propagating signals. Each connector in the series was chosen to be the highest-inductance connector in each of the 20 independent arrays of eight connectors between grounds. The experiment was performed using the layout shown in Figs. 5 and 6. The propagation times of the interconnecting lines were calculated based on the work of Henkels and Kircher [7] together with time domain reflectometry measurements on standard lengths of test lines on both the chips and the carrier. These delays were found to be 13.4 ps/mm on the chip and 9.8 ps/mm on the carrier. In the experimental set-up, a fast rise time signal was launched from the chip by the Josephson interferometer device labeled "pulse generator." This signal is detected by the "start time" device. If this gate is powered (V_1) its time of switching can be measured directly by the voltage step on the output line. The arrival time of the signal after propagating on and off three chips through 20 chip-to-carrier connectors can be detected using the "stop time" interferometer device when this is powered by V_2 . A typical experimental measurement is shown in Fig. 7. Note that with this technique only a single output cable is used from the measurement circuit on the chip to the room-temperature test equipment, avoiding systematic errors due to differences in transmission line lengths and discontinuities to the room-temperature equipment.

There are three contributions to the observed delay:

1. On-chip and carrier transmission line propagation delay ($\tau_{\text{x-line}}$);
2. Chip-to-carrier connector delay ($\tau_{\text{connector}}$);
3. Delay of the signal through the control lines of the detector interferometers (τ_{crossing}).

The crossing delay was determined from separate experiments [4]. The contributions of the various delays to the total observed delay are summarized in Table 1.

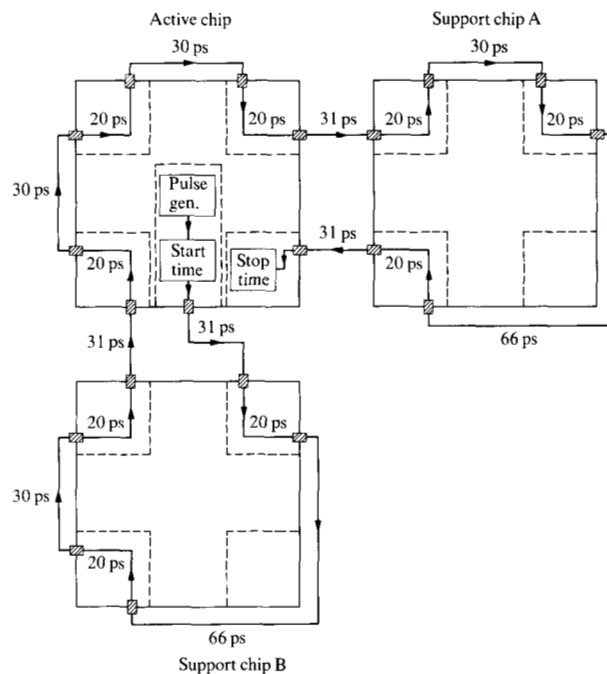


Figure 5 A schematic diagram of the three chips used for the delay experiment. The cross-hatched rectangles are chip-to-carrier connectors and the lines between them are transmission lines. The arrows indicate the direction of signal propagation with the calculated propagation delay of each transmission line segment inserted. There is also a delay on the source chip of 22 ps from the "start time" device to the first chip-to-carrier connector and 20 ps from the last chip-to-carrier connector to the "stop time" device. A summary of the delays is given in Table 1.

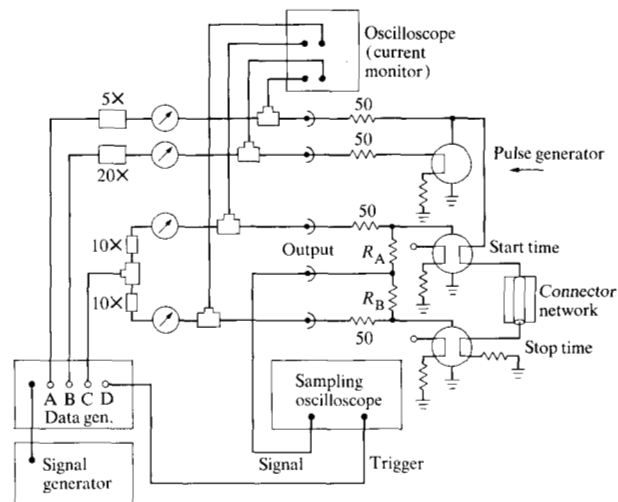


Figure 6 A block diagram of the delay experiment showing the connections to room temperature of the "pulse generator," "start time" and "stop time" devices.

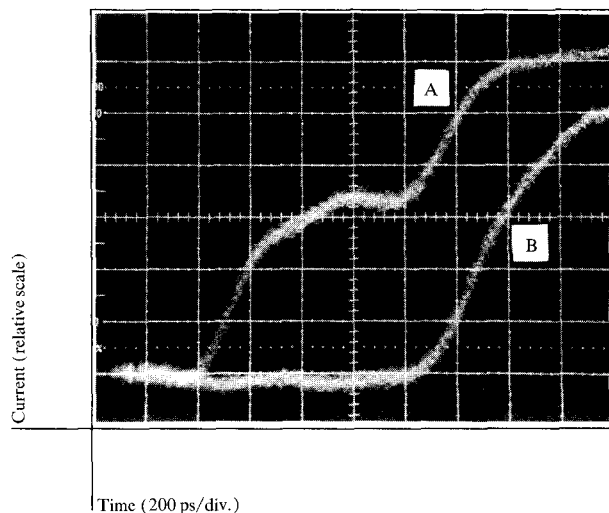


Figure 7 A photograph of the oscilloscope trace showing the superimposed output signals from the "start time" (curve A) and "stop time" (curve B) devices. The distance from the intersection of the tangents to the steeply rising portions of each curve to the base line corresponds to a total delay of 810 ± 20 ps through twenty chip-to-carrier connectors and the associated wiring.

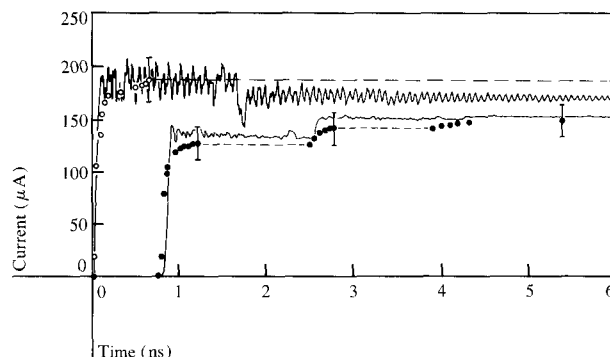


Figure 8 The waveform of the signal from the "pulse generator" before it leaves the source chip and after it has passed through 20 chip-to-carrier connectors as measured by the "start time" device (open circles) and "stop time" device (solid circles). The solid lines are a computer simulation using the ASTAP program [11] of the experiment with the measured device and circuit parameters on these chips and the chip carrier, including the leakage resistance to ground of 45Ω at one of the chip-to-carrier connector pads.

By repeating the previous experiment with varying values of the dc bias on the second control line of the "start time" or "stop time" interferometers in Fig. 6, one can determine both the amplitude and the waveform of the propagating signal at each detector interferometer [8-10]. The reflections and attenuation in this measured signal [Fig. 8] were found to have two causes:

1. A chip-to-carrier connector pad had a leakage resistance to ground of 45Ω ;
2. The terminating resistor was 40% higher than the characteristic impedance of the transmission lines.

More precise measurements, similar to those of Fig. 8, confirmed that the signal waveform was approximately exponential with a time constant τ_s of 35 ps.

Crosstalk

A Josephson circuit driver configuration was designed that enabled simultaneous switching of fast rise time signals through the connectors adjacent to the last connector used in the delay experiment [Fig. 5]. The crosstalk signal produced in this connector could then be measured with the stop time device of Fig. 6. An external trigger signal switched a master interferometer, the output signal of which successively switched seven driver interferometers. The output of each driver interferometer was wired to a chip-to-carrier connector with a delay line such that the signals from all seven drivers arrived simultaneously at the connectors in the array, thereby producing a worst-case crosstalk condition. The amplitude of the induced signal was then determined in exactly the same manner as was done in the delay experiment.

In the experiment only five of the seven driver interferometers were fired. In Fig. 3, row 4, the connectors associated with columns 1, 2, 3, 5, and 6 were driven, with connector 4 as the crosstalk connector. For a nominal gate supply current of $230 \mu\text{A}$ and a device-switched output of $190 \mu\text{A}$ with a rise time $\tau_s \approx 35$ ps, the experimental crosstalk signal from connector 4 was measured as $22 \pm 3 \mu\text{A}$. This compares favorably with the simulated control line transient amplitude of $29 \mu\text{A}$ and an estimated crosstalk of $28 \mu\text{A}$ based on Eq. (1) with

$$\sum M_{ij} = \sum_{i \neq j}^{n=6} M_{ij}, \text{ where } j = 4 \text{ (refer to Fig. 3).}$$

The difference between the experimental and estimated results derives mainly from a time skew between the driver signals arriving at the connectors caused by variations in the device characteristics of the driver interferometers. A worst-case skew of 40 ps was anticipated in the present experiment. Under these conditions the simulated (using ASTAP [11]) crosstalk was found to drop from $29 \mu\text{A}$ to $18 \mu\text{A}$, thereby bracketing the experimentally measured crosstalk of $22 \pm 3 \mu\text{A}$.

Conclusion

The electrical characteristics of arrays of four, six, and eight signal chip-to-carrier connectors between ground connectors were measured. The self- and mutual inductance measurements on these connectors were made by

placing the unknown inductance in one branch of a two-junction interferometer (dc SQUID). For the connector dimensions and spacing used in this experiment, the largest measured self-inductance was 28 ± 2 pH for a chip-to-carrier connector with an additional 8.0 ± 1.2 pH per connector pad due to the associated wiring. The high-speed signal transmission and crosstalk measurements on these connectors were made using Josephson logic circuits as signal generators and detectors. A worst-case delay of 10.1 ± 1.2 ps per connector was measured for a fast rise time signal propagating through 20 connectors in series. A worst-case crosstalk of 12% was measured in an array of eight connectors per ground when five fast rise time signals arrived approximately simultaneously at the connector site. These results were found to be in excellent agreement with simulations and indicate that connectors of this type are a suitable interface between the chips and chip-carrier in applications of the Josephson LSI technology. Although the measurement techniques used in this work are specific to Josephson technology and superconductivity, the results obtained can be applied to similar connector arrays used in semiconductor circuits, and to our knowledge this is the first time that the self- and mutual inductances of such connectors have been directly measured.

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The authors are located at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598.