P. Guéret
A. Moser
P. Wolf

# Investigations for a Josephson Computer Main Memory with Single-Flux-Quantum Cells

*The paper first summarizes requirements for a main memory with Josephson junctions and reviews the work carried out on an experimental main memory model containing an array of single-flux-quantum cells, line drivers, and address decoders with a total of nearly 4500 Josephson junctions. In the second part, theoretical and experimental investigations on the y drive system, including sense circuit, are presented. The investigations deal with both the read and write phases. Finally, the on-chip logic circuits and the address decoders are discussed, and the experimental results presented. Drivers and decoders based on the principle of current steering in superconducting loops are intended to be used on a fully populated main-memory chip.*

## 1. Introduction

For a hypothetical main frame capable of executing 70 million instructions per second, a main RAM capacity of 16 megabytes on 10 000 memory and support chips would be adequate [1]. With a 16K-bit chip, on-chip access time would be about 15 ns with a power consumption per chip of 40 $\mu$W, excluding power supply. Estimated access time and power consumption of the 16-megabyte main RAM on 20 double boards are then 20 ns and 4.8 W, respectively.

These estimates are based on a feasibility study of a 16K-bit RAM chip using Josephson junctions. An experimental memory model was fabricated and tested to study the 16K-bit chip. Nearly 4500 Josephson junctions are used in the model, which includes array, line drivers, and address decoders. The arrangement, on a (6.35 × 6.35)-mm$^2$ chip, is shown in Fig. 1. Power dissipation of an unselected chip is zero; for a read/write cycle time of 30 ns, it is about 10 $\mu$W. Experimental results and a detailed description of the whole memory model are given elsewhere [2]. Basic technological aspects of Josephson device and circuit fabrication are given by R. F. Broom, R. Jaggi, Th. O. Mohr, and A. Oosenbrug in this issue [3].

In this paper, we first give a short overview of the experimental memory model. We focus some attention on the memory cell, because its characteristics and tolerance requirements determine closely the drive systems and the address decoders.

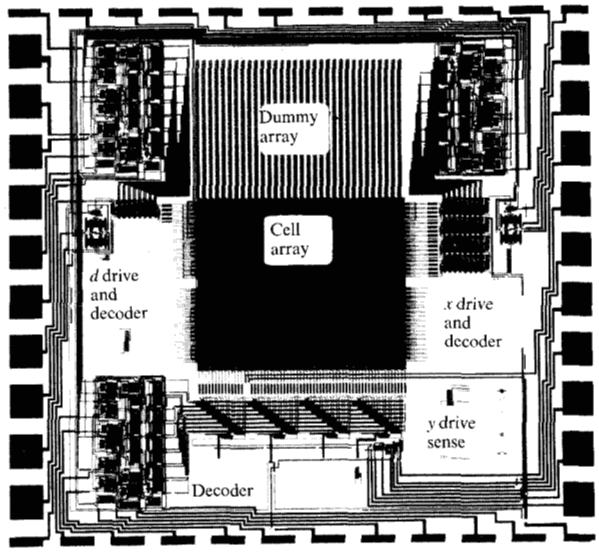


**Figure 1** Photograph of an experimental memory model. It consists of an array with 2048 SFQ cells, part of the drivers and decoders. The model contains ≈4500 Josephson junctions. Measured access time was ≈10 ns. (Reprinted with permission of the *IEEE Journal of Solid-State Circuits* from the article "Model for a 15-ns 16-K RAM with Josephson Junctions" by R. F. Broom *et al.*)

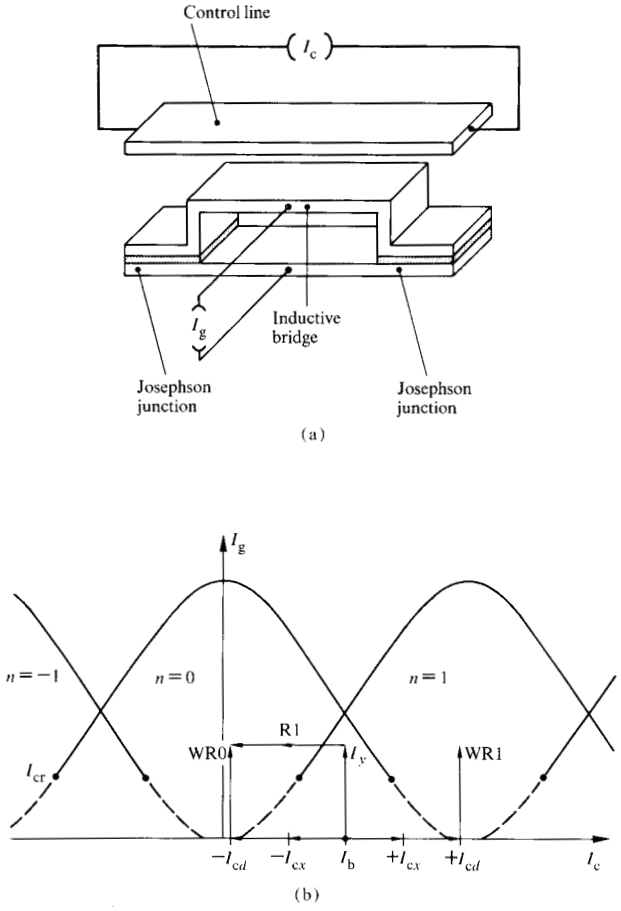


**Figure 2** SFQ cell and its electrical characteristics. (a) The cell consists of two Josephson junctions and a bridge-like inductance. (b) The characteristic consists of bell-shaped superconducting states, the vortex modes. Indicated is the triple coincidence addressing scheme. It uses a $y$ current through the cell and two currents in an $x$ and a diagonal ($d$) control line.

Power consumption of the on-chip peripheral circuits, such as drivers and decoders, is critical. For instance, the ac-powered Josephson circuits with terminated outputs used for high-speed logic have too high power requirements for a main memory. Fortunately, another class of circuits based on current steering in superconducting loops has been utilized in our designs. The lower power is obtained at the expense of speed, which, however, is still adequate for main memory applications.

The $y$ drive system, which demonstrates that the principle of current steering works in quite good agreement with circuit modeling of large circuit blocks, is described in the second part of the paper. The model in the $y$ direction was designed to be very similar to a 16K-bit chip, including its transient behavior.

In the third part of the paper, the address decoder design is presented and compared with experimental results. The decoders in the model are as required on a final chip.

## 2. Overview of memory model

All known Josephson cells store information as magnetic flux in a superconducting loop. The magnetic flux is quantized as a multiple of the flux quantum $\phi_0 = h/2e = 2.07 \cdot 10^{-15}$ Wb. Intuitively, cells that store information as single flux quanta would be expected to be optimal with respect to size and power. This has indeed turned out to be true so far; therefore, single-flux-quantum (SFQ) cells have been used throughout our main memory investigations.

An SFQ cell and its electrical characteristics are shown in Fig. 2. Basically, it is a two-junction Josephson interferometer [4, 5] with an $LI_0$ product of about half a flux quantum $\phi_0$. Here, $L$ and $I_0$ denote the interferometer inductance and the maximum Josephson currents of the junctions, respectively. Under these circumstances the bell-shaped superconducting quantum states, the so-called vortex modes, overlap. In the overlap region the device is bistable, as is required to store one binary bit of information [6, 7]. For reading and writing, use is made of two distinct vortex switching transitions [8, 9], which depend on whether a vortex mode is traversed below or above a critical value $I_{cr}$ of the gate current $I_g$. If the mode is crossed below $I_{cr}$, then switching to another vortex mode occurs. This transition is used for writing. If the mode is crossed above $I_{cr}$, then switching to the voltage state takes place, which is used for reading.

Some general properties of such cells are worth mentioning. In the storing state, the cell consumes no power because it is superconducting. The stored energy $E \approx I_0 \cdot \phi_0$ is about $10^{-18}$ joule. Power is consumed only during reading and writing, when a cell changes its vortex state, and amounts to a fraction of a nanowatt. Reading is destructive; therefore, the information has to be rewritten after a read operation.

Good current margins are obtained with the addressing scheme in Fig. 2(b), which uses the triple coincidence of the current $I_y$, a control current $I_{cx}$ in the $x$ direction of the array, and a control current $I_{cd}$ in a diagonal ($d$) direction of the array. The 1500-$\mu$m$^2$ cell is operated by applying $I_{cd}$ simultaneously with and having the same polarity and amplitude as $I_{cx}$.

In the memory model (Fig. 1), the cells in the $y$ direction are electrically connected in series to form 32 strings. The array consists primarily of two parts. The lower half

is populated with 2048 SFQ cells in a 32 × 64 arrangement. The upper half contains 2048 dummy cells which extend the array to a vertical dimension anticipated in a 16K-bit memory. In the $x$ direction, there are 64 lines on top of the cells to act as control lines. An additional 64 cell control lines are wired through the array in a diagonal ($d$) direction.

In the model the complete $y$ driver is provided. Its outputs are connected to the 32 strings of cells. The $x$ and $d$ drivers with 32 and 8 outputs, respectively, are only partially implemented. Both drivers have to deliver bipolar currents, which is accomplished by polarity switches. The external addresses select the appropriate drive gates via three-bit to eight-bit decoders.

All the functional blocks in the memory model are based on the current-steered superconducting loop approach [10]. Its basic circuit is shown in Fig. 3. It has two superconducting branches, one with a set, the other with a reset junction. The circuit is powered by a dc current $I_g$ which is initially assumed to flow in the set branch. If a current is applied to one or the other control line of the set junction, it switches to the voltage state and current $I_g$ is transferred into the output branch, which, for example, might be an address line in the memory array. Current $I_g$ stays there even if the control current to the set junction is switched off. To retransfer $I_g$, the reset junction has to be switched by applying a current to its control line.

Approximate expressions for the transfer times and the energy stored in the circuit are also given in Fig. 3. Fabricated drive and logic circuits have current transfer times between 0.3 and 5 ns.

In the quiescent state the loop circuits are superconducting and consume no power. During switching the stored energy $E$ is dissipated in one of the junctions. This leads to a transient power dissipation on the order of microwatts for fabricated circuits at their nominal repetition rates of 10 to 100 MHz.

The SFQ cells demand quite precise drive currents. If, for instance, the maximum Josephson current of the interferometer junction varies ±15%, then margins of ±6% for the $y$ current and of ±30% for the $x$ and $d$ currents can be allowed. The tolerance for the maximum Josephson current appears to be tight, but statistical investigations on small arrays of cells have shown that their use is feasible [11]. Thus, the supply current $I_g$ to the drive circuits must be carefully regulated, which poses no problem because it is a dc current from an external supply. Also, the current transfer from one branch of the loop circuit to another has to be as complete as possible. One method to accomplish

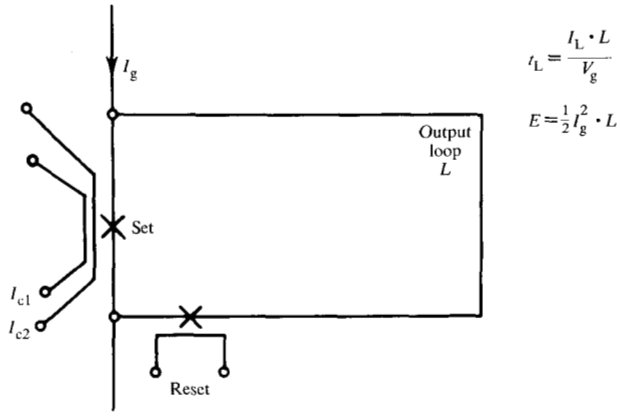


**Figure 3** Current steering in superconducting loops. The arrangement consists of two branches, one with a set, the other with a reset junction. The output branch, for instance, could be an address line in a memory array. The circuit is powered by a dc current $I_g$.

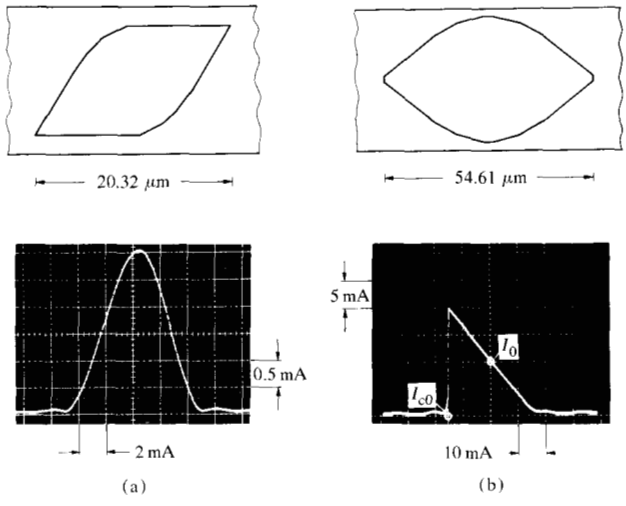


**Figure 4** Junctions with sine-shaped areas. Note the strongly suppressed side lobes in the oscillograms. Junction (a) is used in array drivers and junction (b) for logic circuits.

this is to avoid superconducting leakage $I_r$ in the switched branch by using Josephson junctions with special shapes so that, when a control current is applied, the Josephson current is well suppressed. Two examples of junctions for drive and logic applications are shown in Fig. 4. With the approximately sine-shaped junction, the side lobes of the control characteristics are quite small, ≈2% of the zero-field maximum Josephson current, well within the re-

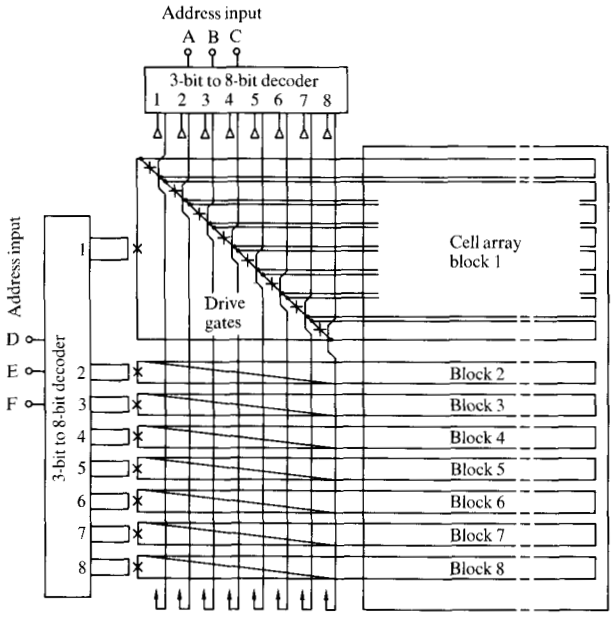


**Figure 5** The $y$ drive system with the $y$ address decoders. The $y$ drive gates are arranged in blocks of eight. Accordingly, addressing 64 array loops requires two 3-bit to 8-bit decoders.

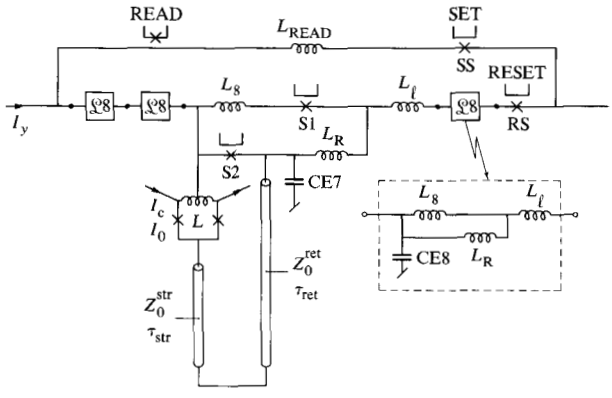


**Figure 6** Equivalent circuit model for the $y$ drive system of the experimental memory model.

quirements. Investigations of shaped gates are reported in [12]. Memory drivers have been realized using junctions like those in Fig. 4(a). (The $y$ drive network is described in the next section.) Logic functions, like inverters, AND's, and OR's as required for decoders and memory control logic, have been realized with the large junctions shown in Fig. 4(b) and described in [13]. Address decoders built with them are discussed later in this paper.

## 3. The y drive system

On a 16K-bit SFQ chip design, the cells would be arranged in a 64- × 256-cell array, due to the physical cell dimensions. A $y$ line would then consist of 256 series-connected SFQ cells. Each $y$ line would be provided with a drive gate having a characteristic similar to that in Fig. 4(a). The array drivers would be arranged in blocks of eight junctions, thus forming a partial decoder as shown in Fig. 5 for the 64-cell strings in the $x$ direction. Accordingly, addressing one string in the $x$ direction requires two three-bit to eight-bit address decoders. In principle, the same is true for addressing an $x$ or $d$ line but, in addition, one two-bit to four-bit address decoder is then necessary.

The junctions with an approximate sine shape allow quite precise control of the array currents, which is necessary because of the aforementioned tolerance requirements of the SFQ cells.

For the current density of 2200 A/cm$^2$ used in the memory model, the array drivers have to provide currents of about 2–3 mA with a current transfer efficiency of ≈98% [2]. This and other requirements lead to a relatively short junction of about 20 $\mu$m. Under these circumstances, the field required to suppress the Josephson current is rather high. To obtain acceptable control currents provided by the control logic or address decoders, the driver control line is wound three times over the junction. With three windings, a control current $I_c \geq 7$ mA is sufficient to suppress the Josephson current to less than 2% of its value at $I_c \geq 0$, as shown in Fig. 4(a).

In our memory model, each $y$ line contains 64 SFQ cells plus 64 dummy cells and has in addition its own return line. The 32 strings are collected into four drive gate blocks each having eight drivers. To select a block, four block selector drive gates are required, which in our model are connected directly to the chip pads. Furthermore, a set and a reset gate are attached to the driver for setting up and resetting the dc $y$ current in the strings. Reading is performed through the $y$ driver; accordingly, a read gate is provided. It is a logic junction with the threshold characteristic shown in Fig. 4(b).

Operation of the $y$ driver is as follows. First, the decoder and the block selector gate are activated, which brings the block selector gate and one drive gate in the block to the resistive state. In this way, a $y$ line is selected. Then the set gate is fired, which transfers the dc supply current into the selected $y$ line. If during a read operation, a cell in the selected $y$ line switches to the voltage state (READ 1), then the current is re-transferred and now flows through the control line of the read gate. If the cell does not switch (READ 0), then the current stays in the $y$ line. In this way, a 1 and 0 can be distinguished from

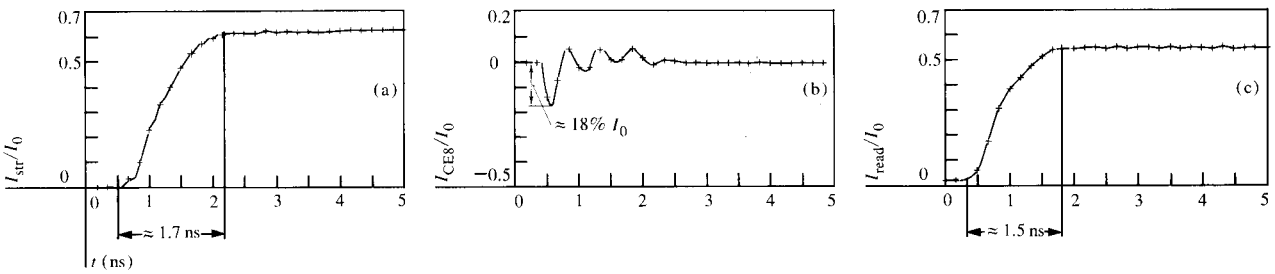


**Figure 7** Computed currents in the *y* drive system with (a) string current during the set phase, (b) string disturb current as a total of the remaining seven unselected strings of the drive block during the set phase, and (c) computed re-transferred current in the read loop during the read phase.

each other. Finally, the reset gate is fired and re-transfers the current out of the array. The decoder and block selector gate are then switched off.

• *Equivalent circuit for y driver and array simulations*

Operation of the *y* driver and array was simulated extensively. To limit CPU time, however, a number of simplifications were introduced into the model. The equivalent circuit used is shown in Fig. 6.

Among the four eight-string blocks, three were replaced by macro circuit $\mathscr{L}8$ in Fig. 6. In this macro circuit, CE8 is the equivalent capacitance of the eight strings in the block, an adequate representation for a group of strings which are not addressed. Inductances $L_R$ and $L_8$ are those of the subloops, as shown.

One string and its return line were modeled in all details to investigate current transfer in or out of a string. The string has a characteristic impedance $Z_0^{str}$ and a delay $\tau_{str}$. Similarly, the return line is characterized by $Z_0^{ret}$ and $\tau_{ret}$.

An SFQ cell was also introduced into this string to investigate the read process. Two set junctions S1 and S2 were also provided in this block for addressing the string. The other seven strings in the block are modeled by their equivalent capacitance CE7.

All blocks are separated by inductance $L_\ell$. The whole array is shunted by the read loop modeled by its inductance $L_{READ}$. This loop also contains a set junction SS and a reset junction RS. All set and reset junctions (S1, S2, SS, SR) are modeled as point junctions which can be switched off so that their maximum Josephson current is 2% of the zero-field value $I_0$ = 2.8 mA. The nominal dc supply current $I_y$ in the simulations was chosen to be about 1.9 mA.

*SET phase*

With bias current $I_y$ initially flowing through the read loop, the set junctions SS, S1, and S2 are switched off. As a result, current $I_y$ is transferred into the string (*y* line). Figure 7(a) shows the string current *vs* time. The transfer is achieved in about 1.7 ns, with 89% of $I_y$ being transferred. Figure 7(b) shows the current flowing in one of the capacitors, CE8. This current, which is the sum of the disturb currents flowing in eight parallel strings, is seen to be less than 18% of $I_0$ and is therefore easily tolerable.

*READ phase*

With current $I_y$ initially in the string, control current $I_c$ is applied to the SFQ cell so as to make it switch into the voltage state. During this phase, S1 and S2 remain switched off by the corresponding address currents. Switching of the cell forces the string current to transfer out of the string into the read loop. Figure 7(c) shows the current in the read loop during this phase. The transfer is achieved in about 1.5 ns, with 84% of the string current being transferred into the read loop to activate the read junction.

With respect to dynamics, the *y* drive system has to be designed rather carefully [14]. By the proper choice of all line impedances, it is possible to avoid current overshoots in the string selected and leakage spikes in nonselected ones. Either of these can destroy information in nonaddressed cells.

• *Experimental results with the y drive system*

To allow individual testing of various parts of the memory model, a form of master-slice approach was adopted. One out of six final masks determines which parts are connected to each other and to the 44 chip pads by the top metallization layer.

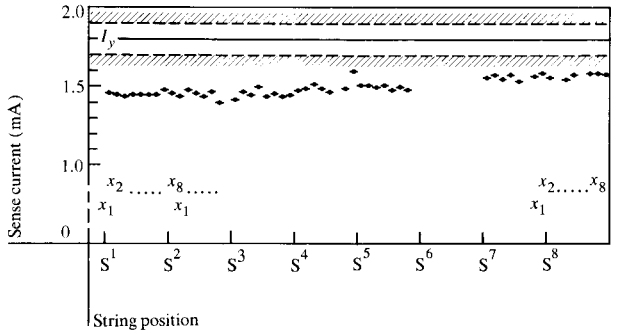


**Figure 8** Operation of the $y$ driver in the read mode. Full circles are the read currents of the 64 accessible cells, as measured with the read gate. Here $x_1$ to $x_8$ indicate the corresponding $x$ control lines of the drive blocks. The variation of the read current is small and is within ±6%. Re-transfer of the string current is around 83%, in agreement with computer simulations.

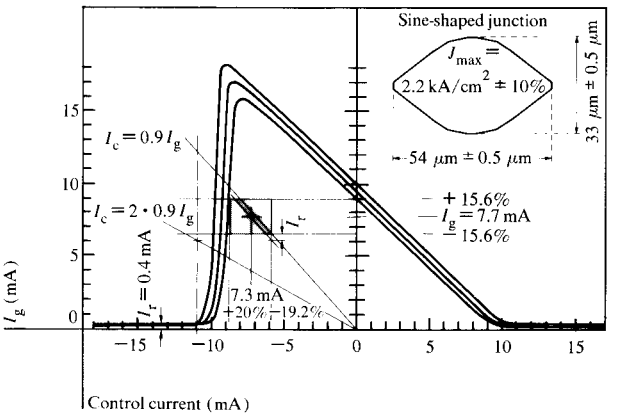


**Figure 9** Threshold characteristic and its spread of a sine-shaped, long, in-line junction for tolerances as indicated. Using the junction as a two-input AND gate, the operating window becomes $I_g$ = 7.7 mA ± 15.6%, $I_c \approx$ 7.3 mA ± 19%.

To test re-transfer of the string current to the read gate during the read phase, the final chip version was chosen, where all the parts, array, drivers, and decoders are connected together. Owing to pad limitations, however, only 64 cells are accessible in this version.

The measured $y$ operating currents are shown in Fig. 8. The 64 accessible cells operate properly as long as the dc supply current $I_y$ = 1.8 mA does not vary more than ±5.6%. We assumed a variance of ±2%. The re-transferred read current as measured at the read gate is 1.5 mA ± 6%. Evidently, the read current is about 83% of dc supply current $I_y$, in agreement with computer simulations [Fig. 7(c)].

A systematic increase of the sense current is visible from the left to the right side of the array. Furthermore, one string of the test array was not operable due to a failure of either the corresponding $y$ drive gate or of the decoder output. However, all other drivers and their decoders worked properly.

## 4. Address decoders

As already mentioned, logic circuits are based on the principle of current-steered superconducting loops. For a fan-out of three, their output loop inductance is about 80 pH, resulting in a current transfer time of $t_t$ = 260 ps, sufficient for the peripheral logic circuits of the main memory chip.

• *On-chip logic for decoder design*

The on-chip logic gates have to deliver control currents of ≈7 mA for the drivers. To include sufficient worst-case margins for the dc gate current, a nominal value $I_0$ = 9.5 mA was chosen for the logic junctions. An additional important requirement for logic gate design is that the junctions be controlled by currents $I_c$ equal to or smaller than maximum junction current $I_0$. This ensures that logic gates can be cascaded (logic gain >1). To achieve sufficient logic gain, a long Josephson junction ($\ell > 40$ μm) should be used. With the junction located on a ground plane, the threshold characteristic for long junctions becomes asymmetric. The resulting well-known experimental characteristic of such a junction is shown in Fig. 4(b). The asymmetric characteristic, with the well-suppressed side lobes of the sine-shaped junctions, provides good logic gain and permits logic fan-in with multiple control lines [13]. Figure 9 represents the simulated nominal and worst-case threshold characteristics of the long in-line junction ($\ell$ = 54 μm). Included in the figure is the operating window for a two-input AND function, illustrating the feasibility of such an approach.

The logic junctions are incorporated in self-resetting, current-steered superconducting loop circuits. Figure 10(a) illustrates a self-resetting inverter circuit with the idealized threshold characteristics of the set and reset junctions. The dc current biases the reset junction outside its superconducting main lobe (point BR), whereas the set junction is still within it (point BS). Accordingly, gate current $I_g$ flows through the complement branch with the superconducting set junction.

An additional input-signal control line is wound once over both junctions in such a way that signal and bias add

over the set junction but subtract over the reset junction. The leading edge of an input signal first biases the reset junction back into the main lobe and subsequently traverses the main-lobe boundary of the set junction, which switches into the voltage state and transfers all current $I_g$ into the true branch with the reset junction. At the trailing edge of the signal, the situation is reversed, and the reset junction switches, which transfers the current $I_g$ back into the complement branch. With the same principle, a two-input OR [Fig. 10(b)] or a partially self-resetting two-input AND [Fig. 10(c)] can be built.

• *Address decoder design*

As described in the previous section, the array drivers are arranged in blocks of eight junctions, thus forming a partial decoder (Fig. 5). Accordingly, addressing one array line requires two three-bit to eight-bit address decoders. Except for the output stage [2], $x$, $d$, and $y$ decoders are equivalent.

The decoder designs are based on the loop circuit principle previously described. The three address bits A, B, and C are picked up by address input latches, each of which controls two flip-flops, one providing the truth and the other the complement of one address, as shown in Fig. 11. In a second stage containing two input AND gates, the A-B address information is combined to $\bar{A} \cdot \bar{B}$, $A \cdot \bar{B}$, $\bar{A} \cdot B$, or $A \cdot B$. In a third stage, the A-B combinations are, in addition, combined with the C address to form $\bar{A} \cdot \bar{B} \cdot \bar{C}$, $A \cdot \bar{B} \cdot \bar{C}$, $\cdots$, $\bar{A} \cdot B \cdot C$, or $A \cdot B \cdot C$.

The address control lines of the input latches have six windings which transform the address currents of 1.2 mA to levels sufficient for operation of the latches. Except for the flip-flop, all other circuits are designed with self-resetting, two-input AND gates. An address-enable pulse sets and resets the address latches. The true and complement flip-flops are controlled by a set and a reset pulse. The A and C address flip-flops can be reset immediately after switch-off of the address-enable pulse. The B address flip-flops reset the AND gates of the second and third stages, and with them the output loops.

Each three-bit to eight-bit decoder contains 42 junctions. All the circuits, input latches, address flip-flops, and AND gates are series connected so that only one supply for the current $I_g \approx 7.5$ mA is required. A second supply of $\approx$7.0 mA is required for appropriate dc biasing. A summary of the design is given in Table 1.

• *Circuit layout*

Owing to the strong nonlinearity of the Josephson effect and the nonuniform junction shape of the logic junctions, an analysis of the circuit dynamics was carried out numerically by computer simulations using ASTAP [15]. To include control by the magnetic field, a distributed junction model had to be used [12]. Simulations of the loop circuit shown in Fig. 3 yield an equivalent transfer time of $t_L = 3.2 \cdot L_{OUT}$ (ps/pH), a value which is close to that given by the expression in Fig. 3. To avoid signal overshoot [16], *e.g.*, $I_{OUT} > I_g$, the circuit should be loaded with $L_{OUT}$

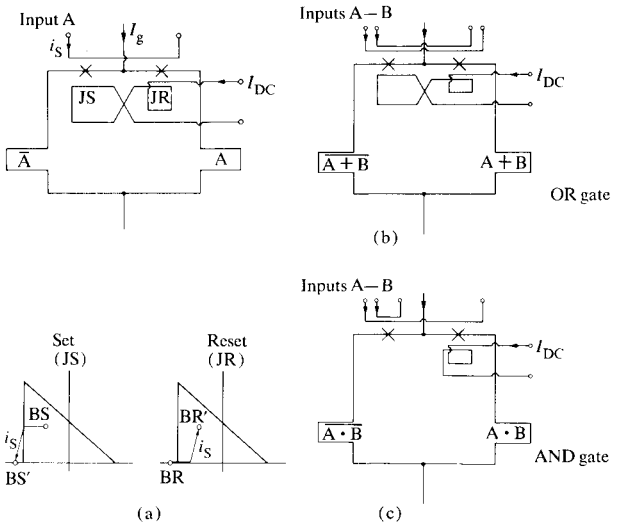


**Figure 10** Current-steered superconducting loop logic circuits. Input signals together with the dc biasing perform self-resetting operation. (a) Inverter circuit; (b) two-input OR; and (c) two-input AND gate.

**Table 1** Decoder design summary.

| | |
|---|---|
| *Basic circuits* | |
| 3 | Address latches |
| 6 | Address flip-flops |
| 12 | Self-resetting two-input AND's |
| Real estate | $0.76 \times 1.37$ mm$^2$ |
| *Design/operating parameters* | |
| Junction type | Sine shape<br>Max. current density = 2.2 kA/cm$^2$ ± 10% |
| Operating currents | $I_g$ (dc) = 7.7 mA ± 5%<br>$I_c$ (dc) = 7.3 mA ± 5%<br>Address input = 1.2 mA (nom.)<br>Decoder output = 7.3 mA (nom.) |
| Decoder delay | Internal ≈ 1.1 ns<br>Output transfer ≈ 3.3 ns/nH |

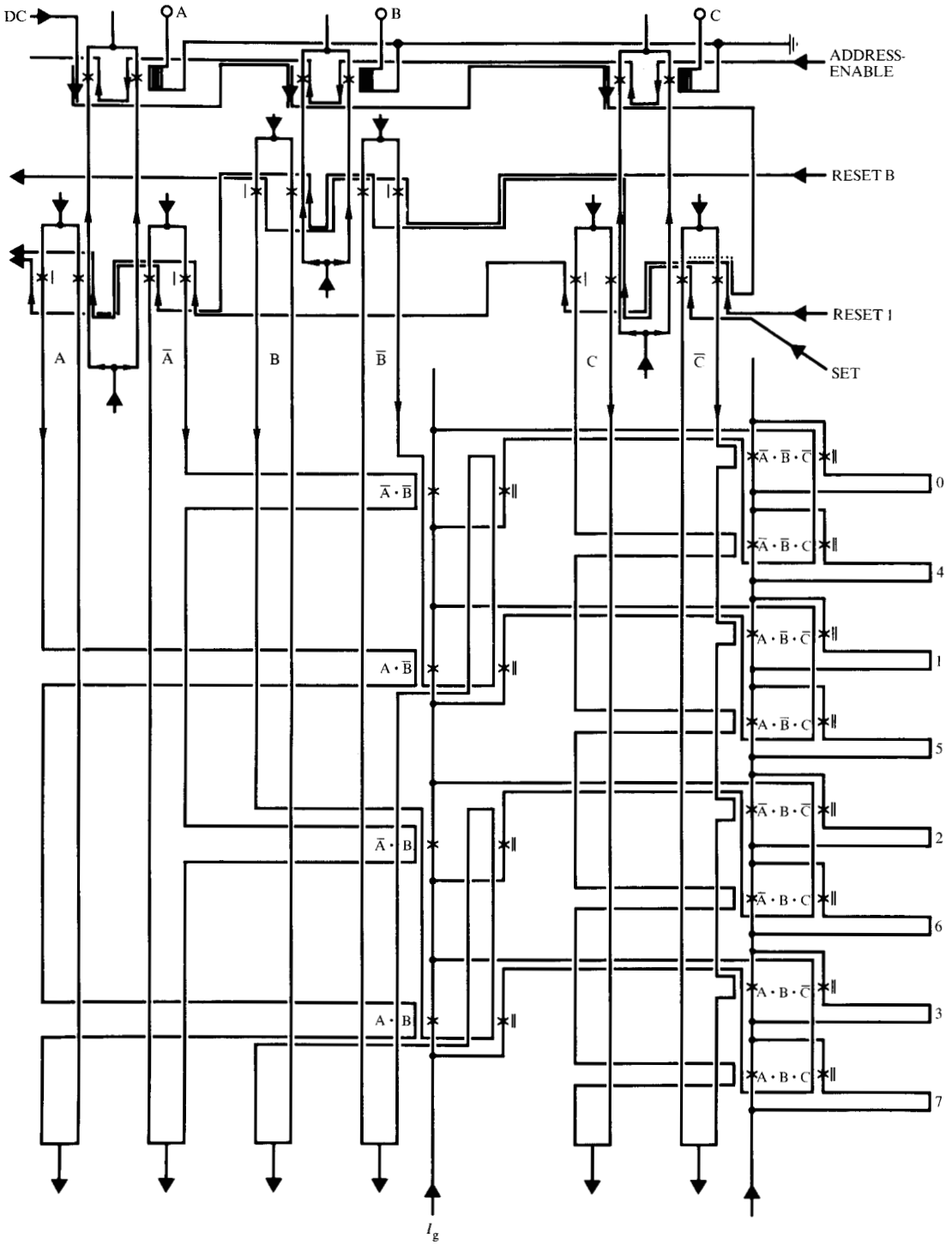


**Figure 11** Schematic diagram of the 3-bit to 8-bit address decoder. The arrows on the gate bias lines indicate the series connection of all the circuits in the diagram. The dots in the dc control line indicate that the line is fed to all remaining junctions marked with one or two side bars.

$\geq L_C = 80$ pH, yielding a minimum delay per stage $t_t = 3.2 \cdot L_C = 260$ ps. In the quiescent state, the loop circuits consume no power. However, during switching, the inductive energy dissipated in the switching junction is $E = 0.5\, L_{OUT} \cdot I_{OUT}^2$; for $L_{OUT} = L_C$, this amounts to $E \approx 2.2 \cdot 10^{-15}$ joule.

Loop length, delay, and fan-out are interrelated. For our technology, with a minimum line width of 2.5 $\mu$m and for the minimal inductance $L_C$ = 80 pH, the shortest allowable output loop length becomes ≈330 $\mu$m [13]. The overall junction length of the logic gates is 100 $\mu$m. Accordingly, for minimum loop length, the maximum fan-out capability of the control logic circuits is three. However, in case of larger fan-out requirements, such as in stages two and three of the decoder, the loop length has to be increased. Due to the size of the junctions, an increase in the inductance can be avoided by increasing control line width $w$.

The whole decoder was simulated with ASTAP; the results are shown in Fig. 12. The signals marked ADD.FF are actually the three output signals of the address flip-flops. A-B LOOP is the output signal of the AND gate processing the A-B address combination. OUTPUT LOOP is the output signal of the AND gate, processing the (A-B)-C address combination. Evidently, in Fig. 12 the three logic stages of the decoder are represented. The overall delay is nominally $t_D$ = 1.06 ns. The worst-case variance, not shown in the figure, is found to be approximately ±10%.

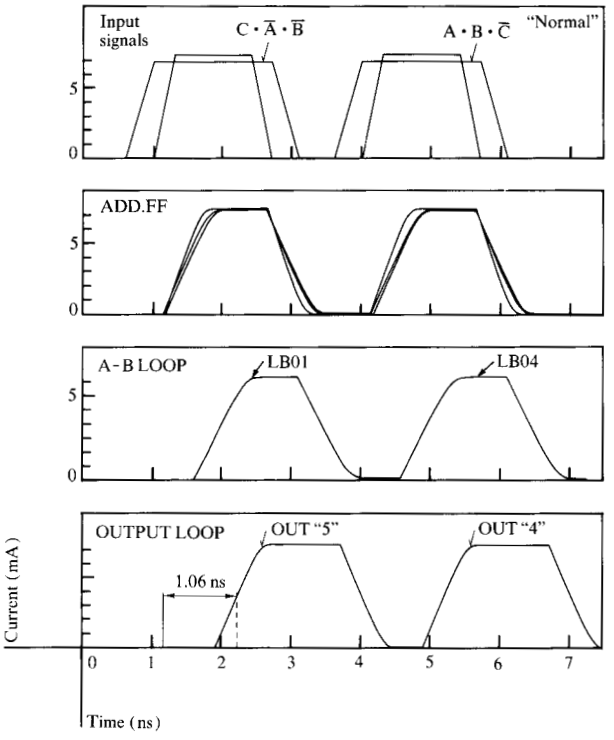


**Figure 12** Dynamic simulation of the decoder design shown in Fig. 11.

### *Experimental results*

The decoders are incorporated as functional blocks into the $y$, $x$, and $d$ drive systems of the experimental SFQ memory model [2]. Consequently, the output inductances are determined by the control lines of the array driver junctions. In the case of the $y$ drive system, Fig. 13, the total drive line inductance is 1.1 nH. To allow individual testing of current transfer in the different output loops of the decoder, six test junctions are incorporated into drive control loops 2 to 7. For high-speed testing, two additional test junctions are located close to the $y$ decoder, allowing the output loop inductance $L_{OUT}$ ≈ 180 pH for outputs one and eight. The test junctions are collected in pairs via the gate current line. Additional control lines are arranged in such a way that each junction can be controlled individually.

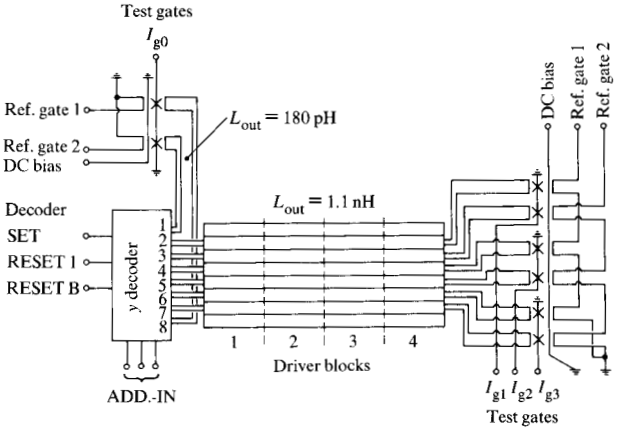


**Figure 13** Circuit diagram of the $y$ decoder connected to the four blocks of $y$ drive junctions and to test junctions. Two test junctions are located close to the decoder to allow low output inductance for decoder outputs 1 and 8.

The decoder tested and described below has a current density somewhat higher than assumed in the design (2.4 kA/cm$^2$ instead of 2.2 kA/cm$^2$). The dc supply currents required to operate the circuits are, therefore, $I_g$ = 8.35 mA and, for dc biasing, $I_{c(DC)}$ = 8.0 mA. Decoder operation at slow repetition rate is shown in Fig. 14. The top oscillogram illustrates the address input combination with the address enable pulse. Only three different address combinations are shown, namely, A · B̄ · C̄, Ā · B · C, and A · B · C. The bottom oscillogram shows the decoder timing signals at the top with SET, RESET 1, and RESET B, as well as the pulsed gate current of the test gates. Below, the switching voltages of ≈2 mV across the test gates of corresponding outputs are illustrated. For perfect operation of all input address combinations, gate current variance of $\Delta I_g$ = ±7.5% is allowed, which is well above the specification of $\Delta I_g$ = ±2%.

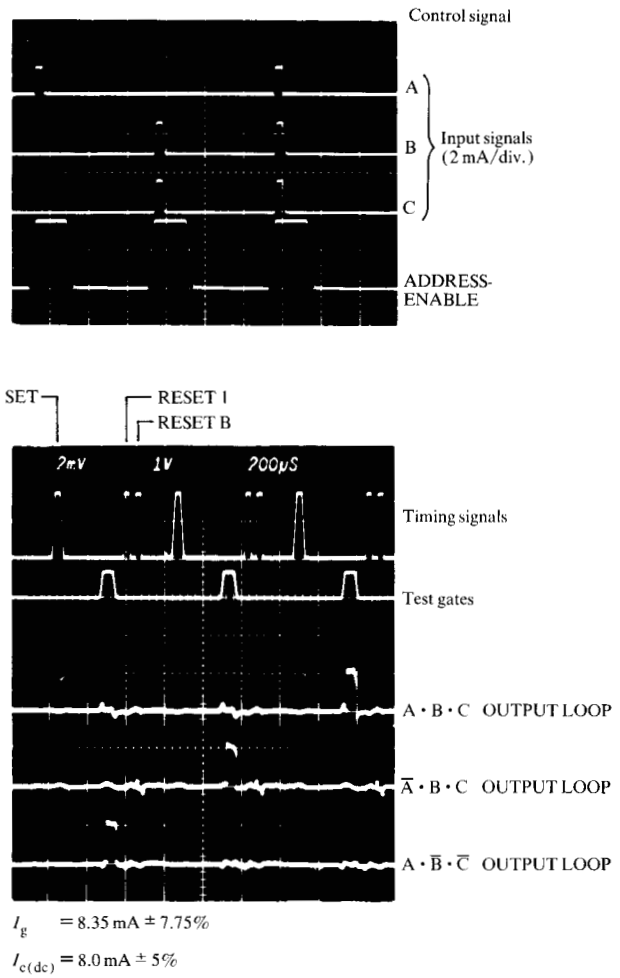


**Figure 14** Decoder operation at slow repetition rate. Illustrated is the operation for the three address bit combinations A · B̄ · C̄, Ā · B · C, and A · B · C.

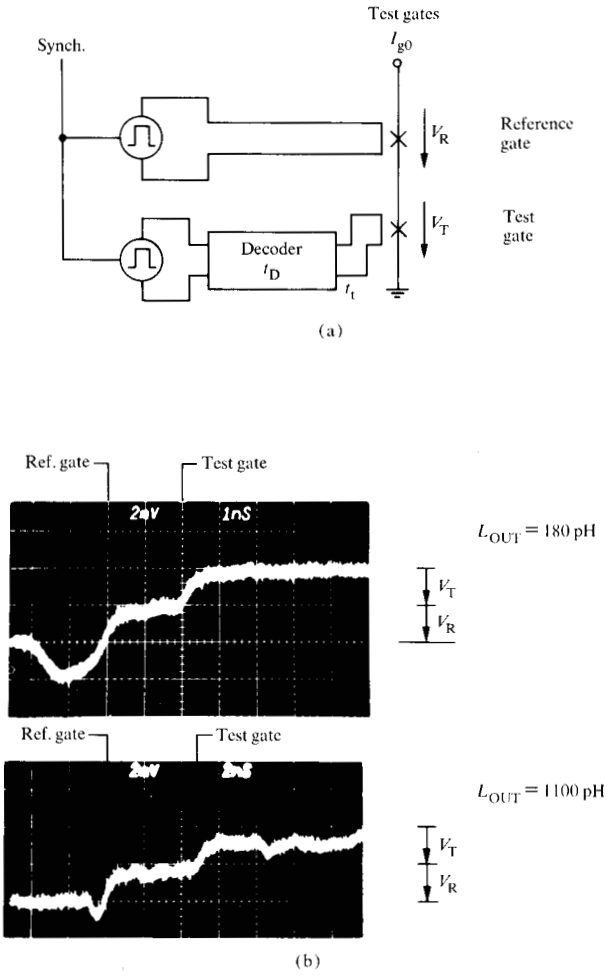


**Figure 15** Decoder delay measurements: (a) test arrangement to deduce the overall decoder delay; (b) measured overall delays for output loop inductances at 180 pH and 1100 pH.

The decoder internal delay was measured as illustrated in Fig. 15(a). Two synchronized pulse generators are used—one for setting the decoder and the other to switch a reference test gate. As already mentioned, the test gates are collected in pairs having one gate current supply. Therefore, the voltage across the series connected test junctions can be measured. The top oscillogram of Fig. 15(b) shows the switching voltages across the test gate pair located close to the decoder for the address bit combination Ā · B̄ · C̄. Owing to the internal decoder delay ($t_D$) and the delay in the decoder output loop ($t_{OUT}$), the test gate at the decoder output loop switches 2 ns after the reference gate. The delay measurement was repeated for an address bit combination having the output running over the drive gates ($L_{OUT}$ = 1.1 nH). In that case [bottom oscillogram of Fig. 15(b)], the overall delay is measured as $t_{tot} = t_D + t_{OUT} = 4.8$ ns. For equal threshold characteristics of the test junctions and equal dc biasing of the test circuits, an equivalent delay factor $t_{OUT'}$ for multiplying the output inductances can be deduced from the two measurements: $t_{OUT'} = (4.8 - 2.0)\ \text{ns}/(1100 - 180)\ \text{pH} = 3.0\ \text{ns/pH}$.

Using this equivalent delay figure for the output loops, one finds for the average internal decoder delay

$$t_D = \frac{(4.8 + 2)\ \text{ns} - 3.0(1100 + 180)\ \text{pH}}{2} = 1480\ \text{ps}.$$

The internal delay per stage, measured at ≈500 ps, is slightly larger than the value deduced from the decoder

simulations, ≈400 ps per stage. The difference may be explained by the somewhat larger operating currents and by the coupling losses of the control lines to the junction being larger than assumed in the simulations.

Finally, the decoder was tested at a high repetition rate. The memory model was designed to operate at a cycle time of ≈30 ns. This figure fixes the maximum required repetition rate for the decoder. Figure 16 shows successful decoder operation up to a repetition rate of 40 MHz, a value limited by our present testing facilities. The bottom oscillogram illustrates the switching voltage of ≈2 mV across the test junction. To test whether the output current was reset properly, the second decoder set pulse in the figure was omitted, yielding a zero at the output. As can also be seen in the figure, the leading and trailing edges of the test gate enable pulse generate a disturb signal in the test output. This disturb signal is not due to the chip circuitry but is caused by inductive crosstalk of the chip holder.

In summary, successful testing of the three-bit to eight-bit address decoders was performed. Maximum repetition rates of the decoders >40 MHz can be achieved. The measured internal decoder delay for the three-stage decoder is $t_D \approx 1.5$ ns. For the target repetition rate of 30 MHz, the calculated transient power dissipation is only ≈1.5 $\mu$W, due to the superconducting loop principle used for the logic circuits.

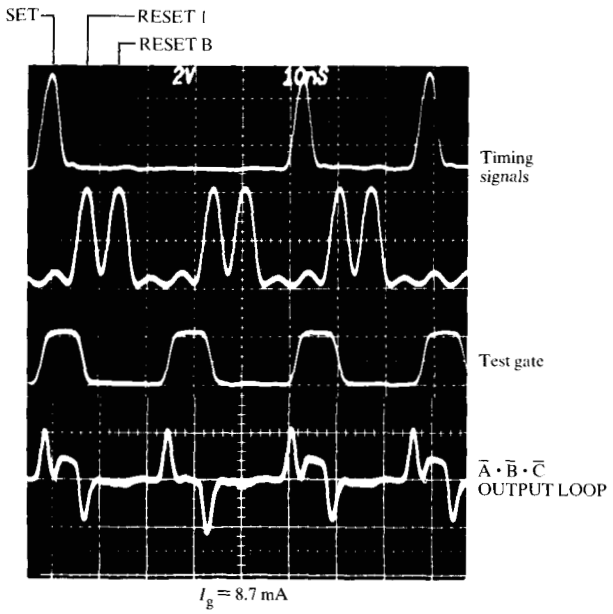


**Figure 16** Decoder operation at 40-MHz repetition rate. To test proper reset of the output loop, the second decoder set pulse in the figure was omitted.

## 5. Summary

This paper reviewed the circuit concepts for a main memory with Josephson junctions. A detailed description of the total memory and the experimental results are given elsewhere [2]. The results presented in this paper show that these concepts work as planned. Nearly final circuit blocks as required on a 16K-bit chip, like the *y* driver and the address decoders, have been built and have been shown to operate in quite good agreement with the design assumptions and simulation studies.

The SFQ cell used in the model with an area of ≈1500 $\mu m^2$ is large. However, one has to consider that only about one-third of the cell area is used for the interferometer, the remainder being used for wiring, especially because *x* and *d* lines are on the same metallization level. This necessitates a space-consuming underpass for crossing these lines. However, investigations have shown [17] that by introducing an additional metallization layer the underpass can be avoided, reducing cell area to values of 550 to 780 $\mu m^2$. With this cell area, a 16K-bit array would use about one-third of the total chip area. This, and the experimental results of the memory model, reveal that a 16K-bit chip is feasible having an access time of 15 ns and a cycle time of approximately 30 ns. The transient power consumption estimated for the chip at full speed is only about 40 $\mu$W.


## Acknowledgment

We are very grateful to U. Deutsch and W. Heuberger for the chip fabrication; to K. Daetwyler, H. Dietrich, T. Forster, M. Gasser, and L. Perriard for their technological contributions, and to O. Baechlin, W. Bucher, and H. P. Gschwind for carrying out the measurements. Without the excellent masks provided by the mask shop of IBM Burlington, VT, this work would not have been possible.


## References


1. W. Anacker, *IEEE Spectrum* **16,** 26 (1979).
2. R. F. Broom, P. Guéret, W. Kotyczka, Th. O. Mohr, A. Moser, A. Oosenbrug, and P. Wolf, *IEEE J. Solid-State Circuits* **SC-14,** 690 (1979).
3. R. F. Broom, R. Jaggi, Th. O. Mohr, and A. Oosenbrug, *IBM J. Res. Develop.* **24** (1980, this issue).
4. A. H. Silver and J. E. Zimmerman, *Phys. Rev.* **157,** 317 (1967).
5. E. O. Schulz-Dubois and P. Wolf, *Appl. Phys.* **16,** 317 (1978).
6. P. Guéret, *Appl. Phys. Lett.* **25,** 426 (1974).
7. P. Guéret, *IEEE Trans. Magnetics* **MAG-11,** 751 (1975).
8. H. H. Zappe, *Appl. Phys. Lett.* **25,** 424 (1974).
9. P. Guéret, Th. O. Mohr, and P. Wolf, *IEEE Trans. Magnetics* **MAG-13,** 52 (1977).

10. J. Matisoo, *Proc. IEEE* **55,** 172 (1967).
11. R. F. Broom and Th. O. Mohr, *J. Vac. Sci. Technol.* **15,** 1166 (1978).
12. R. F. Broom, W. Kotyczka, and A. Moser, *IBM J. Res. Develop.* **24** (1980, this issue).
13. A. Moser, *IEEE J. Solid-State Circuits* **SC-14,** 672 (1979).
14. P. Guéret, Th. O. Mohr, A. Moser, and P. Wolf, *Proceedings of ESSCIRC 1977*, Ulm, W. Germany, VDE Verlag, Berlin, 1977, p. 115.
15. *IBM Advanced Statistical Analysis Program*, IBM Publication No. SH20-1118, available through IBM branch offices.
16. H. H. Zappe, *J. Appl. Phys.* **44,** 1371 (1973).
17. P. Wolf, unpublished results.

*Received April 20, 1979; revised October 22, 1979*

*A. Moser and P. Wolf are located at the IBM Research Laboratory, 8803 Rüschlikon, Switzerland; P. Guéret is now with IBM Switzerland, Zurich.*