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Stability of Lateral pnp Transistors During Accelerated Aging

Lateral pnp devices stressed under accelerated temperature and voltage conditions show a degradation in the transistor breakdown voltage. These results and additional experiments that were conducted to better understand the mechanisms involved in the observed behavior are described. It was concluded that the degradation can be related to a negative surface charge in the base region of the transistor. This preliminary finding has design and process implications for potential improvement of bipolar device reliability in applications that call for high voltages and low epitaxial doping concentration.

Introduction

Lateral pnp structures are found to exhibit considerable degradation in the transistor breakdown voltage BV_{CEX} (Fig. 1), but not in the collector-base breakdown voltage BV_{CBO}, when stressed under accelerated temperature and voltage conditions. The effect of baking without bias on degraded devices was also explored. It was found that the degradation is relaxed by baking at 150°C. These results are indicative of a surface charge problem of particular concern for high voltage devices with low epitaxial (epi) doping concentrations.

A negative charge buildup in the base region of the pnp device would be consistent with the observed effects. Such a charge buildup could be caused by the stress alone or in combination with radiation effects due to the sputtering of quartz. Studies of FET structures have shown device instabilities related to the creation and charging of interface states [1, 2]. Positive oxide charge [3] and neutral electron trapping centers [4] are known to be produced by radiation. Other studies have shown that a high surface state density results from electron-beam irradiation [5].

Results of stress on two types of ring collector pnp structures, shown in Figs. 2(a) and (b), are reported here. In Fig. 2(a), the emitter contact metal is inside the emitter boundary, while in Fig. 2(b) it overlaps the base region. To observe the effects of quartz sputtering, additional measurements were made on bipolar processed MONOS capacitors and FET devices having the same dielectric composition, both with and without quartz.

Experiments

- *PNP stress*

Chips used for stress were designed with ten single-emitter lateral pnp transistors. The emitters of the pnps were connected to a common pad, while the collectors and bases were brought out to separate pads. Three wafer lots

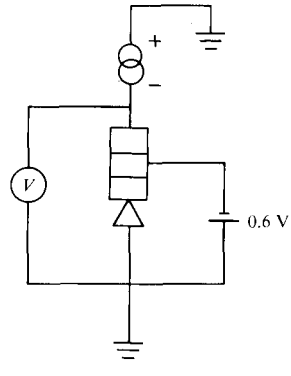

Figure 1 BV_{CEX} determination. V is measured.

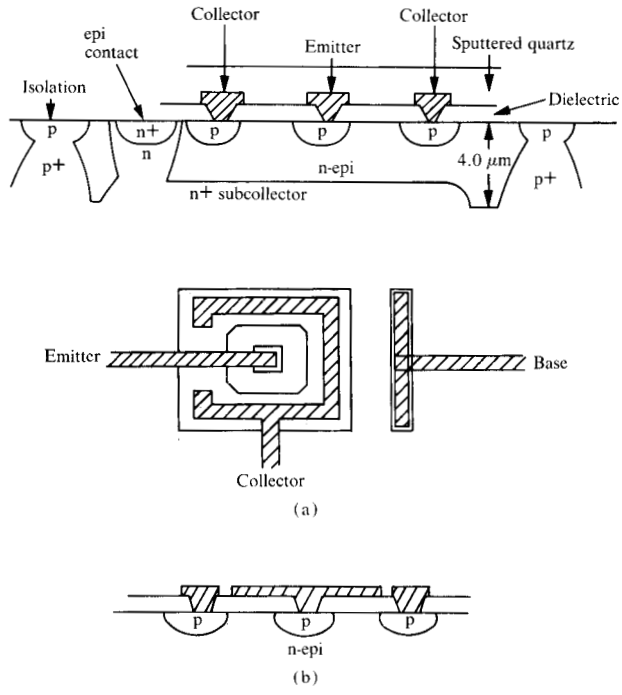

Figure 2 (a) Vertical and horizontal geometry of lateral pnp transistors. The dielectric consists of 400 nm pyrolytic oxide, 85 nm silicon nitride, and 250 nm thermal oxide. (b) Vertical geometry of overlapped emitter pnp.

with pnps of the type shown in Fig. 2(a) and one lot with pnps of the type shown in Fig. 2(b) were processed for the experiments. The chips were mounted on substrates and encapsulated into modules.

During stress, the collectors of the pnps were reverse biased to 8 V and 13.5 V with respect to the emitters. The p isolation was reverse biased to −11 V. The stress temperatures used in the experiments were 125°C, 150°C, and 165°C. The following parameters were measured automatically at ambient temperature:

BV_{CEX} at 50 μA, $V_{BE} = -0.6$ V,

BV_{CBO} at 50 μA,

BV_{CEO} at 50 μA,

I_E/I_B at $I_E = 500$ μA.

Readouts were taken periodically for a total duration of 700 hours of stress. The failure criterion was BV_{CEX} less than 8 V on any pnp on the module. This parameter BV_{CEX} was determined by forcing a constant current of 50 μA between collector and emitter and measuring the collector-to-emitter voltage (Fig. 1).

Measurements with and without quartz

CV measurements

A lot-to-lot variation in the amount of degradation observed on nonoverlapped emitter structures could not be traced to any differences in process history. In order to determine if time-zero differences in effective oxide charge could account for this variation, CV measurements were made on MONOS capacitors located at sites on the left and right sides of the experimental wafers. These wafers were removed from each of the lots after quartz deposition and were not stressed.

To determine the effects of quartz sputtering, additional CV measurements were made on wafers with and without quartz deposition. One lot of wafers was processed with epitaxial resistivity of 0.5 Ω-cm (Process I) and the other with 0.2 Ω-cm (Process II). The dielectric thickness used in Process I is shown in Fig. 2(a); thinner oxide was used in Process II. The quartz sputtering was identical in both processes.

The CV technique involves measuring the high frequency (1-MHz) capacitance with a slow sweep of voltage across the capacitor. The resulting CV plots provide quantitative information on flatband voltage and effective dielectric charge [6], and semi-quantitative information on surface states.

FET measurements

FET threshold voltage measurements were made on long channel FET structures, both with and without quartz deposition, to provide a check on the effects of the sputtering of quartz on small structures. Effective oxide charge density was calculated from the threshold voltage, equivalent oxide thickness, and effective doping concentration of the FET structures.

Results

PNP stress

PNP devices from the three lots of nonoverlapped emitter structures showed a similar degradation in BV_{CEX} and BV_{CEO}, although in varying degree. Figure 3 shows an example of data from lot A, which is typical of the degradation in a device which has not failed. The transistor breakdown voltage BV_{CEX} exhibits a marked decrease with time, while the junction breakdown voltage BV_{CBO} remains relatively stable. Typical behavior of pnp beta during stress is indicated by a plot of measured I_E/I_B, shown in Fig. 4. In general, lot A showed the least amount of degradation, while pnp devices from lot C degraded most severely and contributed most of the failures.

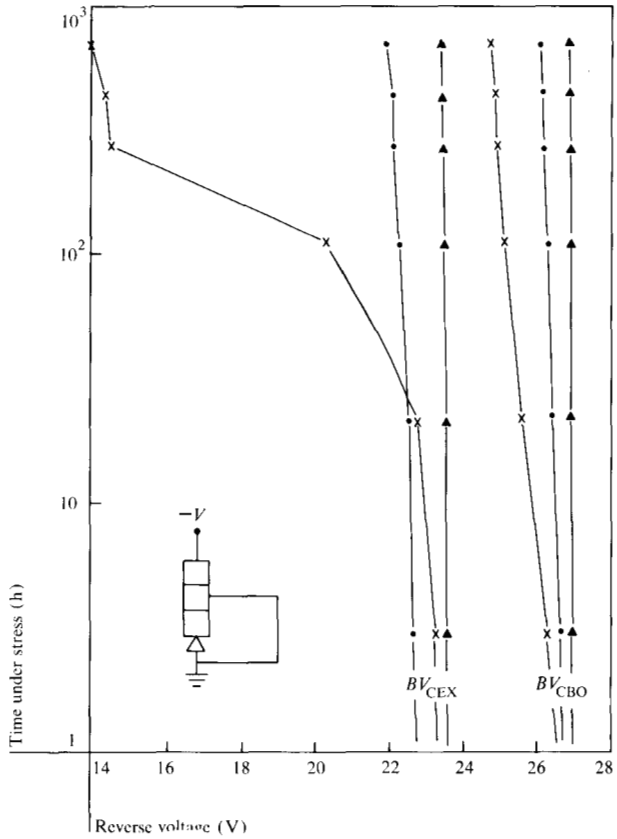

Figure 3 Lateral pnp degradation for lot A at 8-V stress: ▲, 125°C; •, 150°C; ×, 165°C. Circuit diagram shows stress condition.

Device failures under stress allow for the formulation of an empirical model for the degradation. Figure 5 shows a log normal plot [7] of the cumulative percentage of failures as a function of time under stress for lot C at the three stress temperatures. A temperature acceleration factor of the following form can be determined from this plot:

$$af = \exp\left[\frac{\Delta H}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right], \tag{1}$$

where ΔH = temperature activation energy in eV, and T_1 and T_2 are stress temperatures in Kelvin.

The slope σ of the lines is

$$\sigma = \ln\left(\frac{t_{50}}{t_{15.9}}\right), \tag{2}$$

where t_{50} = time to 50% failure, and $t_{15.9}$ = time to 15.9% failure.

The values for ΔH and σ obtained from this plot are

$$\Delta H = 1.6 \text{ eV and } \sigma = 1.1. \tag{3}$$

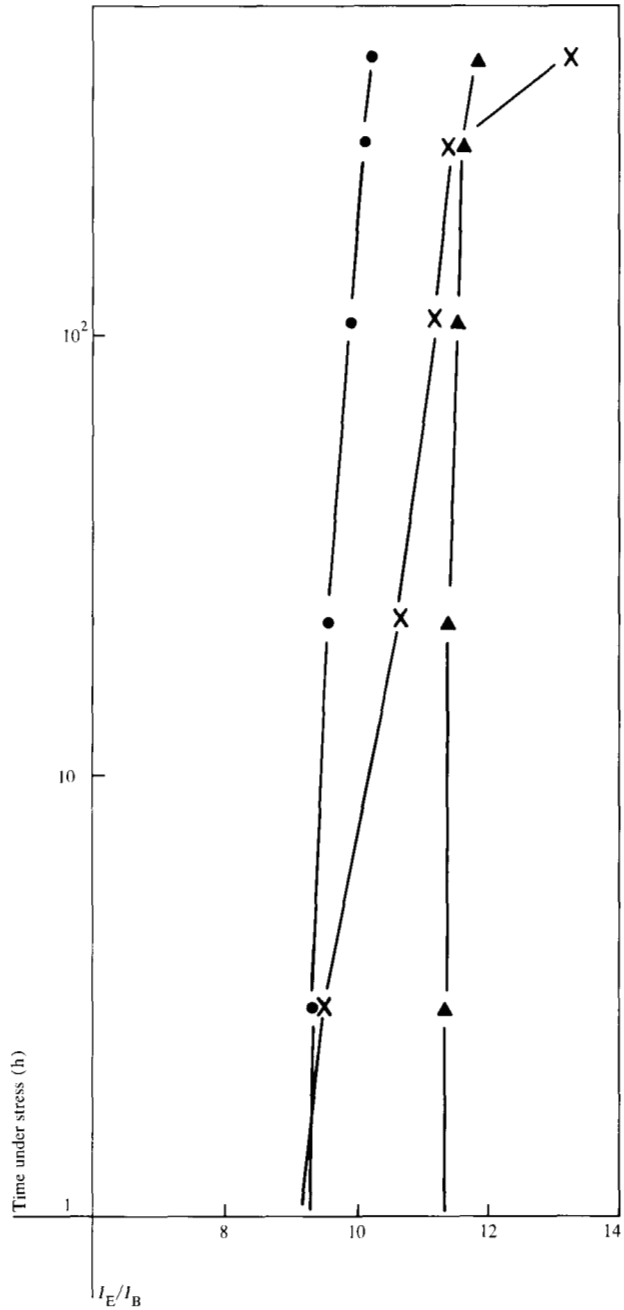

Figure 4 I_E/I_B at I_E = 500 μA for lot A at 8-V stress: ▲, 125°C; •, 150°C; ×, 165°C.

The effect of baking without bias on degraded devices gives further information for understanding the mechanism. A sample of modules from lot C, which degraded most severely, was used to repopulate the 8-V, 150°C stress cell for 371 hours and was subsequently baked at 200°C for 1/2 hour. It was found that the breakdown voltages and beta returned to their time-zero values after this bake. Repeated stressing and baking showed that the deg-

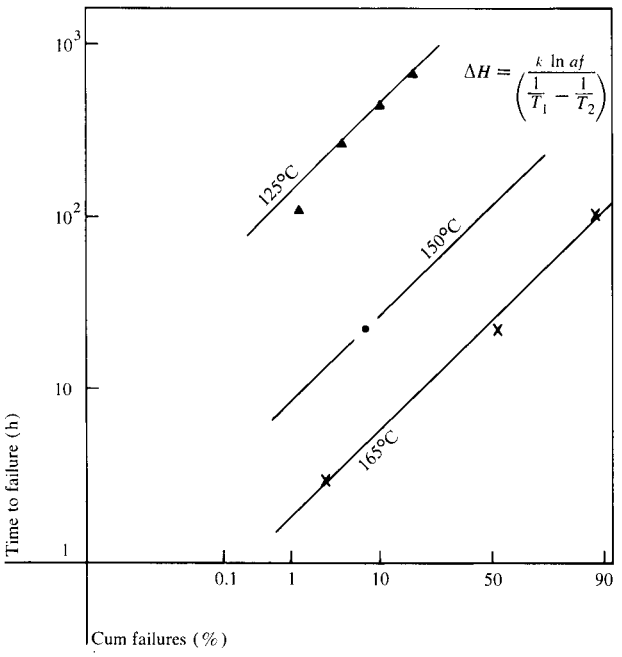

Figure 5 Log normal plot of pnp failures for lot C of 66 modules at each temperature at 8-V stress: ▲, 125°C; •, 150°C; ×, 165°C. ΔH equals 1.6 eV and σ equals 1.1.

Table 1 Effective oxide charge density—pnp test wafers (with quartz).

	A1	*A2*	*B1*	*B2*	*C1*	*C2*
N_{eff} (q/cm^2)	5×10^{11}	4×10^{11}	4×10^{11}	6×10^{11}	9×10^{11}	1×10^{12}

Table 2 Effective oxide charge.

	Process I	*Process II*
Without quartz	-8×10^{10} to $+5 \times 10^{10}$ q/cm^2	-2×10^{11} to $+2 \times 10^{11}$ q/cm^2
With quartz[a]	$+3 \times 10^{11}$ to $>1 \times 10^{12}$ q/cm^2	$+2 \times 10^{11}$ to $>1 \times 10^{12}$ q/cm^2

[a]Note that the upper limit for effective charge with quartz is greater than 1×10^{12} q/cm^2, since in some cases C_{min} had not yet been reached for large values of gate bias.

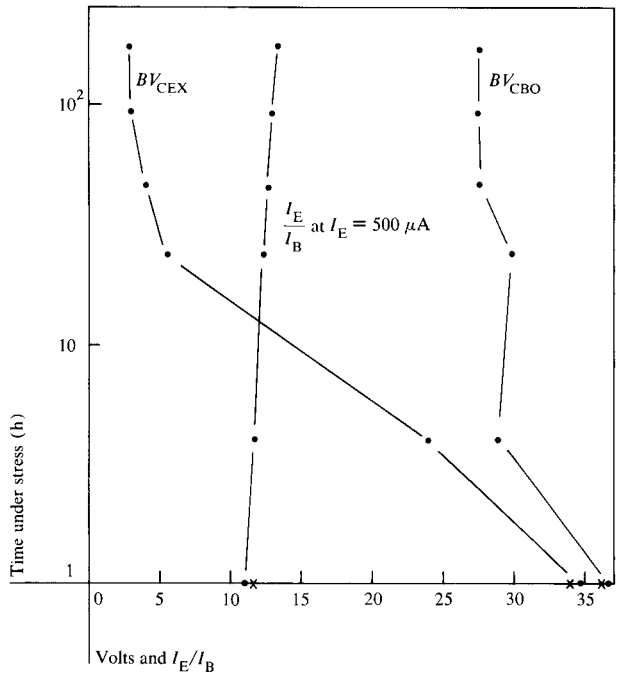

Figure 6 Degradation and recovery after baking. Key: •, stress data for lot C at 150°C and 8 V for 182 hours; ×, recovery after baking at 200°C for one-half hour.

radation mechanism was consistently reversible. Figure 6 shows an example of a module stressed for 182 hours, which degraded below the failure criterion of BV_{CEX} less than 8 V at 50 μA. After baking, the original value of BV_{CEX} = 35 V was restored.

Additional baking experiments were made at 150°C and the increased time necessary for curing was monitored. Figure 7 shows the amount of recovery for two pnp devices as a function of the baking time. In general, it was found that complete recovery can be achieved by baking at 150°C for four to six hours.

A sample from lot C, which had been restored after baking, was restressed at 13.5 V, 125°C in order to study the voltage sensitivity of the degradation. Figure 8 shows a comparison of the resulting failures with those from the original 8-V, 125°C stress cell. An estimate of the voltage acceleration factor at 125°C can be made from this plot:

$$af = e^{-\beta \Delta V} \quad \text{with } \beta = 0.6\ V^{-1}. \tag{4}$$

No degradation was observed during stress at 150°C, at either 8 V or 13.5 V, on structures with emitter metal overlap [Fig. 2(b)].

- *Measurements with and without quartz*

CV measurements

Figure 9 shows the results of CV measurements on MONOS capacitors at two sites on wafers from the three

Table 3 FET results.

		Process I	*Process II*
Without quartz	V_T	−13 V	−9 V to −10 V
	N_{eff}	9×10^{10} q/cm^2	2.3×10^{10} to 9.8×10^{10} q/cm^2
With quartz	V_T	−16 V to −17 V	−13 V to −14 V
	N_{eff}	2.0×10^{11} to 2.4×10^{11} q/cm^2	3.2×10^{11} to 4.0×10^{11} q/cm^2

experimental lots of nonoverlapped emitter structures. The CV data for lot C show a more negative flatband voltage than do those for the other two lots, indicating a larger positive effective dielectric charge. A variation in the slope of the curves between the maximum and minimum values of capacitance is observed as well. The capacitor at site C2 exhibits a severe flattening in the slope, such that C_{min} is not yet reached for a gate bias up to −60 V. This behavior is indicative of a high surface state density [1]. Table 1 shows the values for effective oxide charge density calculated from these curves.

Figure 10 shows an example of CV plots for one sample without quartz deposition and two samples with quartz deposition in Process I. Before quartz deposition, the flatband voltage is close to zero, since the workfunction difference is approximately zero. After quartz deposition, the flatband voltage is shifted in the negative direction, indicating an increase in positive effective charge in the dielectric. The flattening of the slope after quartz deposition shows increased surface state density. This behavior was observed in both processes studied. Table 2 shows the range of values calculated for effective oxide charge density in the two processes.

FET measurements

Typical values for threshold voltage at zero epi bias and effective oxide charge density calculated for each process are shown in Table 3. Values for equivalent oxide thickness and epi doping concentration used for these calculations were t_{eq} = 570 nm, $N_d = 1.5 \times 10^{16}$ cm^{-3} for Process I, and t_{eq} = 300 nm, $N_d = 3.5 \times 10^{16}$ cm^{-3} for Process II.

An increase in threshold voltage is observed on devices with quartz deposition, again indicating an increase in the effective positive charge in the oxide. The charge densities shown in Table 3 are not the same as those calculated from the MONOS data, probably due to the difference in geometry between the FET and MONOS structures.

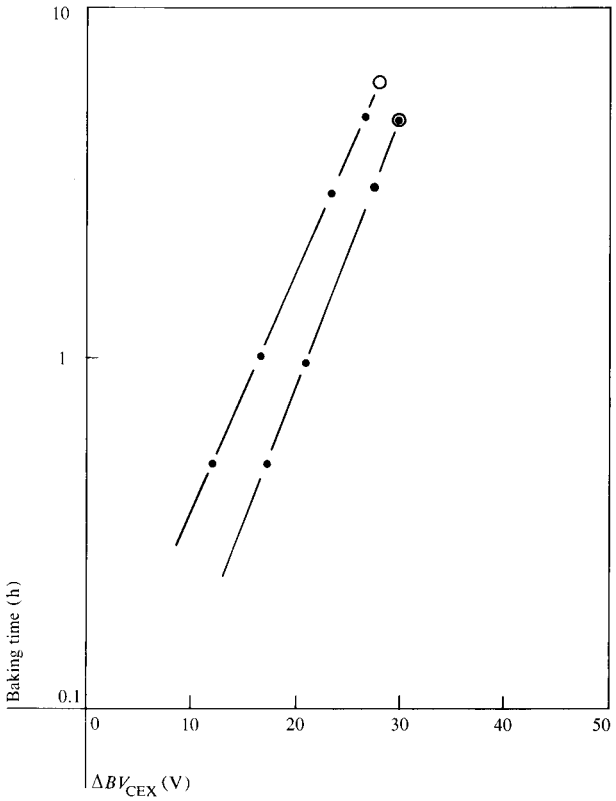

Figure 7 Recovery during baking at 150°C for two pnp samples. Stress condition for lot C was 150°C and 8 V for 812 hours. Key: •, delta in BV_{CEX} (V) recovered from degraded state; ○, amount of recovery necessary to return to initial state.

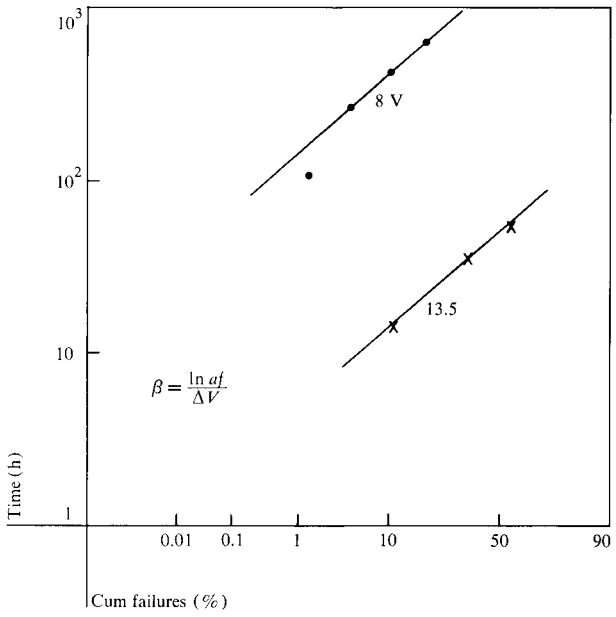

Figure 8 PNP device stress (voltage acceleration) for lot C at 125°C stress. β equals 0.6 V^{-1} and σ is approximately 1.0.

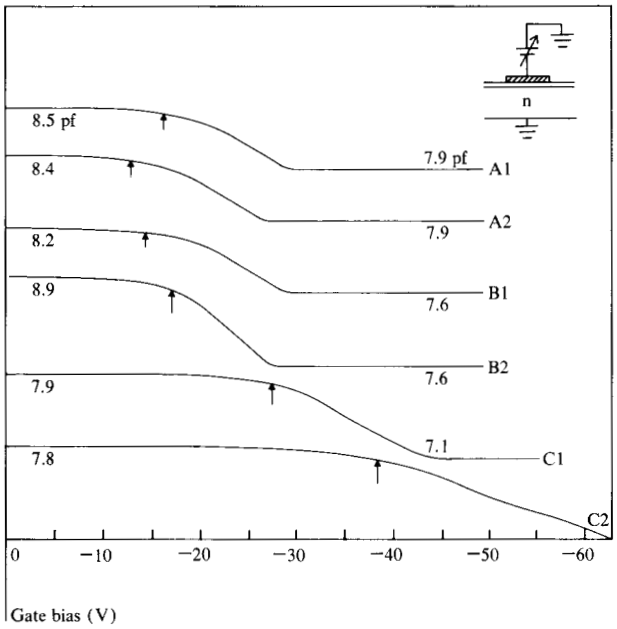

Figure 9 CV plots after quartz deposition for nominal gate area of (400 μm)^2. Note: arrow indicates position of flatband voltage V_{fb}. Curves are for lots A1 to C2 as shown.

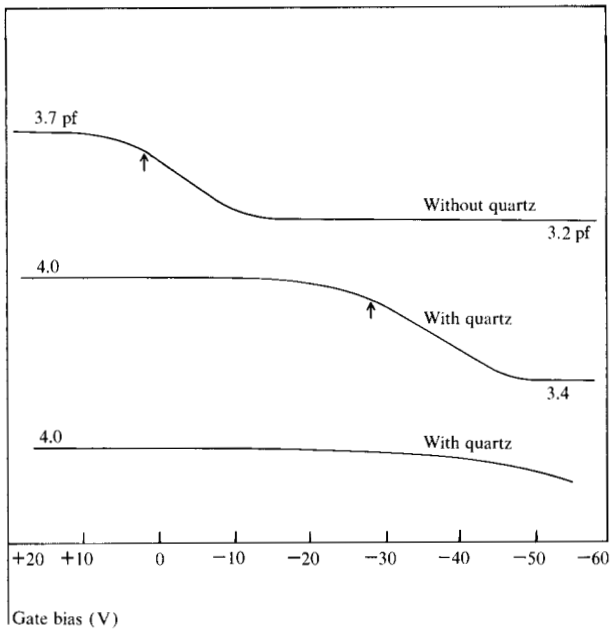

Figure 10 CV plots before and after quartz deposition for nominal gate area of (250 μm)^2.

Discussion

The results have demonstrated that pnp structures can degrade when subjected to stress. There is a decrease in BV_{CEX} (increased emitter-to-collector leakage), accompanied by an increase in beta. The degradation effects relax with baking at 150°C.

The decrease in BV_{CEX}, together with the increase in beta, is consistent with a narrowing of the effective base-width of the pnp device during stress. Figure 11 shows the suggested dynamics whereby negative charge builds up at the silicon-oxide interface, causing the collector depletion layer to spread through the base region. This will result in eventual punchthrough or inversion.

The reversibility of the degradation with baking at such a low temperature is evidence that we are dealing primarily with very shallow traps or surface states. Positive oxide charge could affect the degradation by accelerating electrons to the surface with enough energy to surmount the 3.2-eV barrier [8] at the silicon-oxide interface. However, electron trapping in the oxide would not be so readily annealable [4].

There seems to be a greater susceptibility to degradation in devices where there is an initial high positive oxide charge and surface state density. The CV measurements have shown that positive oxide charge and surface state density increase after the sputtering of quartz. The observed flattening of the CV curves has demonstrated the presence of donor type surface states which become positively charged during the measurement [1, 9]. It remains an open question whether neutral acceptor states are present as well after quartz deposition. It is these states which would become negatively charged during stress and thereby contribute to the degradation.

Further experiments are necessary in order to gain a fuller understanding of the degradation mechanism. Stress of pnp devices before quartz deposition would allow one to separate out the effects of quartz from the total degradation. Alternate techniques of measuring surface states, such as the quasi-static [10] or conductance [11] techniques, could be used to gain more quantitative information, if adapted to achieve the necessary sensitivity for measurement.

Solutions to the degradation problem have been suggested. Under the stress conditions in these experiments, no degradation was shown by pnp devices with emitter contact metal overlapping the base. The metal overlap therefore inhibits the degradation mechanism by acting as a field shield. Such a design could be used in applications involving high voltages, once the limits of its effectiveness were determined. Other design modifications such as an n+ guardring between base and isolation could be implemented where space allowed, in order to avoid a parasitic pnp effect. It has been shown that surface state

density can be reduced by annealing in pure hydrogen at 400°C [12]. If surface states due to the sputtering of quartz are indeed the main contributor to the degradation, such annealing after sputtering may be advantageous.

Summary

Results of experiments described in this paper show that lateral pnp transistors degrade under accelerated stress and therefore pose a reliability concern. A negative charge buildup in the base region of the transistor is consistent with the observed effects, which are reversible under low temperature baking. Device design modifications or process variations have been suggested as solutions to the degradation problem.

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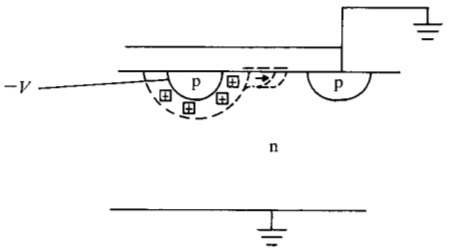

Figure 11 Proposed degradation mechanism.

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