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Transient Analysis of Uniform Resistive Transmission Lines in a Homogeneous Medium

Transient analysis of resistive transmission lines has always been difficult. The need for this type of analysis, however, did not become critical until high-density circuit packaging became commonplace. This paper discusses a method for the transient analysis of resistive lines. It does not require a large number of equivalent circuit elements, and yet it can be used to represent a resistive line to any desired accuracy.

Introduction

Signal interconnections between logic circuits in a high-speed, large-scale integrated (LSI) computer fall into two categories: on-chip and interchip communications. Generally, the on-chip connections are considered to be capacitive loads, since the transition time of the signal from one state to the other is usually greater than the delay of the signal propagation through the interconnecting network. For longer nets, resistance in series with the capacitance may be included. Since the propagation delays are short, the on-chip nets are not terminated and, with the present circuit technology, this delay represents only a small portion of the total delay. Therefore, an accurate prediction of the delay for these nets is not critical.

The second category consists of interchip communication nets, where the interconnection delays are long compared with the signal transition times. To minimize delay and the possibility of double switching, multiple reflections must be prevented. Therefore, the nets whose timing is critical must be terminated in an impedance close to or equal to the characteristic impedance of the transmission lines used for interconnection.

Since LSI chips require high-density packaging with a large number of input/output connections, the conductors used for the connections must be small, and they are placed close to one another. To reduce the coupled noise between adjacent lines, the reference plane is brought into close proximity to the signal lines, which lowers the characteristic impedance of these interconnections.

The current required to switch these low-impedance, terminated lines, together with the high resistance of the small conductors, produces severe loss and distortion of the signal. This distortion can have a very significant effect on the system performance and must be simulated accurately.

In 1967 F. H. Branin, Jr. [1] published a method for the simulation of ideal transmission lines. This method is known as the method of characteristics. Although we were not aware of Branin's work, the author and R. F. Sechler [2] implemented basically the same idea in a subroutine compatible with SCEPTRE [3]. The method of characteristics was later expanded to coupled lossless lines [4].

H. W. Dommel [5] has suggested that a resistive line can be represented by an ideal line with several resistors inserted along the way. He shows with his example that three resistors are sufficient. But this is true only if the transition time of the waveform of interest is long compared with the time separation between these resistors, when the resistance is sufficiently large to produce significant reflections. Thus for accurate representation it may become necessary to make the separation between these resistors less than one tenth of the fastest transition time of interest.

The separation between these resistors becomes very small when the interconnections of high-speed digital

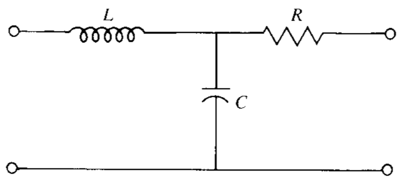

Figure 1 Basic *RLC* representation of a lossy line section.

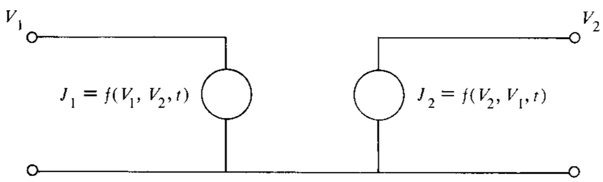

Figure 2 Equivalent circuit for a transmission line.

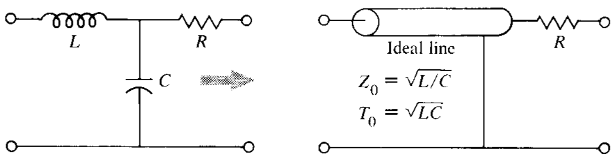

Figure 3 Modification of basic *RLC* circuit.

logic stages are simulated. This in turn forces the simulation program to deal with a large number of transmission lines and resistors. Furthermore, it becomes difficult, if not impractical, for the user to specify this network to the simulation program. The method described here is similar in nature to Dommel's suggestion in that, in effect, the resistive line is treated as a collection of ideal line segments separated by small resistors. However, the ideal line segments and the resistors do not exist in such a form as to be seen by the analysis program. Values of the incoming waveforms are stored at a constant time interval, and every stored point, in effect, becomes a segment of ideal line.

The method described here allows the time-domain simulation of single or coupled multiple resistive lines, in a homogeneous medium, to any desired accuracy. We assume that the resistance R, the capacitance C, and the inductance L for the lines being simulated are all independent of frequency and position along the line. Obviously, since all parameters are assumed to be constant, the application of a signal whose frequency spectrum extends up into the region where the transmission line exhibits skin effect would produce erroneous results. Therefore, this assumption places an upper limit on the frequency content of the drive signal.

Single resistive lines

The transient behavior of a resistive line with constant parameters (R, L, C) can be simulated by the repetitive use of circuit sections, as shown in Fig. 1.

To eliminate false ringing at the output, when the input is excited by a fast transition, the electrical length (delay) of each section has to be made small. Therefore, a long transmission line requires a large number of sections, which, in turn, forces the simulation program to solve a large number of differential equations at every pass.

The method described here is a combination of the method of characteristics for a lossless line and the distributed circuit shown in Fig. 1. When this method is used, the equivalent circuit becomes two voltage-dependent current sources (Fig. 2). With this representation, changes in length of the transmission line do not affect the network seen by the simulation program. (In ASTAP [6] implementation, this allows changes in length by means of the rerun control.)

To better illustrate this method, we start by modifying the circuit of Fig. 1 to look like that shown in Fig. 3.

The ideal line segment is used to replace the LC portion of the circuit. This step in itself will eliminate false ringing. Furthermore, if we use the method of characteristics to represent this ideal line segment, we reduce the overall problem to a resistive network, as shown in Fig. 4.

Rewriting Branin's [1] equations (9) and (10) to fit the nomenclature used here (see Fig. 4), we have

$$E_{2_n}(t) = (2V_n - E_{1_n})(t - T_0), \tag{1}$$

$$E_{1_n}(t) = (2V'_{n+1} - E_{2_n})(t - T_0), \tag{2}$$

where $(t - T_0)$ represents a time delay of T_0. Since (again referring to Fig. 4)

$$V_n = I_n Z_0 + E_{1_n}$$

and

$$I_n = \frac{E_{2_{n-1}} - E_{1_n}}{2Z_0 + R},$$

then

$$V_n = \frac{Z_0(E_{2_{n-1}} - E_{1_n})}{(2Z_0 + R)} + E_{1_n} = \frac{1}{2} A(E_{2_{n-1}} - E_{1_n}) + E_{1_n}, \tag{3}$$

where A is the attenuation coefficient/section

$$A = \frac{2Z_0}{(2Z_0 + R)}.$$

Substituting Eq. (3) into Eq. (1) gives

$$E_{2_n}(t) = [-A(E_{1_n} - E_{2_{n-1}}) + E_{1_n}](t - T_0)$$
$$= [AE_{2_{n-1}} + (1 - A)E_{1_n}](t - T_0). \quad (4)$$

In the same manner,

$$E_{1_n}(t) = [AE_{1_{n+1}} + (1 - A)E_{2_n}](t - T_0). \quad (5)$$

If the transmission line is broken up into N ideal line segments, interconnected with $N - 1$ resistors, N can be chosen so as to make the delay of each ideal line segment short in comparison with the fastest transition time of the signal propagated down the transmission line.

Since each ideal line segment requires two voltage sources for its representation (see Fig. 4), $2N$ storage locations are needed to completely represent the interior of the transmission line. In Fig. 5 these locations are designated as E_{11} through E_{1N} and E_{21} through E_{2N}.

With this arrangement the time delay for each ideal line segment and therefore the time separation between adjacent storage locations is

$$T_s = \frac{(\text{Total delay})}{N},$$

while the value of each of the resistors used for interconnection is

$$R = (R_{\text{total}})/(N - 1).$$

The ends of the transmission line require special attention and four more storage locations are used for this purpose. Storage locations E_{20} and E_{1N+1} in Fig. 5 contain the input values as generated by the simulation program during the previous time step. Locations E_{10} and E_{2N+1} store the output from the transmission line, and therefore contain values that existed in E_{11} and E_{2N} respectively; however, these values are delayed in time by T_S. Since E_{11} and E_{2N} represent the input values to the ideal line segments at the ends of the transmission line, T_S represents the propagation delay for these segments.

The total number of storage locations necessary to fully represent the waveforms on the transmission line is therefore $2(N + 2)$.

The use of these memory locations to simulate signal flow is as follows. DC conditions are solved, based on the total resistance and the voltage applied to the line. By using this information and the equivalent circuit of Fig. 4, all locations in memory are initialized. There are auxiliary storage locations to keep track of the last simulated time (T_{sim}) and the last time the storage was updated (T_{stor}).

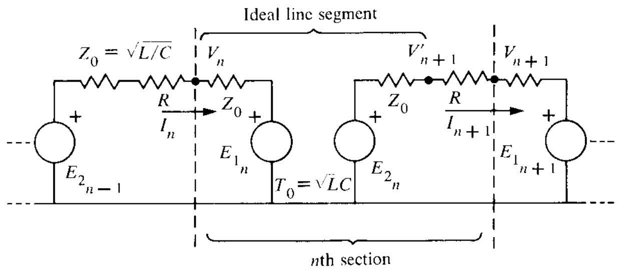

Figure 4 Resistive line representation using ideal line segments interconnected with resistors.

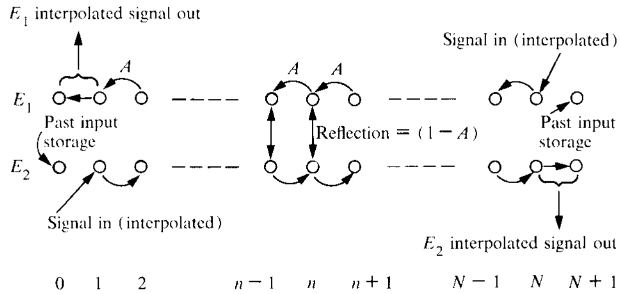

Figure 5 Illustration of signal flow through the storage array. Circles represent storage locations.

For dc conditions these times are equal to the simulation start time.

When transient simulation starts, and the simulation time takes the first step, a check is made as follows:

$$M = \frac{(T_{\text{sim}} - T_{\text{stor}})}{T_s} \quad \text{(truncated to an integer).}$$

If M is zero, the information in storage is not shifted. If M is greater than 1 or equal to 1, all the information is shifted M steps, in the manner of one step M times, and T_{stor} is updated to $T_{\text{stor}} + MT_s$. The distinction (M steps or one step M times) is important, since it guarantees that all reflections and attenuations are kept small and in proper phase. To accomplish this, the stored information is modified by Eqs. (4) and (5) and shifted to the adjacent locations. After all locations have been shifted, the process is repeated for a total of M times.

Shifting information from E_{11} to E_{10} and from E_{2N} to E_{2N+1} involves neither attenuation nor reflection. Since the actual simulation time in any program with variable step size doesn't necessarily change in increments corresponding to T_s, the output from the transmission lines has to be interpolated from the above four points. Similarly, as the waveforms are shifted down the line, positions E_{21} and E_{1N} have to be filled in. This is accomplished by interpolating between the present input values and the information stored in E_{20} and E_{1N+1} (past input values).

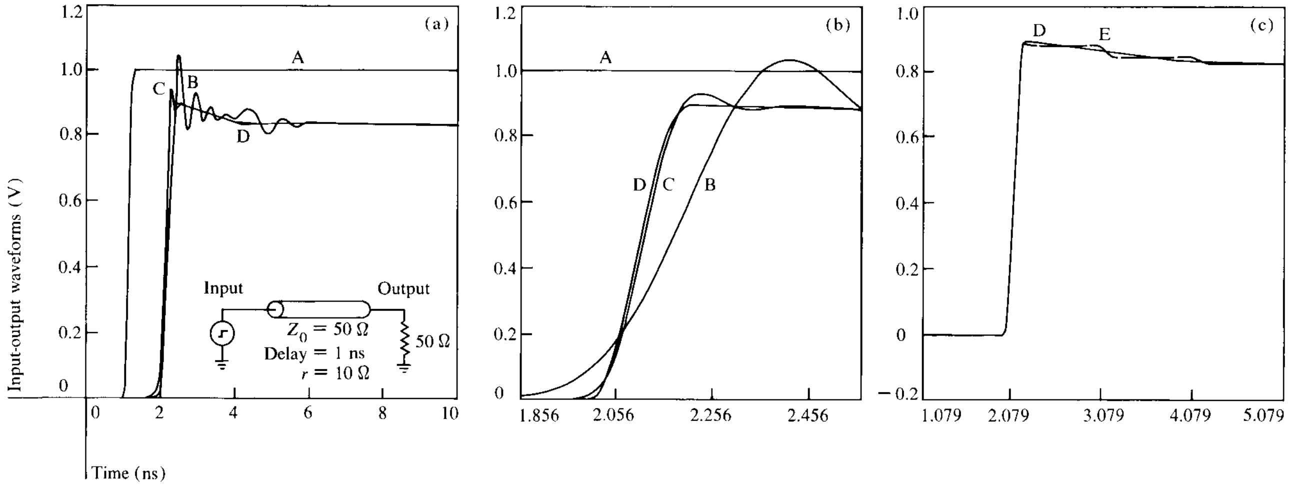

Figure 6 Input (A) and output waveforms for a transmission line simulated with: (B) 10 sections of *RLC*, (C) 100 sections of *RLC*, (D) method described here with N = 50, and (E) Dommel's method using three resistors. (a) Comparison of B, C, D; (b) Expanded view of the output waveform transition shown in (a); (c) Comparison of D and E.

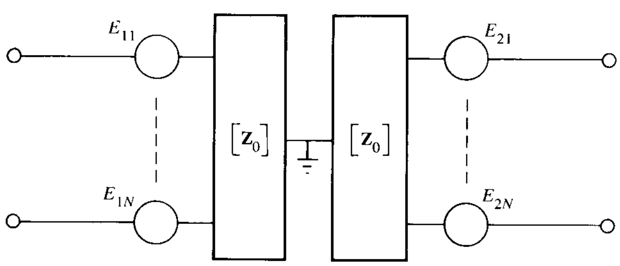

Figure 7 Method of characteristics representation of ideal coupled lines.

Table 1 Effect of simulation method for transmission lines on the simulation program (for circuit shown in Fig. 6).

	Simulation methods		
	Present method	*RLC*	
	(N = 50)	*10 sections*	*100 sections*
Number of			
E sources	1	1	1
J sources	2	0	0
Capacitors	0	10	100
Inductors	0	10	100
Resistors	1	11	101
Total elements	4	32	302
Number of simulation passes	113	169	261
Relative computer time			
Input phase	1	1.29	7.18
Execution phase	1	0.65	2.31
Total	1	0.87	4.0

To obtain the actual output from the subroutine, the information obtained by interpolation between E_{11} and E_{10} and between E_{2N} and E_{2N+1}, together with the input voltage applied to the line at the present time, is converted by means of Z_0 to a value of current for the sources shown in Fig. 2.

An experimental version of ASTAP has been modified to accept a simple description of resistive lines. In the execution phase the simulation is done according to the method described here. Figures 6(a) and (b) show the results of simulating a resistive line driven by an ideal source and terminated by a resistor whose value is equal to the square root of L divided by C, *i.e.*, the characteristic impedance of an equivalent ideal line.

In Fig. 6, even 100 sections of *RLC*, used to represent a 1-ns transmission line, produce ringing of significant magnitude when excited by an input whose transition time is 0.2 ns. To show the effect on the simulation program of the various approximations used in obtaining the waveforms shown in Fig. 6, we set up each method individually; the simulation statistics are listed in Table 1. In Table 1 the most significant factor is that accurate simulation by means of *RLC* sections requires a large investment of resources. Furthermore, the use of *RLC* sections forces the simulation program to use a greater number of passes than the present method, so that if the transmission line were simulated inside a large network, the increase in running time could be even more significant than it appears in Table 1.

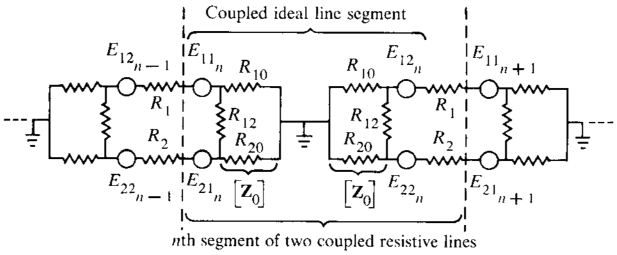

Figure 8 Coupled resistive line representation using ideal line segments interconnected with resistors.

Multiple coupled resistive lines

The method described above is easily expandable to transient analysis of coupled lines in a homogeneous medium. It is restricted to a homogeneous medium so that there is a one-to-one correspondence between the delay and the physical length of the line. This correspondence, in turn, produces a correspondence between the delay and the line resistances, so that the lines can be broken up into ideal line segments interconnected with pure resistances. In this manner, the waveforms can be properly attenuated, reflected, and coupled to adjacent lines.

Based on the method of characteristics, coupled lines can be represented as shown in Fig. 7. The characteristic impedance $\mathbf{Z}_0$ is a matrix as described by H. Amemiya [7] and K. D. Marx [8].

For simplicity in discussion let us consider two coupled resistive lines. According to the method described here, the equivalent circuit for these two lines would consist of four current sources. One current source is connected from each of the terminals to ground. The current in these current sources is a function of time and of all the four terminal voltages.

The equivalent circuit simulated by the subroutines is similar to that shown in Fig. 4. Now, however, besides attenuation and reflection, there is also some signal coupling among the various lines at every interconnection of the ideal line segments, as shown in Fig. 8.

The equations for the various voltage sources are equivalent to Eqs. (4) and (5), except that $\mathbf{Z}_0$ is now a symmetrical matrix, $\mathbf{R}$ is a diagonal matrix, and the $\mathbf{E}$ are vectors. Therefore, we can write

$$\begin{aligned}\mathbf{E}_{i2_n} &= 2\mathbf{Z}_0[2\mathbf{Z}_0 + \mathbf{R}]^{-1}\mathbf{E}_{i2_{n-1}} \\ &\quad + \mathbf{R}[2\mathbf{Z}_0 + \mathbf{R}]^{-1}\mathbf{E}_{i1_n}(t - T_0) \\ &= \mathbf{A}[\mathbf{E}_{i2_{n-1}} - \mathbf{E}_{i2_n}] + \mathbf{E}_{i1_n}(t - T_0), \qquad (6)\end{aligned}$$

and

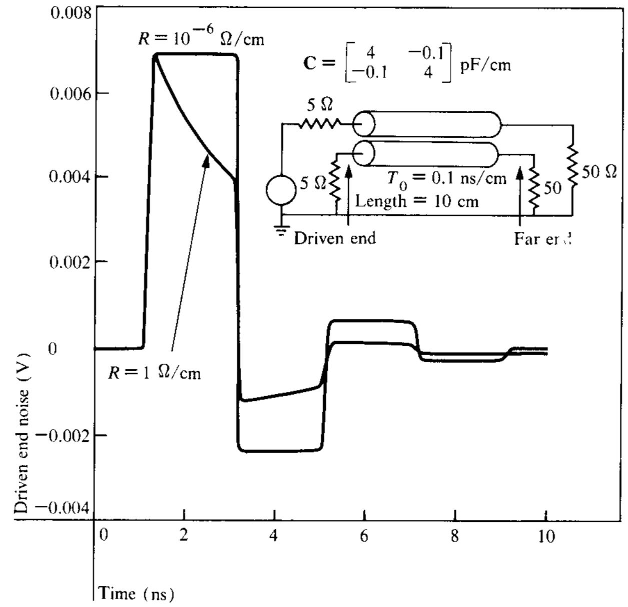

Figure 9 Driven end coupled noise for circuit as shown.

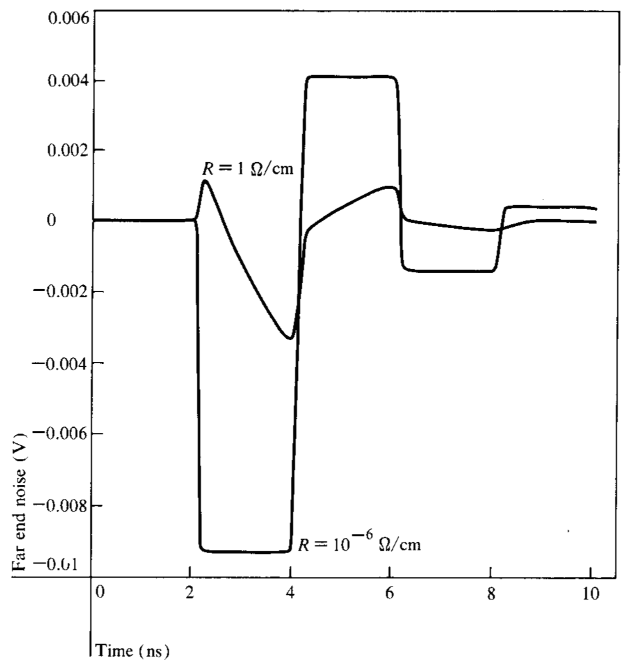

Figure 10 Far end coupled noise for circuit of Fig. 9.

$$\mathbf{E}_{i1_n} = \mathbf{A}[\mathbf{E}_{i1_{n+1}} - \mathbf{E}_{i2_n}] + \mathbf{E}_{i2_n}(t - T_0), \qquad (7)$$

where $\mathbf{A}$, now the attenuation and coupling matrix, is equal to

$2\mathbf{Z}_0[2\mathbf{Z}_0 + \mathbf{R}]^{-1}$.

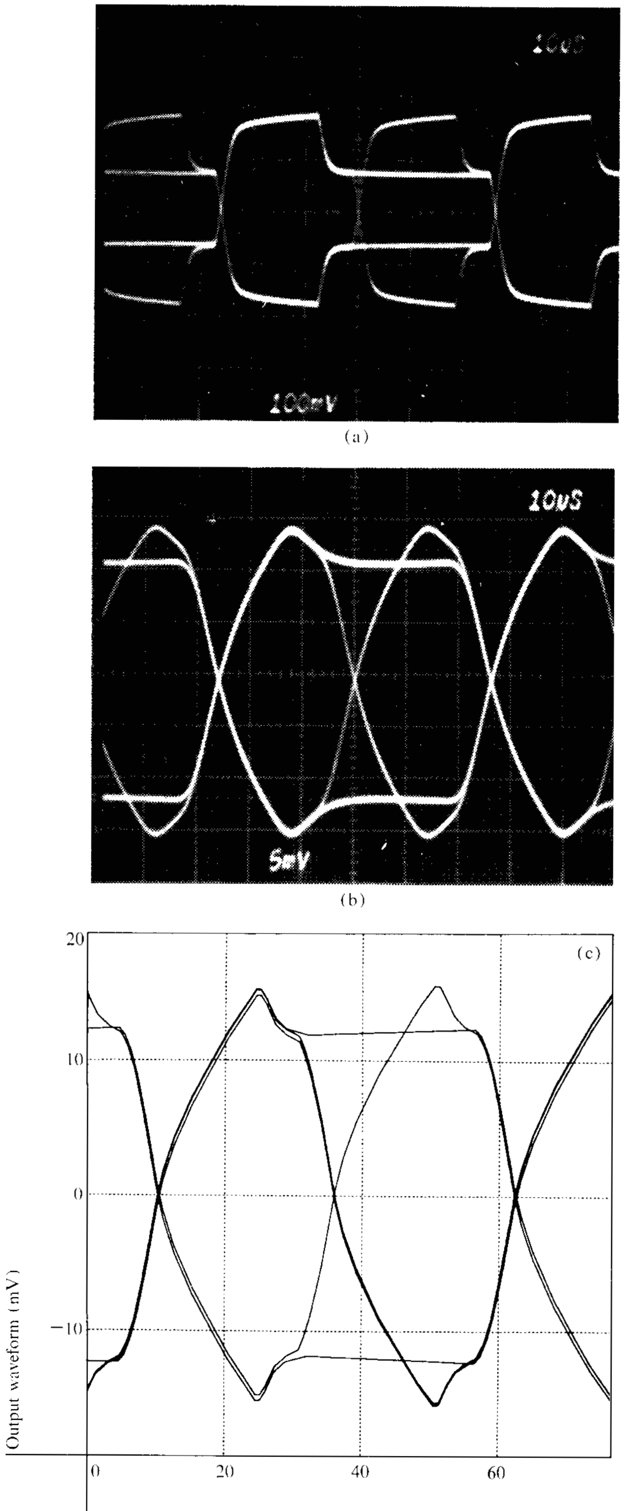

Figure 11 (a) Input waveform for a communications cable with the following characteristics: length = 6.45 km; resistance = 105 Ω/km; Z_0 = 110 Ω; T_0 = 5.3 μs/km, terminated with 155 Ω in parallel with 0.02 μF. (b) Measured output waveform—eye pattern. (c) Predicted output waveform—eye pattern, using method described here with a storage increment T_s = 0.25 μs.

To show the need for resistive line simulation in coupled noise analysis, we set up two coupled transmission lines in ASTAP with the resistive terminations close to $\mathbf{Z}_0$ (true $\mathbf{Z}_0$ termination would require three resistors). One line is switched with a low impedance source, while the other line is tied to ground with the same low impedance value. The input signal transition from zero to two volts is accomplished in 0.2 ns.

Two traces are shown in both Figs. 9 and 10. In both figures, trace A represents a series line resistance equal to 10^{-6} ohms per cm, whereas trace B represents one equal to 1 ohm per cm. Figure 9 represents the coupled noise at the driven end of the quiet line, whereas Fig. 10 represents coupled noise at the far end.

Accuracy of the proposed simulation method

Since this is an engineering solution to the problem of lossy lines, and no analytic solution is known to the author [9], the following comments can be made as to its accuracy:

a. The accuracy improves with decrease of the time interval between adjacent stored points (while computer time and required storage increase). Therefore one can determine the proper interval to use to obtain the desired accuracy "experimentally," by making several runs with different time intervals.

b. In general, for engineering analysis the recommended time interval is the smaller of the following:
   1. 0.1 times the fastest signal transition time applied to the line. (This is required to properly reproduce the signal since interpolation is required at the output.)
   2. A storage interval such that the series resistance per section is less than 0.01 times $\mathbf{Z}_0$ (to guarantee that the reflection coefficient per section is less than 0.5 percent).

Experimental verification

As discussed in the introduction, the method described here is intended for use in the analysis of interchip communication nets in a high-speed computer. However, these nets, although representing a relatively large delay when compared to a high-speed logic circuit, are physically quite short. It is therefore difficult (due to the contributions related to probe connections) to use these interconnections directly for accurate experimental verification of the program. It is, however, possible to minimize the probe effect by use of long transmission lines and lower frequencies.

Experimental results with negligible probe effects are shown in Fig. 11. These data represent waveforms associated with a 6.45-km communications net. The waveforms are shown plotted as eye patterns [10]. The input to this long transmission line is a 19.2-Kb/s bi-phase, predistorted signal whose peak-to-peak amplitude is 370 mV.

The measured output waveform shows an attenuation by a factor of 12.7, while the predicted waveform shows attenuation of 12.0. In comparing the measured waveforms with the predictions, note that the measured waveform has a much smoother appearance. The difference in the shape is attributed to skin effect attenuation, which becomes significant at the third harmonic.

Conclusions

Accurate simulation of resistive lines is necessary in fabricating high-density LSI packages; it is necessary not only for the proper prediction of the distorted incident pulse, but also for applications where coupled noise is a problem. Furthermore, the use of the method described here results in a more accurate prediction and/or more efficient use of computer resources than the *RLC* equivalent circuit representation.

This method, implemented in an experimental version of ASTAP and used extensively by circuit designers with satisfactory results, is becoming widely accepted because of increasing packaging densities, more complicated package structures, and the ever-increasing need to obtain the proper design the first time around. This method can be extended to include shunt conductance G by replacing the series resistance with an appropriate resistive network. In most cases this effect can be ignored and the packages analyzed by the author did not require this additional complication.

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References

1. F. H. Branin, Jr., "Transient Analysis of Lossless Transmission Lines," *Proc. IEEE* **55,** 2012 (1967).
2. R. F. Sechler and A. J. Gruodis, "Transmission Line Transient Analysis Techniques," unpublished result, IBM DSD East Fishkill laboratory, Hopewell Junction, NY.
3. J. C. Bowers and S. R. Sedore, *SCEPTRE, A Computer Program for Circuit and Systems Analysis*, Prentice-Hall, Inc., Englewood Cliffs, NJ, 1971.
4. C. W. Ho, "Theory and Computer-aided Analysis of Lossless Transmission Lines," *IBM J. Res. Develop.* **17,** 249 (1973).
5. H. W. Dommel, "Digital Computer Solution of Electromagnetic Transients in Single and Multiphase Networks," *IEEE Trans. Power App. Syst.* **PAS-88,** 388 (1969).
6. *Advanced Statistical Analysis Program (ASTAP), Program Reference Manual*, Pub. No. SH20-1118-0, IBM Corporation, Data Processing Division, White Plains, NY 10604.
7. H. Amemiya, "Time Domain Analysis of Multiple Parallel Transmission Lines," *RCA Rev.* **28,** 241 (1967).
8. K. D. Marx, "Propagation Modes, Equivalent Circuits, and Characteristic Terminations for Multiconductor Transmission Lines with Inhomogeneous Dielectrics," *IEEE Trans. Microwave Theory Tech.* **MTT-21,** 450 (1973).
9. G. R. Haack, "Comments on Transient Analysis of Lossy Transmission Lines," *Proc. IEEE* **59,** 1022 (1971).
10. R. W. Lucky, J. Salz, and E. J. Weldon, Jr., *Principles of Data Communication*, McGraw-Hill Book Co., Inc., New York, 1968, p. 61.

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