Pierce A. Brennan
Norman Raver
Albert E. Ruehli

Three-Dimensional Inductance Computations with Partial Element Equivalent Circuits

Inductance computations represent an important part in the design of hardware packages, especially for high performance computers. Partial element equivalent circuits (PEEC) [1] are used in this paper to investigate two problems, viz., the inductance of ground plane connections and the reduction in inductance due to eddy currents set up in perpendicular crossing wires. The results from the PEEC models are compared, for the first problem, to experimental hardware measurements and, in the second case, to simplified analytical solutions.

Introduction

Inductances represent an important electrical quantity in the design of hardware packages for high performance computers. The term "high performance" generally implies very fast switching times (a few nanoseconds or less) and large switching currents. Large unwanted inductive voltage drops may result because of the large, fast switching currents. The purpose of this paper is to present the concept of partial element equivalent circuits (PEEC [1]) and to illustrate its use by applying it to two geometries where inductance is the main electrical quantity of importance. The first geometry is shown in Fig. 1 where the self- and mutual inductances depend in large measure on the current distribution in the ground planes. This problem requires the PEEC concept to represent the ground plane. The second problem chosen is shown in Fig. 2. The problem is to find the reduction in inductance due to crossing wires. This requires PEEC treatment of the secondary line due to the eddy currents induced there.

Inductance problems have been considered previously by several authors [2-5], and most of the problems are from the microwave area [2-4] where the low frequency behavior is not of importance. This is in contrast to digital systems applications where the switching pulses, with fast rise times and long durations, cover a wide spectrum of frequencies.

The next section has an introduction to the PEEC solution method for inductances. The third section examines the plane connection problem, and in the last section the crossing wire eddy current problem is considered.

PEEC solution

This section presents the PEEC solution method as applied to packaging problems.The fundamental idea is to represent packaging geometries by electrical equivalent circuits whose combined elements can be analyzed by

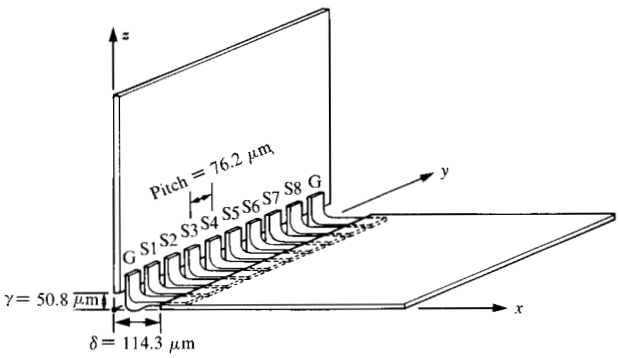

Figure 1 Geometry for two ground planes. Vertical plane = chip carrier; horizontal plane = foot.

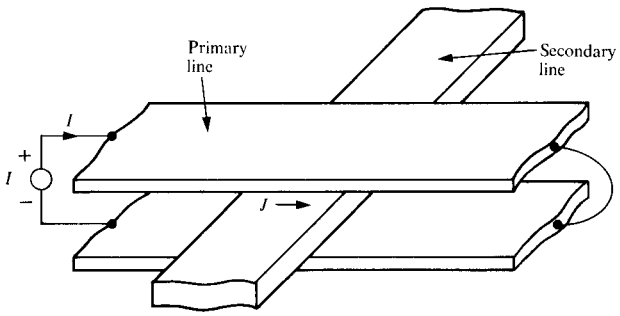

Figure 2 Crossing-line geometry. I = primary current; J = eddy current.

a general purpose network analysis program such as ASTAP [6, 7]. The currents and voltages of interest can then be obtained in the time or frequency domain in the usual manner.

It is assumed that the geometry consists of K conducting bodies each having a conductivity σ_k. Since the displacement current is assumed to be zero for inductance problems, there are two contributions to the electric field at a point $\bar{r}$ inside a conductor [1],

$$\bar{E}_0(\bar{r}, t) = \frac{\bar{J}(\bar{r}, t)}{\sigma} + \frac{\partial \bar{A}(\bar{r}, t)}{\partial t}, \tag{1}$$

where $\bar{J}$ is the current density. The vector potential, $\bar{A}$, for K conductors is

$$\bar{A}(\bar{r}, t) = \sum_{k=1}^{K} \frac{\mu}{4\pi} \int_{v_k} \frac{1}{|\bar{r} - \bar{r}'|} \bar{J}(\bar{r}', t) dv', \tag{2}$$

where v_k is the volume of conductor k, $\bar{E}_0$ is an external applied field, and retardation effects are neglected. As a result, Eqs. (1) and (2) yield

$$\bar{E}_0(\bar{r}) = \frac{\bar{J}(\bar{r}, t)}{\sigma} + \sum_{k=1}^{K} \frac{\partial}{\partial t} \left[\frac{\mu}{4\pi} \int_{v_k} \frac{1}{|\bar{r} - \bar{r}'|} \bar{J}(\bar{r}', t) dv' \right]. \tag{3}$$

For a thick conductor, the current density can be in an arbitrary direction at point $\bar{r}$ inside a conductor. This is represented in terms of orthogonal components as $\bar{J} = J_x\hat{x} + J_y\hat{y} + J_z\hat{z}$, and Eq. (3) can be rewritten as three integral equations, one for each of the orthogonal current densities $J_\gamma = J_x, J_y, J_z$.

All inductors in the geometry are carefully divided into cells and the surfaces laid out with nodes as illustrated in Fig. 3. Each cell is rectangular and current flow is uniform along one axis of the cell. Figure 3(a) shows the horizontal current flow cells and Fig. 3(b) shows the vertical current cells only. With this arrangement of cells the current density can be written as

$$J_\gamma^k = \sum_{n=1}^{N_{\gamma_k}} B_n^k J_{\gamma_n}^k, \tag{4}$$

where $B_n^k = 1$ for the nth cell of conductor k and is zero elsewhere and $J_{\gamma_n}^k$ is the uniform current density in conductor k on the cell n in the $\gamma = x, y, z$ direction. Conductor k is divided into N_{γ_k} cells in the γ direction. With Eq. (4), Eq. (3) is rewritten as a system of equations

$$E_{0_\gamma}(\bar{r}) = \frac{J_\gamma(\bar{r}, t)}{\sigma} + \sum_{k=1}^{K} \sum_{n=1}^{N_{\gamma_k}} \frac{\mu}{4\pi} \int_{v_{n_k}} \frac{1}{|\bar{r} - \bar{r}'|} \frac{\partial J_{\gamma_n}}{\partial t} dv', \tag{5}$$

for $\gamma = x, y, z$.

Up to this point it has been assumed that $\bar{r}$ is inside any one of the K conductors. Now we specifically assign $\bar{r}$ to be inside a cell m in conductor i and Eq. (5) is integrated over the volume of cell m:

$$\int_{v_{m_i}} E_{0_\gamma} dv = \frac{1}{\sigma} \int_{v_{m_i}} J_\gamma(\bar{r}, t) dv + \sum_{k=1}^{K} \sum_{n=1}^{N_{\gamma_k}} \frac{\mu}{4\pi} \left[\int_{v_{m_i}} \int_{v_{n_k}} \frac{1}{|\bar{r} - \bar{r}'|} dv' dv \right] \frac{\partial J_{\gamma_n}}{\partial t} \tag{6}$$

It is now possible to rewrite the current density in Eq. (6) in terms of the total cell current $I_\gamma = J_\gamma a_\gamma$. Further, we divide by the cross-sectional area a_{m_i} and we obtain an equation for each direction γ of the form

$$\int_{l_{m_i}} E_0 dl = \frac{l_{m_i}}{\sigma a_{m_i}} I_{m_i} + \sum_{k=1}^{K} \sum_{n=1}^{N_{\gamma_k}} \left[\frac{\mu}{4\pi} \frac{1}{a_{m_i} a_{n_k}} \int_{v_{m_i}} \int_{v_{n_k}} \frac{dv' dv}{|\bar{r} - \bar{r}'|} \right] \frac{\partial I_n}{\partial t}. \tag{7}$$

Equation (7) is interpreted as

$$V_{m_i} = R_{m_i} I_{m_i} + \sum_{k=1}^{K} \sum_{n=1}^{N_{\gamma_k}} L_{p_{m_i,n_k}} \frac{dI_n}{dt}, \tag{8}$$

where the left-hand side is the voltage between the nodes at the ends of the cell i in conductor m and the first term is the resistance of this cell. The summation term represents the coupling inductances over all cells in the same direction. Note that the cells involved in the integration act as conductors and the inductances among these so-called "partial" conductors or elements are called partial inductances [8]. The equivalent circuit which evolves from this technique is shown in Fig. 4 for the example of Fig. 3. All the nonperpendicular partial inductances are coupled.

Ground plane problem

Figure 1 illustrates the structure of a circuit board assembly which is used in the Josephson junction computer package [9]. This assembly consists of two pieces joined

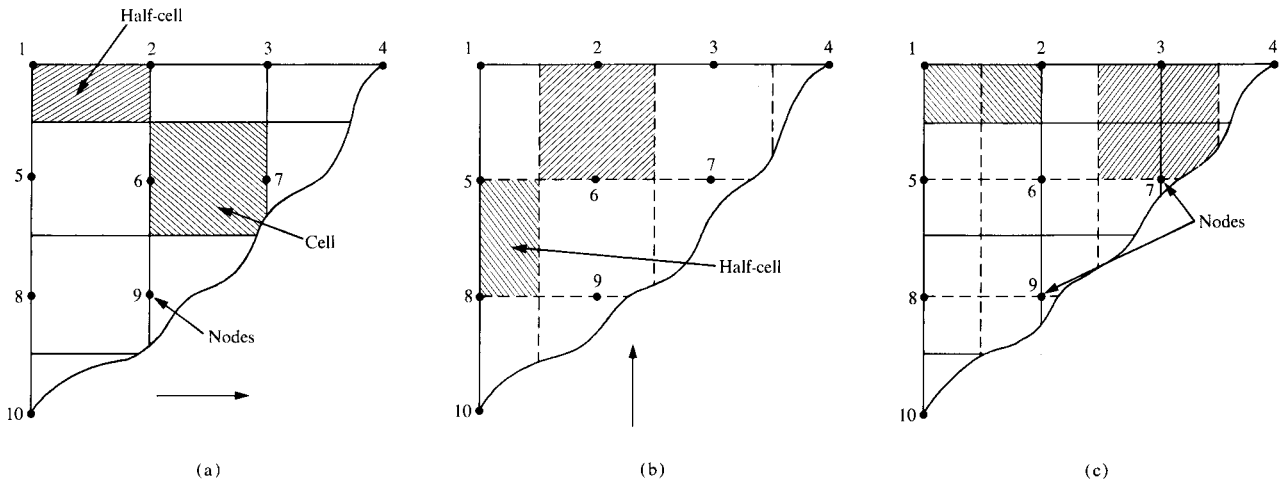

Figure 3 Cells for a corner geometry. (a) Horizontal current flow cells. (b) Vertical current flow cells. (c) Combined cells. Arrows indicate direction of current flow.

at right angles. The vertical piece has the chips mounted on it (chip carrier) while the horizontal piece (called the foot) is used to connect signals to the remainder of the package. The horizontal foot has a ground plane and superconducting signal transmission lines on its bottom surface, while the vertical piece has a ground plane and superconducting signal transmission lines on the inside surface. Connections between the lines and planes are made with solder connectors which fall into two categories. Two of the connectors, called G, link both ground planes together, while the remaining solder connections carry signals (S1 through S8 in the example of Fig. 1). Thus, a signal propagating from the horizontal to the vertical piece encounters discontinuities in both the signal and ground because of the solder connectors.

The problem is to compute the inductance resulting from the signal path discontinuities, including the mutual inductive coupling between the signal paths. These inductances determine the magnitude of the cross-talk among signal paths and also the rise time of a signal. Fabrication limits the smallest gap between the planes given by the parameters δ and γ indicated in Fig. 1. One way to limit the inductances is by the number of ground connectors between signal connections. In the example shown in Fig. 1, eight signal connections are placed between the two ground connections. We call this the signal to ground pin ratio.

Using the technique of the second section, the ground planes and solder connections are divided into PEEC to evaluate their contribution to the inductance. The vertical and horizontal ground planes are very thin and superconducting so that the cells have zero resistance. The inductive interaction is restricted to the y-direction since the planes are perpendicular to each other. These factors permit both ground planes to be represented by a single layer of overlapping cells.

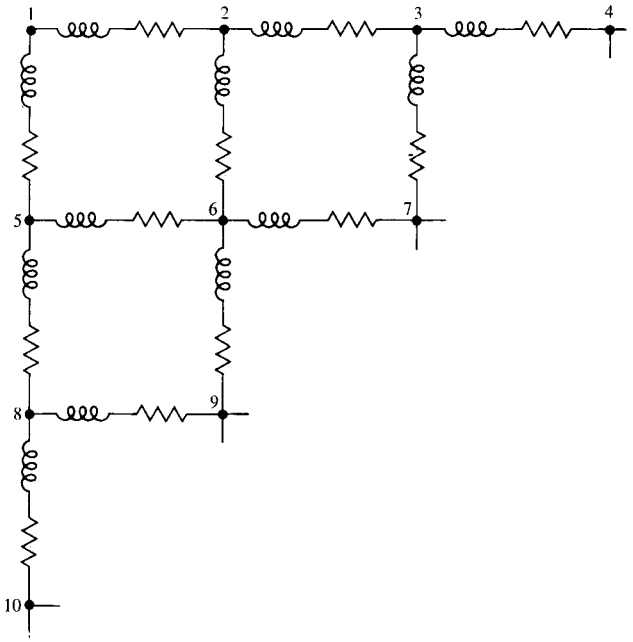

Figure 4 PEEC for corner geometry of Fig. 3.

Each plane allows a two-dimensional current flow along the length and width of the planes similar to the situation shown in Fig. 3. Thus, each of the two planes is replaced with a PEEC as shown in Fig. 4, where all cells

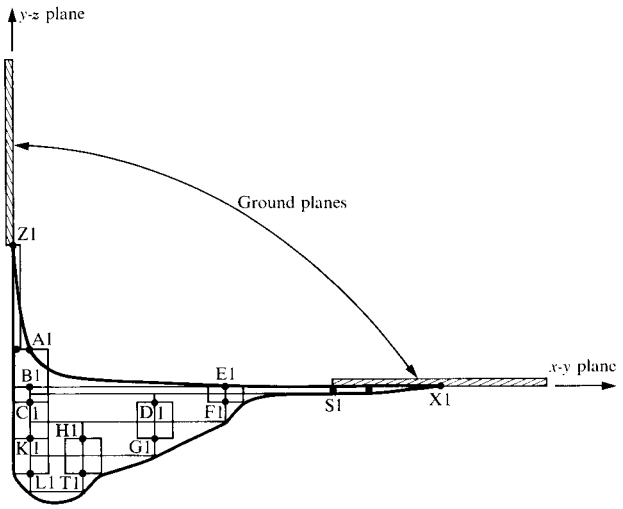

Figure 5 Inductance model for solder fillet.

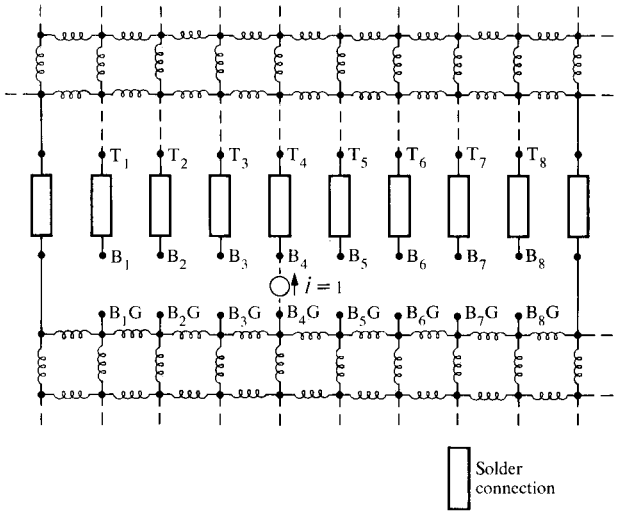

Figure 6 PEEC model for connection region.

in the same direction are coupled while the orthogonal cells lead to zero mutual inductance. For superconducting planes we must add to the partial inductance an additional inductance term, which is the kinetic inductance [10] due to the kinetic energy of the super-electrons. However, for the geometries considered here this term is negligible [11].

So far we have considered models only for the planes. For a complete PEEC model we also require inductance models for the solder connections. A typical connection is illustrated in bold outline in Fig. 5 with the approximate cell divisions also shown. The PEEC model is self-evident from this. The width of the solder connection is divided into a single cell only. In the subsequent models the solder connections are represented by a rectangular box for simplicity. Specifically, Fig. 6 shows the PEEC for the solder connections and the planar model for the nearby region.

To obtain the effective discontinuity inductance caused by the ground plane gap we short the top node of the solder connections to the ground plane as shown in Fig. 6 by the dashed line. A current source, also shown by dashed lines, with a unit slope $\dot{I} = 1$ is introduced between ground and the solder connection B_iG to B_i where $i = 1, 2, \cdots, 8$ and the discontinuity voltages $V_i = V_{B_i} - V_{B_iG}$ are measured. The vector of voltages $\mathbf{V}$ and currents $\dot{\mathbf{I}}$ leads to the inductance matrix of interest. From an analytical point of view the terminal voltages of interest are obtained with a matrix reduction step which corresponds to the usual admittance matrix computation [12] or

$$\mathbf{V} = (\mathbf{A}\mathbf{L}_p^{-1}\mathbf{A}^T)^{-1}\dot{\mathbf{I}}, \tag{9}$$

where $\mathbf{V}$ is the vector of terminal voltages and the $\dot{\mathbf{I}}$ are given above. Thus, the inductances of interest are

$$L_{ij} = \frac{(V_{B_i} - V_{B_iG})}{\dot{\mathbf{I}}_{B_j}}, \tag{10}$$

where $i, j = 1, 2, \cdots, 8$.

In our problem, the $\mathbf{L}_p$ matrix in Eq. (9) for the 434 cells used is a 434 × 434 matrix. Each plane is represented by 142 cells while each solder connection involves 15 cells. The final symmetric 8 × 8 matrix corresponding to Eq. (10) is given by

$$\mathbf{L} = \begin{bmatrix} 119.2 & 76.4 & 62.7 & 52.53 & 43.48 & 34.8 & 25.93 & 16.08 \\ & 161.5 & 108.7 & 88.02 & 71.78 & 56.92 & 42.15 & 25.99 \\ & & 184.6 & 125.4 & 99.16 & 77.53 & 56.91 & 34.86 \\ & & & 195.2 & 130.7 & 99.15 & 71.76 & 43.54 \\ & & & & 195.2 & 125.4 & 88.0 & 52.6 \\ & & & & & 184.6 & 108.7 & 62.78 \\ & & & & & & 161.5 & 76.5 \\ & & & & & & & 119.3 \end{bmatrix} \tag{11}$$

where the values are in picohenries (pH).

A copper model scaled to 1000 times the actual model was fabricated to verify these results experimentally. Each plane in the model for Fig. 1 is 81.3 cm long, 45.7 cm wide, and 1.59 mm thick. The plane spacings are $\delta = 114.3$ μm and $\gamma = 50.8$ μm. The ground connections form electrical contacts while the signal connections are insulated. The measurements were made with a Hewlett-Packard 4815 vector impedance meter. A frequency range of 2 MHz to 15 MHz was covered to ensure the accuracy of the measurement and the absence of resonances. In addition, the measured data were corrected for possible resonances. The copper planes and the actual package boards are thin compared to the other spatial dimensions.

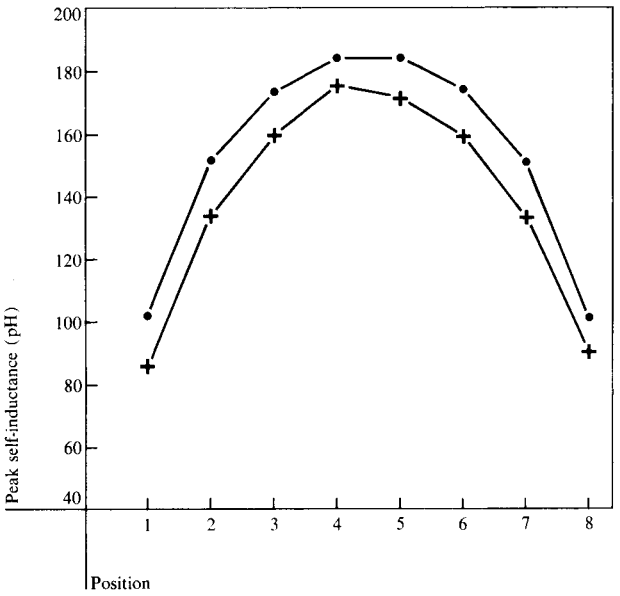

Figure 7 Measurements *vs.* PEEC model for self-inductances for geometry of Fig. 1. Comparison geometry: +, measured; •, calculated.

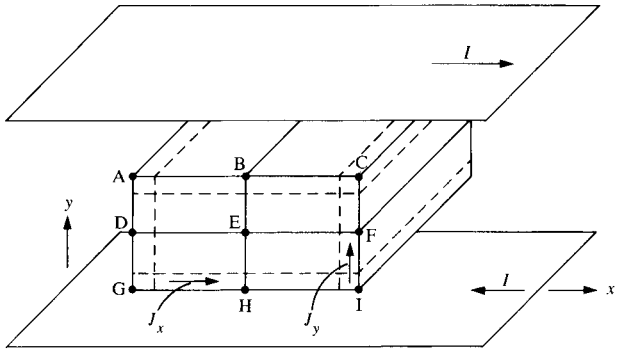

Figure 8 Cell divisions for secondary line.

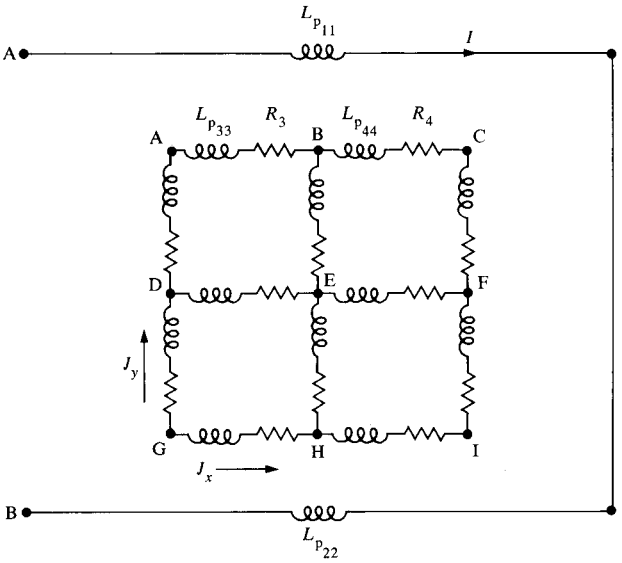

Figure 9 PEEC model. All inductances in parallel are coupled.

It was observed that skin effect along the model plane thickness was small and that there was a linear dependency of inductance with frequency. Figure 7 shows the agreement between the PEEC model and the measurements for the self-inductances.

Inductance of crossing lines

In this section we consider the reduction in inductance of a stripline shown in Fig. 2 due to the crossing secondary line. This represents a small but important part of a realistic geometry for high performance integrated circuits. Eddy currents are set up in the secondary line which are in the same direction as the primary line current and this leads to coupling between the primary and secondary line. These induced currents cause a reduction in the primary line inductance.

In Fig. 8, the direction of current flow for both the primary and the secondary lines is indicated. Note that only the parts of the secondary line that are important for the eddy current flow are shown. The currents in the secondary line are confined to the x-y plane since the currents in the z direction are small, especially for closely spaced planes where the impact of the crossing lines is the largest. Figure 9 shows the equivalent circuit for the model of Fig. 8 where the center conductor is partitioned into three divisions or cells in each direction with half-cells always placed at each edge. We are interested in the impedance between the terminals A and B, which is given as a function of frequency, f, as

$$Z(f) = R(f) + j\omega L(f) = V(f)/I(f). \quad (12)$$

Since we want to isolate the reduction in $L(f)$ due to the eddy currents in the crossing line, the top and bottom conductors are assumed to be of zero thickness, which eliminates their frequency dependence.

To establish the number of cells required to obtain an accurate equivalent circuit representation for the center conductor, an analytical solution was derived with the assumption that fringing is ignorable. This analytical solution for the inductance is obtained by solving the boundary value problem for the geometry depicted in Fig. 10, or

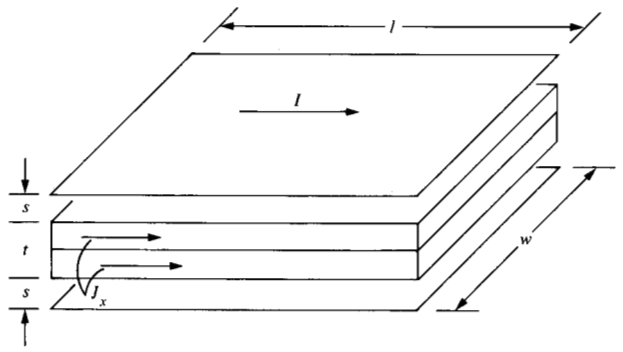

Figure 10 Test model for analytical evaluation.

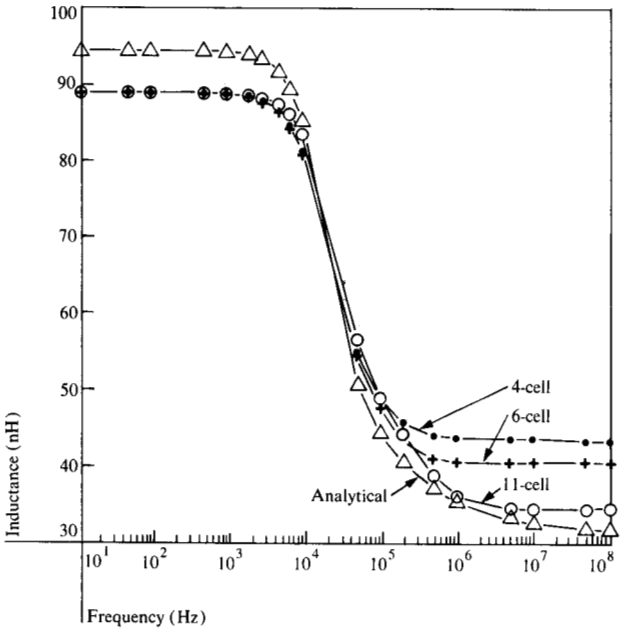

Figure 11 Frequency *vs.* inductance. Compares analytical with PEEC solution.

$$L(f) = \frac{\mu l}{w}\left[2s + t\,\frac{\sinh\left(\frac{t}{\delta}\right) + \sin\left(\frac{t}{\delta}\right)}{\cosh\left(\frac{t}{\delta}\right) + \cos\left(\frac{t}{\delta}\right)}\right], \tag{13}$$

where $\delta = (\pi f \mu \sigma)^{-1/2}$ is the skin depth.

It is observed from Figs. 11 and 12 and Eq. (13) that there are two limiting values for the inductance, the low frequency and high frequency limits. The low frequency limit is

$$L_0 = \frac{\mu l}{w}(2s + t), \tag{14}$$

which is the inductance without the presence of the center conductor. The low frequency inductance for the equivalent circuit of Fig. 9 is simply

$$L_0 = L_{p_{11}} + L_{p_{22}} - 2L_{p_{12}}, \tag{15}$$

where the $L_{p_{ii}}$, $i - 1, \cdots, n$, are the partial self-inductances and the $L_{p_{ij}}$, $i = 1, \cdots, n, j = 1, \cdots, n, i \neq j$, are the partial mutual inductances of the conductors. The high frequency inductance for the theoretical solution completely excludes fields from the center conductor so that

$$L_\infty = \frac{\mu l}{w}\,2s. \tag{16}$$

The equivalent circuit of Fig. 9 was modified to have current in the direction of the horizontal cells only, corresponding to the test model. To keep the fringing fields small, the dimensions chosen (see Fig. 10) were $l = 2$ m, $w = 4$ cm, $t = 1$ mm and $s = 0.25$ mm. The conductors were copper with $\sigma = 5.8 \times 10^7$ mhos/m, while μ is the permeability of air $= 1.257 \times 10^{-6}$ H/m. It can be seen from Fig. 11 that the solution of Eq. (15) (where fringing is included) is about five percent lower than the theoretical (no fringing) solution of Eq. (14) for low frequencies. At high frequencies $L_\infty = 31.42$ nH. From the curves it is clear that an accurate prediction of the high frequency inductor by the PEEC method depends on the number of cells into which the center conductor is partitioned. Increasing the number of cells provides a better representation of the current distribution in the conductor so that the skin effect is properly depicted, particularly at high frequencies where it is fully developed. The prediction for the change in inductance as a function of frequency is seen to be quite accurate over the full range for eleven cells per side.

One of the results that can be obtained from Eqs. (14) and (16) is that the normalized change of inductance between the low and high frequency limits is approximated by

$$\frac{\Delta L}{L} = k\,\frac{A_C}{A_T} \times 100, \tag{17}$$

where A_C is the cross-sectional area of the center conductor while A_T is the total area enclosed by the primary line and k is a constant determined by the shape of the center conductor. For the analytical model $k = 1$, since the length of the center conductor is the same as the primary line. Figure 13 shows three limiting cases for the center conductor in which the total area is kept constant. The dimensions of the primary line are the same as before except the length (l) has been shortened to 4 cm with a

spacing s = 1.1 cm. The three cases for the center conductor have t = 0.1 cm and w = 1 cm; t = 1 cm and w = 0.1 cm; $t = w$ = 0.333 cm, respectively. As can be seen from Fig. 12, the reduction in inductance is a function of the center conductor shape being greater for the horizontal and square cases. One of the reasons for this is that the coupling between the primary and center conductors is accomplished only through the horizontal segments. Thus, greater width causes increased coupling which results in lowered primary line inductance. The absolute value of the reduction in inductance depends on the geometry at hand. The geometrical dimensions are chosen to accommodate the different positions of the center conductor in Fig. 13. It was also observed that, for the case where t = 0.1 cm, varying the location of the center conductor caused no change in inductance from the value obtained when the conductor was centered with respect to the primary line. Finally, the value for k in Eq. (17) was empirically found to be 0.5 for these three cases.

The complex micromodel representing the crossing-line geometry can be simplified to a network of the type shown in Fig. 14. This is accomplished by synthesizing the frequency response of the impedance in Eq. (12). The simplified model in Fig. 14 is then used to analyze complex geometries.

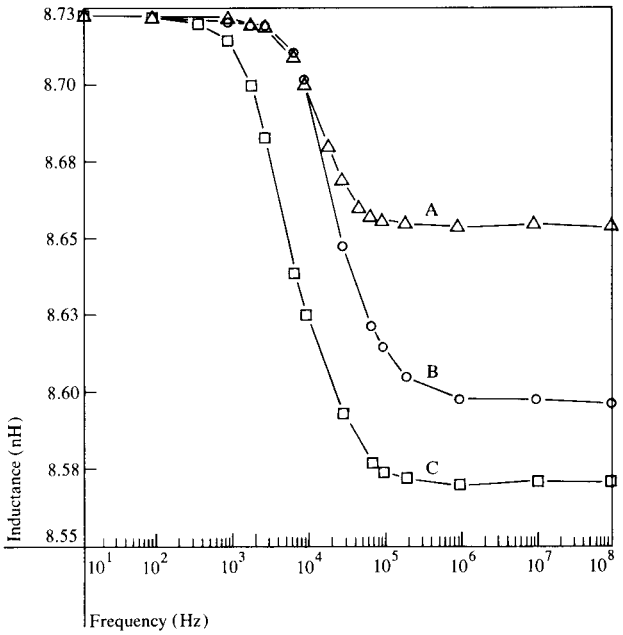

Figure 12 Frequency *vs.* inductance for vertical, horizontal, and square areas. All curves are for six cells per side: A, vertical shape; B, horizontal shape; C, square shape.

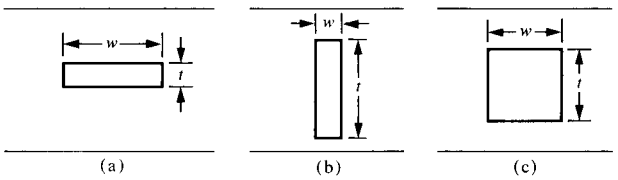

Figure 13 Cross-sectional shapes for secondary line. (a) Horizontal shape with w = 1.0 cm and t = 0.1 cm. (b) Vertical shape with w = 0.1 cm and t = 1.0 cm. (c) Square shape with w = 0.333 cm and t = 0.333 cm.

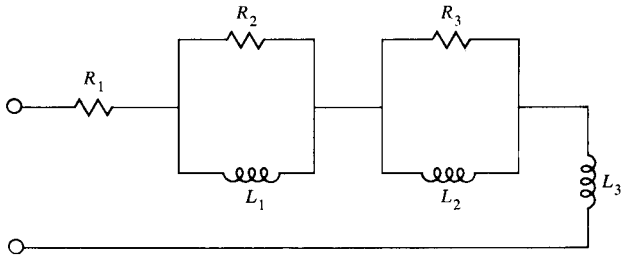

Figure 14 Simplified circuit model.

Summary

The use of partial element equivalent circuits, in conjunction with a circuit analysis program such as ASTAP, is a powerful method for solving three-dimensional inductance problems for high performance machines. It can be applied to both large scale and micromodel geometries with equally good results.

Acknowledgment

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The authors are located at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598.