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Survey of Computer-Aided Electrical Analysis of Integrated Circuit Interconnections

In the last decade an important shift has taken place in the design of hardware with the advent of smaller and denser integrated circuits and packages. Analysis techniques are required to ensure the proper electrical functioning of this hardware. In this paper we give a coherent survey of the modeling and computer-aided design techniques applicable to solving these problems. Methods are considered for the computation of resistances, capacitances, and inductances. Also, an extensive list of references is given.

1. Introduction

In the last decade an important shift has taken place in the design of hardware with the advent of smaller and denser integrated circuits and packages. Previously, the hardware components consisted of both physically and electrically large discrete components. Stray elements and coupling among the components were small in most cases and the interconnections between the components were electrically insignificant. The corresponding electrical network models were highly decoupled and the network analysis matrices sparse. This led to relatively simple analysis models and techniques for the electrical performance of these systems.

In contrast, today's high level of integration can lead to very large and complex systems with extremely small physical dimensions. An electrical analysis which excludes coupling among the closely spaced components is invalid. Further, the interconnections which once led to insignificant stray elements are now the main elements in the equivalent circuits. Thus, the circuit models for integrated circuit systems are extremely complex, with highly coupled components. An electrical analysis of these models without computer-aided design (CAD) techniques is not possible, especially for high performance systems.

The type of hardware designs which lend themselves to miniaturization are microwave, digital- and analog-type systems [1-4]. Usually, the overall dimensions of the relevant parts of a subsystem for which a signal or coupling analysis is of interest are small, less than a few centimeters. Often, the highest frequency component contained in the signals which are propagating in the system corresponds to a wavelength which exceeds the physical dimensions of the subsystem. These small physical and electrical dimensions in many cases make an analysis with lumped circuit models valid.

The type of analysis required for a particular system depends on its performance and purpose. The electrical analysis may become a very simple one for low speed or low frequency circuits since the reactance of the capacitances is high and the inductances are almost short circuits. Then a simple analysis may suffice which involves a few key capacitances, resistances, or inductances. In contrast, complex models are required to represent high speed or high performance systems. The signal transitions in very low speed digital systems may be in the micro- or even millisecond range. At the other end of the spectrum, we may be concerned with the analysis of a Josephson [5] or MESFET [6] technology where the signal transitions are in the picosecond range.

A fundamental quantity which characterizes a particular interconnection technology is what we call the *general impedance level*. It is simply the lossless characteristic

impedance of the "average" connection in the system,

$$Z_G = \left(\frac{L}{C}\right)^{1/2}.$$

Typical values of Z_G range from 5 to 200 ohms. In lower-performance FET logic hardware the devices are typically of a higher impedance than Z_G, and thus the capacitance C is the dominant circuit element. Bipolar transistor logic hardware may exhibit impedances on the order of Z_G, so that both C and the inductance L are important. Josephson junctions exhibit a very low internal impedance and the inductance L becomes a dominant stray element.

The computer-aided electrical analysis approach proposed here is based on electromagnetic field theory and circuit theory. The unknowns are expressed in terms of voltages and currents and this allows the use of well-known circuit theory concepts and models. The interconnection analysis of a system consists of several steps. First, the appropriate models of the circuit elements must be determined and the capacitances, inductances, and resistances must be computed. Then an analysis is performed to obtain the signals of interest, namely the voltages and currents, from which we evaluate the electrical operation of the hardware being modeled.

An illustration is given in Fig. 1 which includes all elements of high performance integrated circuit hardware. The integrated circuit chips are placed on a chip carrier which is sometimes called a space transformer, since it transforms the closely spaced integrated circuit chip connections to larger connection points. In the example shown, the connections among the chip carriers are established in the multi-plane board. A logic signal may start with an LSI circuit located on one chip in Fig. 1 and may be received by a circuit located in the other chip. Thus, the signal may be delayed by both the integrated circuits and the package. The major contribution to the average delay is due to the circuits for lower-performance systems, while the package delay dominates for the average delay for high performance hardware. Typical electrical design criteria which must be met by a hardware design can be summarized as follows for the example of a digital system:

a. All signals in the system must meet the timing requirements.
b. The signal wave shapes must be within given tolerances since, for example, a negative transition in a positive signal may lead to additional switching delay.
c. Unwanted signal coupling between wires must be less than an upper bound so that the coupled signals do not cause improper switching of the logic circuits.

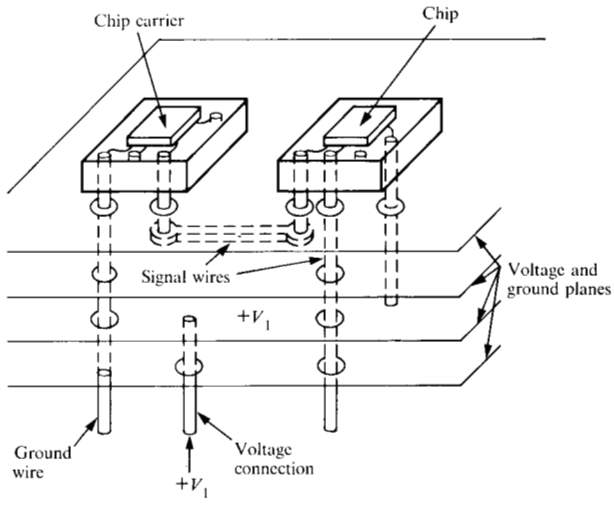

Figure 1 Example hardware.

d. Voltage transients on voltage distribution wires (and ground) induced by switching circuits must be limited to small fractions of the supply dc voltages.
e. External electromagnetic disturbances should not cause false switching of the digital circuits.

Thus, the purpose of computer-aided electrical analysis is to ensure that the hardware at hand meets these electrical design criteria.

The analysis of digital system interconnections encompasses a wide spectrum of frequencies. This is quite in contrast to microwave systems, which usually operate at a few discrete frequencies. As a consequence of this, a mixture of static, quasi-static and dynamic models is employed. Quasi-static models such as lumped equivalent circuits play an important role in the representation of the complex physical geometries. Further, an analysis with an incomplete model may lead to valuable information without solving the complete dynamic problem. An example of this is the analysis of a low impedance voltage supply system with an inductance-resistance model as is discussed in Section 4. In contrast to this, a complex capacitance-resistance model may suffice to represent most parts of a low current, high impedance FET package.

In this paper we discuss different aspects of the electrical analysis. In Section 2, resistance models and analysis techniques are discussed, while Section 3 is devoted to capacitance analysis. Inductance is considered in Section 4, while electrical models and analysis methods are given in Section 5.

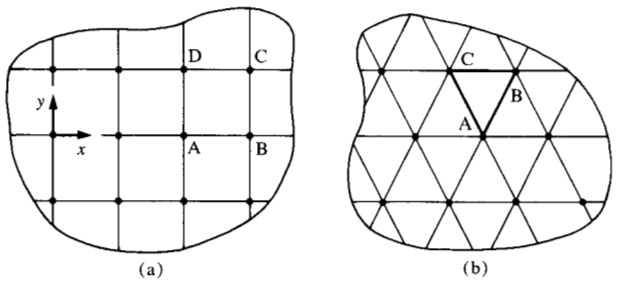

Figure 2 Nodal grids: (a) rectangular, (b) triangular.

2. Resistance computations

The purpose of the resistance computation for the interconnections and the ground and voltage supply planes is to determine whether the dc voltage drops along the conductors are within tolerable limits. In an LSI system, the dc supply current paths may require series resistances in the milliohm range for the voltage drops to be tolerably small. Especially as the spatial dimensions are further reduced for VLSI, an increase in resistance results and usually the current per unit area increases. Thus VLSI compounds the resistance problem. The effect of a decrease in size can easily be illustrated by the resistance of a simple rectangular conductor with the resistance $R = \rho l/wt$, where ρ is the resistivity. If all spatial dimensions l, w, and t are reduced by a factor α, the new resistance is $R' = R/\alpha$. However, if the vertical thickness t is constant, the scaled resistance remains the same, or $R' = R$. In this case, the major VLSI resistance problem is due to the increase in current density.

The geometries in the resistance problem can be very complicated, consisting of planes and wires having complex shapes as illustrated in [7]. However, the macromodel which results as a solution of the resistance problem for the n terminal currents $\mathbf{I}$ and potentials $\boldsymbol{\phi}$ is simply

$$\mathbf{I} = \mathbf{G}\boldsymbol{\phi}, \tag{1}$$

where $\mathbf{I}, \boldsymbol{\phi} \in \mathcal{R}^n$ and $\mathbf{G} \in \mathcal{R}^{n\times n}$ is the indefinite short circuit conductance matrix [8]. A macromodel is basically a simplified terminal model which allows the analysis of even larger systems [9]. The ith element of the current vector $\mathbf{I}$ is found by integration of $\nabla \cdot \bar{J} = 0$, or

$$I_i = \int_S \bar{J} \cdot \mathbf{n} ds, \tag{2}$$

where $\bar{J}$ is the current density and S is a closed surface including a source of current I_i. We use $\boldsymbol{\phi}$ to indicate the indefinite matrix potentials. If a ground node is defined, Eq. (1) can be expressed in terms of voltages, with $V_{ij} = \phi_i - \phi_j$, where j is the ground node, and

$$\mathbf{I} = \mathbf{G}\mathbf{V}, \tag{3}$$

where $\mathbf{I}, \boldsymbol{\phi} \in \mathcal{R}^{(n-1)}$ and $\mathbf{G} \in \mathcal{R}^{(n-1)\times(n-1)}$

The best computational technique for finding $\mathbf{G}$ depends on many factors, such as required accuracy, the conductor shape, and the size of the problem at hand. The conductor geometry represents a very large boundary value problem. The main approaches used for the solution of this problem are based on differential equation [10] or variational finite element [11] formulations. Earlier, finite differences were expressed in terms of electrical models [10] so that physical models could be used as a means of finding solutions. Today, computer solutions are far superior due to the increased speed and storage capacity of large scale computers.

Chips and packages are usually designed in a planar fashion and the conductor thickness t is generally small. Then a quasi-two-dimensional solution with a uniform current along the thickness suffices for most resistance computations. Figure 2 illustrates two types of nodal grids for the conductor surfaces where the nodal potentials are the unknowns. The grid in Fig. 2(a) is used for finite differences and for some of the finite element solutions, while the triangular cells in Fig. 2(b) are particularly suited for irregular boundary interfaces. The main difference for the various grids is the order of the potential approximation, which is of the form

$$\phi(x, y) = k_1 + k_2 x + k_3 y + k_4 xy. \tag{4}$$

An additional term is included in Eq. (4) for each added node. As an illustration we will match the potential at two points A and B by the cell C_i shown in Fig. 3 and $\phi(x, y) = k_1 + k_2 x$. Then the variation inside C_i is

$$\phi(x, y) = \frac{x_B - x}{x_B - x_A}\phi_A + \frac{x - x_A}{x_B - x_A}\phi_B. \tag{5}$$

The current through cell C_i is measured by the surface $\alpha - \beta$ with a length $|\alpha\beta|$ and the thickness t, with $J = \sigma E = -\sigma(\partial\phi/\partial x)$. Thus Eq. (2) becomes

$$I_i = -\frac{1}{R_{sq}}\int_\alpha^\beta \frac{\partial\phi}{\partial x} dy = -\frac{|\alpha\beta|}{R_{sq}}\frac{\partial\phi}{\partial x}, \tag{6}$$

where the resistance per square is $R_{sq} = 1/\sigma t$. Finally, obtaining $\partial\phi/\partial x$ from Eq. (5),

$$I_i = \frac{|\alpha\beta|}{R_{sq}(x_B - x_A)}(\phi_A - \phi_B), \tag{7}$$

where the conductance of the cell C_i is $G_{AB} = |\alpha\beta|/[R_{sq}(x_B - x_A)]$. The total surface for the current computa-

tion of Eq. (2) for node A is bounded by α-β-γ-δ in Fig. 3 and the external current may be injected at node A. The modified nodal stamp [12] which enters the appropriate contributions in the circuit matrix is

	ϕ_A	ϕ_B	RHS
A	G_{AB}	$-G_{AB}$	0
B	$-G_{AB}$	G_{AB}	0

(8)

From this it is easy to collect all the appropriate contributions for each node. Specifically for node A and all the neighboring nodes the matrix stamp is

	ϕ_A	ϕ_B	ϕ_C	ϕ_D	ϕ_E	RHS
A	$G_{AB} + G_{AC} + G_{AD} + G_{AE}$	$-G_{AB}$	$-G_{AC}$	$-G_{AD}$	$-G_{AE}$	I_i

(9)

Elsewhere in this issue [7] the triangular cell case is discussed, where the potential expansion is $\phi(x, y) = k_1 + k_2 x + k_3 y$ and the current surfaces are the sides of the triangle. The total nodal stamp corresponding to Eq. (9) will have six entries for this case. Further, if we form a finite element with the four nodes A, B, C, D in Figs. 2(a) and 3, the potential function is given by Eq. (4), with all four terms present.

The above discussion illustrates how the finite element equations can be formulated as a circuit problem so that a modified nodal matrix [12] or tableau [13] is formed and a circuit analysis can be performed. Thus the method can easily be employed in conjunction with other circuit elements, as will be the case in Sections 4 and 5. Further steps in the usual network analysis are equation ordering and the efficient solution of the sparse equations. Some of these aspects are discussed in [7] as well.

The circuit matrices formed by stamping in contributions of the type of Eq. (9) are extremely sparse and the solution of systems with several thousand unknowns is feasible. Since most practical problems have only relatively few external nodes in the macromodel, the dimensions of Eq. (3) may be very small, with $n < 100$. Thus, macromodels of the type of Eq. (3) can be formed separately for different parts of the structure, and they can be interconnected by the joining of appropriate nodes. Hence, very large problems are solvable by this approach.

Another application of the resistance model will be the resistances and cell structure in partial element equivalent circuits in Sections 4 and 5. However, the finite element solution represents a different approach from the partial element techniques given below for capacitance and inductance. The main difference between these problems and the resistance problem is the restricted solution

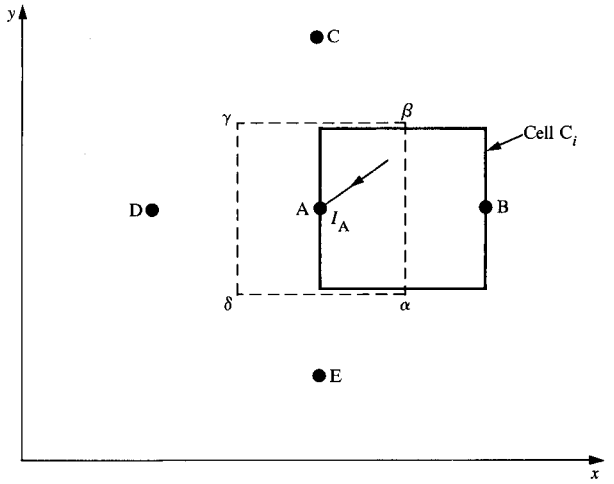

Figure 3 Rectangular cell and current surface.

domain for the resistance which consists of the conducting bodies only. In contrast, coupling exists outside the conductors for both capacitances and inductances.

3. Capacitance computations

Capacitance computations are of central importance for the electrical representation of interconnections. For example, as discussed in Section 1, most connections on FET chips are capacitive since the device impedances are generally much larger than Z_G. The characterization of integrated circuits (ICs) in terms of capacitance matrices is discussed in [14] and the importance of fringing for the ever-decreasing horizontal geometries is quantified in [15, 16] for ICs and for microwave circuits in, for example, [17, 18].

In most applications, there are problems which can be approximated by two-dimensional computations. Examples are transmission lines with a length much larger than the cross-sectional dimensions and spacings. In fact, the first computation with an integral equation matrix method of practical interest was a two-dimensional stripline problem [19]. Today, integral equation methods are in wide use for capacitance computations [17, 18, 20–37] and advances have been made on different aspects of the techniques.

In this paper we give a general integral equation formulation applicable to both two- and three-dimensional geometries which unifies some of the recent developments and includes both finite and infinite dielectric regions. The charge density in the capacitance problem represents surface charge which is denoted by $q(\bar{r})$ for both $\mathcal{R}^2$ and $\mathcal{R}^3$ so that both cases are included by the same formulation.

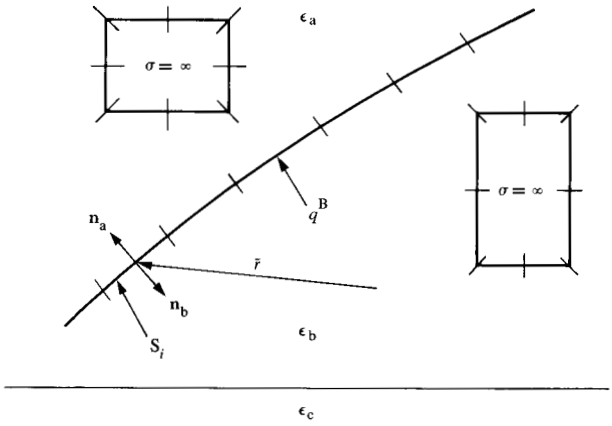

Figure 4 Conductors and dielectric interfaces.

Here, all charges are represented in free space with permittivity ϵ_0 by the total charge concept [38]. The general problem can include finite curved and infinite boundaries as well as arbitrary conductor boundaries, as is illustrated in Fig. 4. If we consider K conductors and I finite interfaces, the potential at $\bar{r}$ is

$$\phi(\bar{r}) = \int_{S_K+S_I} \mathbf{G}(\bar{r}, \bar{r}')q^T(\bar{r}')ds', \tag{10}$$

where S_K and S_I are the conductor surfaces and the interfaces, respectively. Also, q^T is the total charge density with $q^T = q^B + q^F$, where q^B is the bound charge and q^F is the free charge.

All infinite interfaces are taken into account by appropriate two- or three-dimensional Green's functions. For a single dielectric material $\mathbf{G}$ is simply $\mathbf{G}_0(\bar{r}, \bar{r}') = -(2\pi\epsilon_0)^{-1} \ln|\bar{r} - \bar{r}'|$ in $\mathcal{R}^2$ and $\mathbf{G}_0(\bar{r}, \bar{r}') - (4\pi\epsilon_0|\bar{r} - \bar{r}'|)^{-1}$ in $\mathcal{R}^3$. The extension of the Green's function to include infinite dielectric or conductor interfaces can be represented as

$$\mathbf{G} = \sum_n \alpha_n \mathbf{G}_{0_n}.$$

Usually image theory is employed to find both the image strength α_n and the spatial location of the images $\mathbf{G}_{0_n}$.

The form of the images is given by $\mathbf{G}_0$ and details of the image solution are given in [23-25] and [17, 34]. We found that the inclusion of up to three infinite dielectric regions is feasible with Green's functions, while four or more regions result in a much slower solution.

Next, all finite interfaces are divided into N cells as shown in Fig. 3, and thus we can rewrite Eq. (10) as

$$\phi(\bar{r}) = \sum_{j=1}^{N} \int_{S_j} \mathbf{G}(\bar{r}, \bar{r}')q_j^T(\bar{r}')ds'. \tag{11}$$

In the finite element method of Section 2 we approximated the potential by Eq. (4). In contrast to this, we here approximate the charge density in Eq. (11) by a similar approximation on the cell S_j,

$$\begin{aligned} q_j^T(x, y) &= \sum_{m=1}^{M} a_{j,m} b_m(x, y) \\ &= a_{j,1} + a_{j,2}x + a_{j,3}y + a_{j,4}xy \\ &\quad + a_{j,5}x^2 + a_{j,6}y^2, \end{aligned} \tag{12}$$

where the x, y are representative of the surface variables and usually only a few terms [Eq. (12)] are present. The definition of b_m is evident from Eq. (12). The higher-order terms especially lead to complicated integrals over the cell S_j. Inserting Eq. (12) into Eq. (11) yields

$$\phi(\bar{r}) = \sum_{j=1}^{N} \sum_{m=1}^{M} a_{j,m} \int_{S_j} \mathbf{G}(\bar{r}, \bar{r}')b_m(\bar{r}')ds', \tag{13}$$

where $a_{j,m}$ is representative of the unknown charge density. We first concentrate on problems without finite dielectric interfaces and we derive an integral equation of the first kind for this case which results in the solution of a matrix. Equation (13) is multiplied on both sides by b_n where $n \in \{1, 2, \cdots, M\}$, and we choose $\bar{r}$ to be located on cell S_i with $i \in \{1, 2, \cdots, N\}$. Integrating over cell S_i yields

$$\psi'_{i,n} = \sum_{j=1}^{N} \sum_{m=1}^{M} a_{j,m} P'_{S_{i,n,j,m}}, \tag{14}$$

where

$$\psi'_{i,n} = \int_{S_i} \phi(\bar{r})b_n(\bar{r})ds \tag{15}$$

and

$$P'_{S_{i,n,j,m}} = \int_{S_i} \int_{S_j} \mathbf{G}(\bar{r}, \bar{r}')b_n(\bar{r})b_m(\bar{r}')dsds'. \tag{16}$$

Again the only unknowns in Eqs. (14)-(16) are the $a_{j,m}$, since ϕ is known on the K conductor surfaces. If we let $i = 1, 2, \cdots, N$ and $n = 1, 2, \cdots, M$ and we replace the double index pairs i, n and j, m with single indices k and w, we get the matrix system

$$\boldsymbol{\psi} = \mathbf{P}_s \mathbf{a}_p, \tag{17}$$

where $\boldsymbol{\psi}(k)$ and $\mathbf{P}_s(k, w)$ are the appropriate replacements for $\psi'_{i,n}$ and $P_{S_{i,n,j,m}}$, respectively. Once $\mathbf{a}_p$ or equivalently $a_{j,m}$ is known by solving Eq. (17), we can find the total charge on all conductors. Since using the total charge concept [38] $q^F = \epsilon_r q^T$, we can find the free charge as

$$Q_j^F = \int_{S_j} q_j^F(\bar{r})ds = \epsilon_r \sum_{m=1}^{M} a_{j,m} \int_{S_j} b_m(\bar{r})ds, \tag{18}$$

for $j = 1, \cdots, N$. Summing up appropriate cell charges Q_j^F on the conductors we find the capacitances of interest.

An efficient solution for both two- and three-dimensional geometries based on the above formulation is necessary for a multitude of interconnection problems. In many practical cases the problem analyzed is limited by the capabilities of the analysis tool. For some problems symmetry can be exploited to reduce the size of the $\mathbf{P}_s$ matrix in Eq. (17), as is discussed in [39]. In fact, Maxwell [26] used symmetry to obtain a manageable solution for the capacitance of a square plate in free space. The formulation given by Eqs. (14)–(18) corresponds to the Galerkin method if the same approximation function is used in n and m, and further, this approach is equivalent to a variational solution [40–42].

We chose the two conductor problems in Fig. 5 to illustrate how the solution accuracy and complexity are impacted by the approximations of the charge and potential. In this problem, both conductors are located on a dielectric sheet of $\epsilon_r = 10$ with a thickness of $t = 0.635$ mm. We surmise the exact answer to be 450 fF, which may be somewhat in error. However, the percentage error, which is more accurate, gives an understanding of the solution errors involved. In the subarea method [33] in Fig. 5, which corresponds to point matching or $b_n = \delta(\bar{r})$ in Eq. (17), the charge density [Eq. (12)] is constant, or $q_j^T(x, y) = a_{j,1}$. The matching points $\bar{r}$ are at the center of the cells. For about 100 equations, solution errors on the order of 10 to 20 percent result for C_{12}, which shows the largest sensitivity in this problem [37]. A major improvement is obtained for $b_n = 1$ in Eq. (15), as can be seen from the constant charge curve [33], while still maintaining $q_j^T(x, y) = a_{j,1}$. Far fewer equations are required by the approximation equation (12), where only $a_4 = 0$ [36], as shown in Fig. 5. Another important aspect especially for the zero thickness conductors in this problem is the increase of the charge density near the conductor edge. This can be accommodated by choosing smaller cells along the conductor edges. Figure 5 shows the improvement which is obtained by choosing smaller cells along the edge of the conductors. In [35] a singular term is added to the charge expansion of the form $a_1 + a_7(x - x_0)^{-1/2}$, where x_0 indicates the position of the sharp corners. The solution obtained by this approach is also quite accurate for a moderate matrix size. However, this type of charge approximation does not improve the solution for what we call the near conductor problem [37], which occurs if overlapping conductors are placed in close proximity. Large variations of the charges on the surfaces result, and careful placement of the cells and higher-order charge expansions are helpful. It is important to note that the charge expansion can vary for different cell locations.

Next, we include the finite dielectric interfaces shown in Fig. 4 by an integral equation of the second kind in

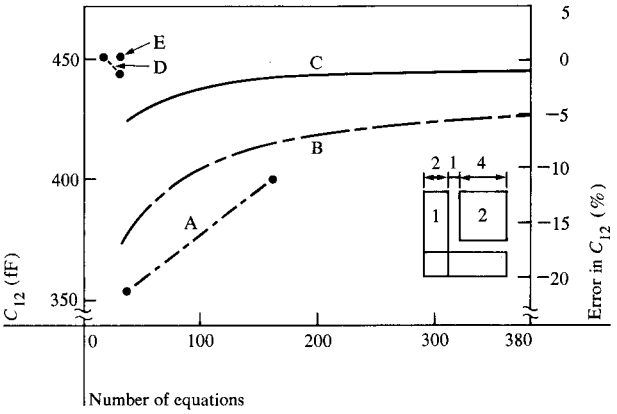

Figure 5 Coupling capacitance *vs.* number of equations: Curve A—subarea [33]; Curve B—constant charge [34]; Curve C—edge cell [34]; Curve D—reference [35]; Curve E—reference [36]. All dimensions in the insert capacitance configuration are in mm.

terms of the total charge density $q^T(\bar{r}) = q^F(\bar{r}) + q^B(\bar{r})$, where q^B is the bound charge and q^F is zero for the dielectric interfaces. Equations of this type have been derived and tested for point matching (collocation) for electric fields [28] and magnetic fields [43]. Further, another nonphysical integral equation is quite common [44]. We start by computing the local electric field due to a charge density $q^T(\bar{r})$ at point $\bar{r}$ in Fig. 4,

$$E_{na} - E_{nb} = \frac{q^T}{\epsilon_0}. \tag{19}$$

The local electric field is symmetric, or $E_{na} = -E_{nb}$, and thus the field contribution E_L just outside the interface on S_i between the two dielectrics is

$$E_L = \frac{q^T}{2\epsilon_0}. \tag{20}$$

The total electric field in the $\mathbf{n}_a$ direction due to all charges in the system is similar to Eq. (13):

$$E_{na}(\bar{r}) = E_L(\bar{r}) + \sum_{\substack{j=1 \\ j\neq i}}^{N} \sum_{m=1}^{M} a_{j,m} \int_{S_j} \frac{\partial \mathbf{G}(\bar{r}, \bar{r}')}{\partial \mathbf{n}_a} b_m(\bar{r}')ds', \tag{21}$$

where $\bar{r}$ is assumed to be close to S_i. Similarly, the total field outside S_i on the ϵ_b side is

$$E_{nb}(\bar{r}) = -E_L(\bar{r}) + \sum_{\substack{j=1 \\ j\neq i}}^{N} \sum_{m=1}^{M} a_{j,m} \int_{S_j} \frac{\partial \mathbf{G}(\bar{r}, \bar{r}')}{\partial \mathbf{n}_a} b_m(\bar{r}')ds' \tag{22}$$

in the $\mathbf{n}_a$ direction. The boundary condition for the free charge is from $\nabla \cdot \bar{D} = q^F$, which for the dielectric interface yields

$$\epsilon_a E_{na} - \epsilon_b E_{nb} = 0, \tag{23}$$

and Eqs. (21)–(23) yield

$$0 = (\epsilon_a + \epsilon_b)\frac{q^T}{2\epsilon_0} + (\epsilon_a - \epsilon_b)\sum_{\substack{j=1\\ j\neq i}}^{N}\sum_{m=1}^{M} a_{j,m}\int_{S_j}\frac{\partial \mathbf{G}(\bar{r}, \bar{r}')}{\partial \mathbf{n}_a} b_m(\bar{r}')ds'. \quad (24)$$

Using Eq. (12) for q^T in the first term on the right-hand side and with the definition $R_{ab} = (\epsilon_a - \epsilon_b)(\epsilon_a + \epsilon_b)^{-1}$, Eq. (24) is rewritten by using Eq. (12) for q^T:

$$0 = \sum_{n=1}^{M} a_{i,n} b_n(\bar{r}) + 2\epsilon_0 R_{ab}\sum_{\substack{j=1\\ j\neq i}}^{N}\sum_{m=1}^{M} a_{j,m}\int_{S_j}\frac{\partial \mathbf{G}(\bar{r}, \bar{r}')}{\partial \mathbf{n}_a} b_m(\bar{r}')ds', \quad (25)$$

where $i \in \{1, 2, \cdots, N\}$. The final form of the integral equation is obtained if we multiply Eq. (25) by b_k and integrate over cell S_i:

$$0 = \sum_{n=1}^{M} a_{i,n}\int_{S_i} b_k(\bar{r})b_n(\bar{r})ds + 2\epsilon_0 R_{ab}\sum_{\substack{j=1\\ j\neq i}}^{N}\sum_{m=1}^{M} a_{j,m}\int_{S_i}\int_{S_j}\frac{\partial \mathbf{G}(\bar{r}, \bar{r}')}{\partial \mathbf{n}_a} b_k(\bar{r})b_m(\bar{r}')ds ds', \quad (26)$$

for $k \in \{1, 2, \cdots, M\}$. We again write this as a matrix equation by defining for $i \neq j$

$$f_{S_{i,k,j,m}} = 2\epsilon_0 R_{ab}\int_{S_i}\int_{S_j}\frac{\partial \mathbf{G}(\bar{r}, \bar{r}')}{\partial \mathbf{n}_a} b_k(\bar{r})b_m(\bar{r}')ds ds', \quad (27)$$

and the first term

$$f_{S_{i,k,n}} = \int_{S_i} b_k(\bar{r})b_n(\bar{r})ds, \quad (28)$$

where the second integral leads to "diagonal-type" elements. The matrix equation for this case is written as

$$\mathbf{0} = \mathbf{F}_s\mathbf{a}_s. \quad (29)$$

Thus, the total system of equations which includes both conductor and dielectric interfaces is given by Eqs. (17) and (29) if all cells are included simultaneously:

$$\begin{bmatrix} \mathbf{P}_s \\ \mathbf{F}_s \end{bmatrix}\begin{bmatrix} \mathbf{a}_p \\ \mathbf{a}_s \end{bmatrix} = \begin{bmatrix} \boldsymbol{\psi} \\ \mathbf{0} \end{bmatrix} \quad (30)$$

The $\mathbf{a}_s$ coefficients are the unknowns for the dielectric interfaces and the $\mathbf{a}_p$ coefficients are involved in the computation of the charges for the capacitances [Eq. (18)]. The formulation equation (30) includes all the interfaces shown in Fig. 4, and it represents a solution for a large class of capacitance problems which will occur in packages like the one shown in Fig. 1.

It is evident from the above discussion that capacitance computations can lead to sizable matrices [Eq. (17) or (30)]. The computational complexity of the solution can be estimated if we make simplifying assumptions about the problem. We assume that the problem consists of $K + I$ conductors and finite interfaces, respectively, and that both are square with n cells per side. Thus the number of unknowns is $n^2M(K + I)$ with M expansion terms per cell according to Eq. (12). The time to compute the matrix coefficients [Eqs. (16) or (27), (28)] is of $O[n^4M^2(K + I)^2]$. If we choose charge expansions leading to symmetric matrices, the solution of the systems of equations is of $O[n^6M^3(K + I)^3]$ for Choleski's method [45]. Thus, for small problems, the matrix element computation dominates due to its complexity, while the solution of the system of equations dominates for large problems. Further, the solution time is greatly affected by n, which is the number of cell divisions per conductor side.

The capacitance computation method presented here yields another result which is useful for further understanding the interconnection problem for LSI and VLSI. If we scale all dimensions in our capacitance formulation [Eq. 30] by a factor α, the resultant capacitances will be $C' = \alpha C$, which is inverse to the scaled resistance considered in Section 2.

4. Inductance computations

Historically, inductance analysis was important in three areas. Lumped coils were used in electronics applications and microstrip lines in microwave circuits, whereas power bus inductances were of interest in power engineering applications. Today's integrated circuit geometries are more closely related to the physically large power bus structures rather than the lumped coils used in electronic circuits. For this reason the early work in power system inductance computations is quite useful for modern problems. For example, Grover [46] includes a large number of references as well as formulas for hand-type calculations.

The computation for two-dimensional geometries such as long power busses or stripline-type geometries is considered in [47] and [48], respectively. These formulas have applications in computer interconnections. Often, two-dimensional approximations lead to valuable insight into three-dimensional cases. Recently, several authors have concerned themselves with three-dimensional inductance computations for integrated circuit type geometries. Specifically in [49], three-dimensional integrated circuit inductances are computed via a building block approach. The building blocks, which are rectangular conductors, are called partial conductors and the problem at hand is subdivided into these conductors. In this approach, the so-called partial self- and partial mutual inductances are computed from

$$L_{p_{km}} = \frac{\mu_0}{4\pi}\frac{1}{a_k a_m}\int_{a_k}\int_{a_m}\int_{b_k}^{c_k}\int_{b_m}^{c_m}\frac{|\overline{dl}_k \cdot \overline{dl}_m|}{|\vec{r}_{b_k} - \vec{r}_m|}\,da_k da_m, \quad (31)$$

where the conductors k and m coincide for the partial self-inductance. The conductor cross-sections are a_k and a_m, while the length coordinates b_k, b_m, and c_k, c_m represent the endpoints as shown in Fig. 6. The inductances in Eq. (31) are called partial inductances to distinguish them from the inductances of the loops and other arrangements.

The effect of scaling down the inductance geometry by a factor α can easily be observed from Eq. (31) by introducing scaled variables. The result is that if the conductor in Fig. 6 is reduced by α in all dimensions, its new partial inductance is $L'_{p_{km}} = \alpha L_{p_{km}}$, which is of the same form as the capacitances in Section 3.

For a system of partial conductors we come up with the partial inductance matrix $\mathbf{L}_p$, where in the s domain

$$\mathbf{V}(s) = s\mathbf{L}_p\mathbf{I}(s). \quad (32)$$

Inductances of the overall physical arrangement are computed using network analysis where **V, I** are the branch voltage and current, respectively. If we specify a set of nodes in the partial inductance network, we compute the inductance from

$$V_i(s) = s\sum_{j=1}^{n} L_{p_{ij}} I_j(s), \quad (33)$$

where $I_k = 0$ for $k \neq j$, for $\mathbf{L}_p \in \mathcal{R}^{n\times n}$. Thus all currents are set to zero, except for the source applied at the partial conductor j while the voltage is measured at the terminals of inductance $\mathbf{L}_{p_{ij}}$.

Inductances for shapes other than the partial conductor in Fig. 6 have been considered in [50–52]. The current in both the two- and three-dimensional partial conductor cross-sections is assumed to be uniform. This yields low frequency inductances, since it is well known that at very high frequencies the current density is nonuniform. However, the effect of the nonuniform current density on the inductance value is small if the distance between the conductors is much larger than the cross-sections, and the accuracy of the uniform current computation is often sufficient for the entire frequency range.

An integral equation-circuit solution can be set up for the solution of the skin effect or current redistribution problem in the cross-section of two-dimensional conductors [48, 53, 54]. The integral equation for the current density for each of a set of two-dimensional conductors is of the basic form

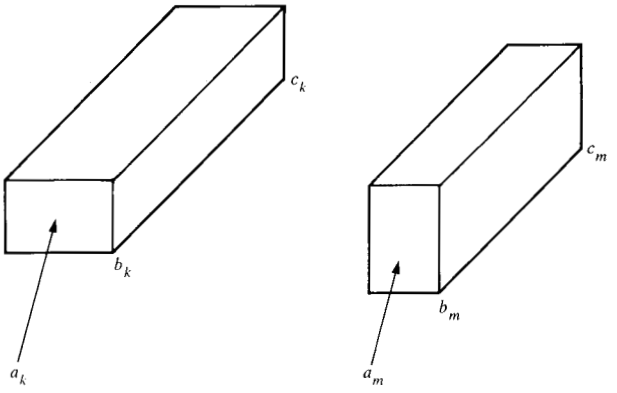

Figure 6 Two partial conductors.

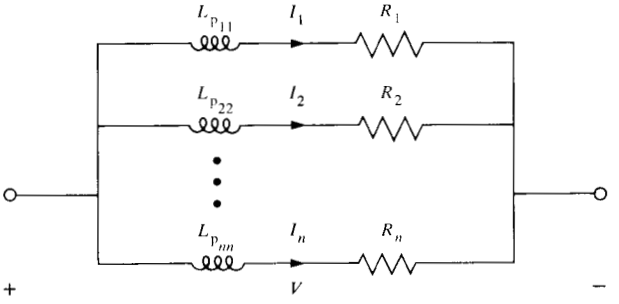

Figure 7 Equivalent circuit for inductance per unit length.

$$\frac{J(\vec{r})}{\sigma} + \frac{j\omega\mu_0}{2\pi}\int_a \ln|\vec{r} - \vec{r}'|J(\vec{r}')da' = V(\vec{r}), \quad (34)$$

where σ is the conductivity and J the current density in the conductor cross-section a. This can be transformed into an equivalent circuit in the form of Fig. 7 by discretization. The solution of the frequency-dependent inductance and resistance can be found from a set of equations which correspond to the circuit in Fig. 7, or

$$\mathbf{RI} + s\mathbf{L}_p\mathbf{I} = \mathbf{V}. \quad (35)$$

If we rewrite Eq. (35) in state variable form in the time domain,

$$\frac{d\mathbf{i}(t)}{dt} = -\mathbf{L}_p^{-1}\mathbf{R}\mathbf{i}(t) + \mathbf{L}_p^{-1}\mathbf{v}(t), \quad (36)$$

we can see that an alternate solution method to the homogeneous equation can be stated as an eigenvalue problem,

$$\mathbf{L}_p^{-1}\mathbf{RI} = \lambda\mathbf{I}, \quad (37)$$

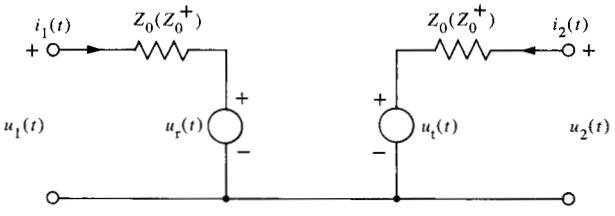

Figure 8 Voltage source model for transmission line.

where λ is the eigenvalue. The relative efficiency of the solutions of the matrix solution compared to the eigenvalue solution depends on the numerical techniques and the particular $\mathbf{L}_p$ matrix. Details concerning the matrix solution together with measured results for a two-dimensional skin effect problem are considered in more detail in this issue [48].

The three-dimensional skin effect problems can be treated in a similar way by a three-dimensional integral equation. Again, we will not give details here since this issue includes a derivation [55], together with example applications. Other examples of similar problems are given in [56–58]. We call the equivalent circuits which result from the integral equation *partial element equivalent circuits* (PEEC), as opposed to the finite element solution of Section 2. The solution in the time domain for the **L**/**R** problems can be given in the form

$$\begin{bmatrix} -\mathbf{A}^T & \mathbf{R} + \mathbf{L}_p \dfrac{d}{dt} \\ 0 & \mathbf{A} \end{bmatrix} \begin{bmatrix} \mathbf{v}(t) \\ \mathbf{i}(t) \end{bmatrix} = \begin{bmatrix} 0 \\ \mathbf{I}_s(t) \end{bmatrix}, \tag{38}$$

where the $\mathbf{I}_s(t)$ are the forcing current sources and **A** is the incidence matrix.

The case where $\mathbf{R} = 0$ is very useful if the solution for small t is of interest [59]. This leads to a greatly simplified problem, and hence larger problems can be solved. In the future $\mathbf{L}_p$ matrices larger than 1000×1000 will not be uncommon, as is evident from [55].

5. Electrical models and analysis

Electrical circuit models are key to the analysis approach pursued here, and several advantages result from this approach. The interfaces among submodels like the digital circuits or gates and the package models are in terms of voltages and currents, which are measurable quantities. The possible coupling among the submodels is specified in terms of mutual capacitances and inductances. Approximations in terms of these variables are well known to the design engineers, and a good understanding is obtained of the purpose and functioning of the hardware.

From an analytical point of view, concepts are combined from mathematics, electromagnetic theory and circuit theory. Besides the geometrical details of the interconnections, we must know what drivers and receivers are connected to them, with appropriate electrical circuit models or macromodels [9, 60, 61]. The interconnection geometry can be viewed as a large boundary value problem, while the resistance, capacitance, and inductance problems considered in the last three sections each represent only one aspect of the general problem. However, complete methods or models include all three types of elements.

Some of the early work in computer interconnection modeling [62–73] concentrated on the transmission line nature of the source to sink connections among the logic circuits or gates. These models allow the prediction of possible reflections with the waveshape distortion and coupling among the lines. The analysis of larger interconnection nets prompted the development of approaches suitable for computer-aided analysis [74–78]. The key transmission line model in this approach is the voltage source model shown in Fig. 8, which is based on the method of characteristics from the theory of partial differential equations. The reflected voltage in Fig. 8 is

$$u_r(t - \tau) = u_2(t) - Z_0 i_2(t), \tag{39}$$

while the transmitted voltage is

$$u_t(t - \tau) = u_1(t) - Z_0 i_1(t), \tag{40}$$

where τ is the delay and Z_0 the characteristic impedance $Z_0 = (L/C)^{1/2}$. The lossless nature of this model restricts its applications, and the inclusion of losses is the subject of many papers [79–85]. For example, a resistance R in series to the section of transmission line shown in Fig. 8 is accommodated by defining new impedances $Z_0^+ = Z_0 + R/2$ and $Z_0^- = Z_0 - R/2$. The new impedances in Fig. 8 are Z_0^+ as indicated, and the voltage source equations are

$$u_r(t - \tau) = u_2(t) - Z_0^- i_2(t) \tag{41}$$

and

$$u_t(t - \tau) = u_1(t) - Z_0^- i_2(t). \tag{42}$$

This model applies only to short resistive lines; extensions for long lines are given in [80] and also in [79] for multiple resistive transmission lines. Other authors have made attempts to include the skin effect [81–84] in their models. For example, in [83, 84] an approach which we call the "synthesis technique" is employed. Basically, the impedance of a section of transmission line is obtained from a complex subdivided model given by Eq. (35). From this, simple frequency domain equivalent circuits are synthesized which exhibit the same frequency

behavior. These simple synthesis models are employed in distributed-lumped lossy transmission line models.

Another important transmission line problem which requires special attention is the propagation of signals on high performance on-chip interconnections. As is shown in Fig. 9(a), the silicon substrate represents a lossy ground return plane for the signals on the wire. It was first shown in [85] that for $\epsilon_{ox} < \epsilon_{Si}$ and $t_{ox} << t_{Si}$ the structure supports slow waves. Subsequent publications [84, 86–89] provide further insight and models for the slow wave problems. A simple physical model for the phenomenon is given in Fig. 9(b). For a range of frequencies within the pulse spectrum the capacitance of the equivalent transmission line is given in Fig. 9(b) by the oxide capacitance, which is large since t_{ox} is small. Further, the inductance is large since the current penetration or skin effect in the silicon leads to a remote return path and a much larger delay $d = (LC)^{1/2}$ results, which is very undesirable. Delays of 0.3 ns/cm are not uncommon.

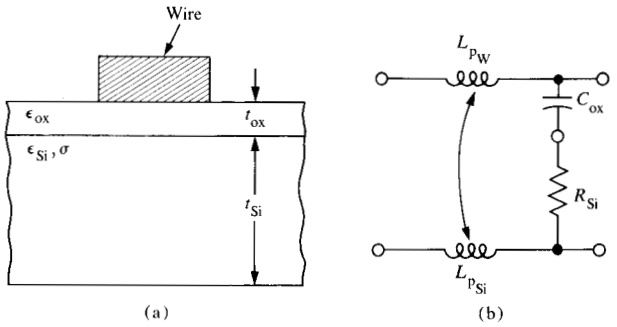

Figure 9 Wire on silicon and circuit model: (a) Cross-section of wire on Si and (b) equivalent circuit model.

In a general model we can have all combinations of dominant circuit elements for R, L, and C depending on the particular hardware configuration to be analyzed. The case where R and C dominate is of importance for lower-speed FET transistor circuits, and in [89] transmission lines of this type are considered, while a two-dimensional RC model is given in [90]. In a large class of problems the complete three-dimensional nature, including L, R, and C, must be taken into account. In [91] and [92] an integral-equation-based equivalent circuit solution is given, leading to partial element equivalent circuits (PEEC). Three-dimensional time domain or frequency domain solutions are obtained if the PEECs are used in conjunction with a general purpose network analysis program [93].

The PEECs are derived by summing all sources of electric field inside a conductor,

$$\tilde{E}_0(\bar{r}, t) = \frac{\tilde{J}(\bar{r}, t)}{\sigma} + \frac{\partial \tilde{A}(\bar{r}, t)}{\partial t} + \nabla\phi(\bar{r}, t), \tag{43}$$

where $\tilde{E}_0$ represents an applied field. Both the vector and scalar potentials $\tilde{A}$ and ϕ respectively are expressed in terms of integrals,

$$\tilde{A}(\bar{r}, t) = \sum_{k=1}^{K} \frac{\mu}{4\pi} \int_{V_k} \frac{1}{|\bar{r} - \bar{r}'|} \tilde{J}(\bar{r}, t')dv' \tag{44}$$

and

$$\phi(\bar{r}', t) = \sum_{k=1}^{K} \frac{1}{4\pi\epsilon} \int_{V_k} \frac{1}{|\bar{r} - \bar{r}'|} q(\bar{r}, t')dv', \tag{45}$$

where K conductors are involved in the system. A derivation in [92] shows that Eq. (44) leads to partial inductances of the form of Eq. (31). The derivation for the capacitance from Eq. (45) leads to a concept called partial capacitance. Partial capacitance should not be confused with the German "Teilkapazitaet," which is used for the usual multiconductor capacitances [14] for complete conductors. Partial capacitances are required to represent surfaces which become nonequipotentials under time domains or high frequency excitation. Specifically, Fig. 10 shows a cell configuration similar to Fig. 3 where we compute resistances (R_3) and partial inductances ($L_{P_{33}}$) for cells such as the one between nodes 3 and 5. Further, the surface cells (solid line for node 5 and dash-dot line for node 3) are capacitance cells which are electrically disconnected by an infinitesimal gap. Thus, the partial capacitance between them ($C_{P_{35}}$) is finite and it can easily be computed by the techniques given in Section 3. A PEEC for the cells in Fig. 10 is shown in Fig. 11, where all nonperpendicular inductances $L_{P_{ij}}$ are coupled and the partial capacitances are specified in terms of a short circuit capacitance matrix [14].

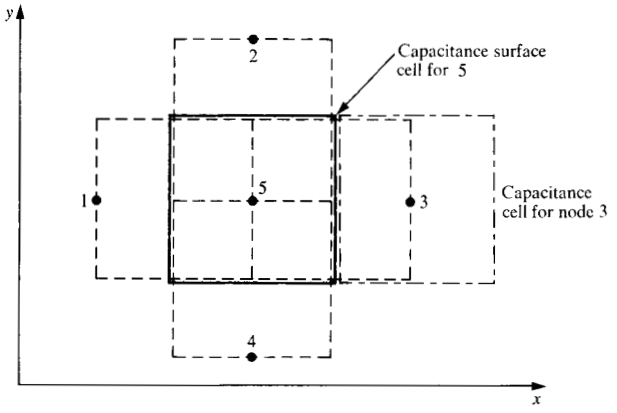

Figure 10 Cell structure for PEEC.

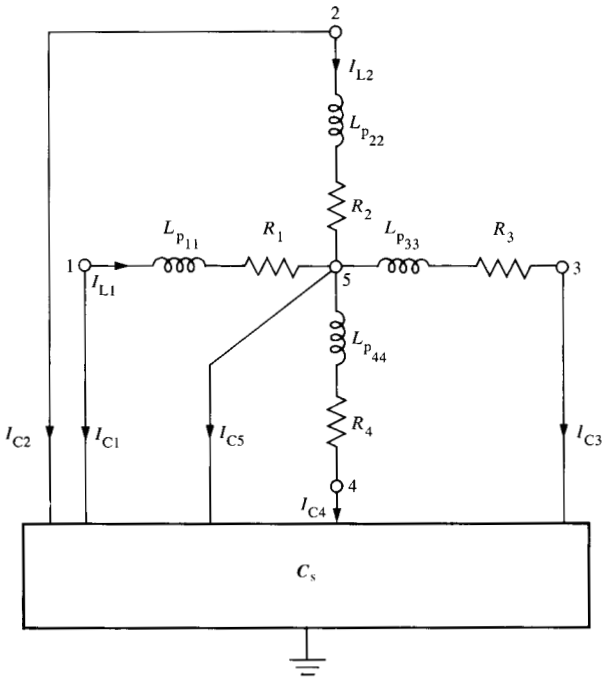

Figure 11 PEEC for node 5.

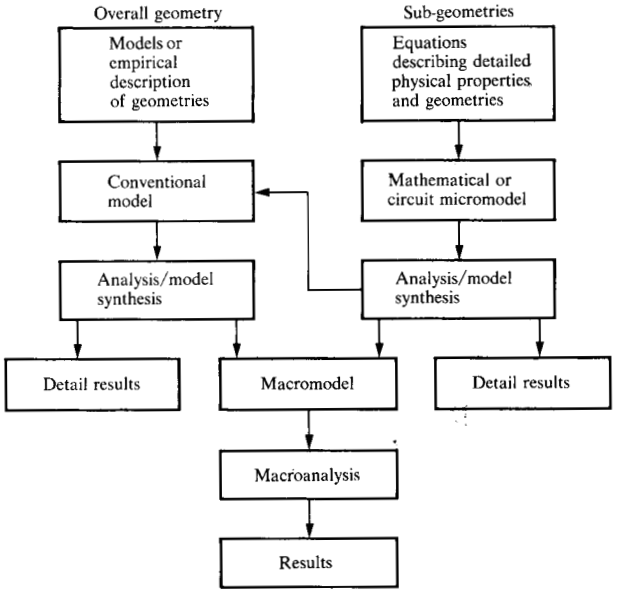

Figure 12 Unified modeling and analysis approach.

The circuit analysis of PEECs is performed using a general purpose program [93] for moderately sized problems. However, it is obvious that the number of elements can grow rapidly with the problem size. For example, the number of partial capacitances is $O(N^2)$ for N nodes. Advantages can be gained by tailoring an analyzer to the interconnection networks [94]. A circuit matrix for the PEEC of Fig. 10 can be written with h being the time step,

	V_1	V_2	V_3	V_4	V_5	I_{L1}	I_{L2}	I_{L3}	I_{L4}
1	$\frac{C_{s_{11}}}{h}$	$\frac{C_{s_{12}}}{h}$	$\frac{C_{s_{13}}}{h}$	$\frac{C_{s_{14}}}{h}$	$\frac{C_{s_{15}}}{h}$	1			
2	$\frac{C_{s_{21}}}{h}$	$\frac{C_{s_{22}}}{h}$	$\frac{C_{s_{23}}}{h}$	$\frac{C_{s_{24}}}{h}$	$\frac{C_{s_{25}}}{h}$		1		
3	$\frac{C_{s_{31}}}{h}$	$\frac{C_{s_{32}}}{h}$	$\frac{C_{s_{33}}}{h}$	$\frac{C_{s_{34}}}{h}$	$\frac{C_{s_{35}}}{h}$			1	
4	$\frac{C_{s_{41}}}{h}$	$\frac{C_{s_{42}}}{h}$	$\frac{C_{s_{43}}}{h}$	$\frac{C_{s_{44}}}{h}$	$\frac{C_{s_{45}}}{h}$				1
5	$\frac{C_{s_{51}}}{h}$	$\frac{C_{s_{52}}}{h}$	$\frac{C_{s_{53}}}{h}$	$\frac{C_{s_{54}}}{h}$	$\frac{C_{s_{55}}}{h}$	-1	-1	-1	-1
BR1	-1				$+1$	$R_1 + \frac{L_{p_{11}}}{h}$		$\frac{L_{p_{13}}}{h}$	
BR2		-1			$+1$		$R_2 + \frac{L_{p_{22}}}{h}$		$\frac{L_{p_{24}}}{h}$
BR3			-1		$+1$	$\frac{L_{p_{31}}}{h}$		$R_3 + \frac{L_{p_{33}}}{h}$	
BR4				-1	$+1$		$\frac{L_{p_{42}}}{h}$		$R_4 + \frac{L_{p_{44}}}{h}$

(46)

using a Modified Nodal-Tableau type formulation [12, 13]. The network is linear and the structure of the circuit matrix is well defined [94]. Sparsity can be introduced in the matrix by ignoring small coupling elements since only relatively large voltages are of interest for the coupled noise signal analysis.

In general, different models and analysis approaches are combined [95] to find out whether a system meets the design goals given in Section 1. Several circuit matrices must be interfaced by using techniques [96] developed recently for mixed multilevel macromodeling. These approaches are designed to allow the analysis of large electrical networks. For example, we can use macromodels to simplify problems in terms of resistances [Eq. (3)] or inductances [Eq. (38)]. Substantial savings can be obtained using this approach in a general situation. The analysis approach for the interconnections of a complex hardware system in terms of the techniques presented above is shown in Fig. 12. Subgeometries or details are represented by what we call micromodels. Examples of inductance micromodels are given in [55]. Analysis and synthesis techniques are employed to abstract the global behavior from the synthesis model. These models are employed in conjunction with other models for the overall analysis, as is shown in Fig. 12. The overall analysis is performed in terms of macromodels as much as possible to reduce computation time and to allow the analysis of very large subportions of a hardware system.

Finally, it is noted that the main topic of this paper is analysis rather than design. Today's analysis techniques are presently evolving and are still incomplete. Since design relies on efficient analysis, we expect that design techniques will be emerging in the future. Two examples of design methods which involve interconnections in a digital system are given in [97, 98].

6. Conclusions

The electrical analysis of hardware interconnections is a new, evolving field. In this survey a coherent framework for the solution of these problems is established which draws on many different disciplines such as numerical analysis, solution methods for boundary value problems, and electromagnetic and circuit theory. Some of the techniques used, like the inductance analysis of complex geometries, are well understood today. Problems with hundreds of subconductors can be analyzed. The macromodeling of these large problems is an area which is presently evolving. Other areas, such as capacitance computations, are limited today to relatively small problems involving less than one hundred subconductors. Thus, hardware such as that illustrated in Fig. 1 must be analyzed in terms of subproblems by the approach outlined in Fig. 12.

7. Acknowledgments

Many of my colleagues at IBM have contributed to the understanding presented here. During my involvement in the DA and CAD areas I had the opportunity to cooperate closely with P. A. Brennan, H. Y. Hsieh, C. W. Ho, B. S. Landman, N. B. Rabbat, H. Young, P. K. Wolff, and D. A. Zein.

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