A. Reisman
K. C. Park

AC Gas Discharge Panels: Some General Considerations

Abstract: This introductory paper attempts to provide some perspective on the key technology issues associated with ac gas panel displays to set the stage for a series of nine technology and physics-oriented papers that follow. It uses the cathode ray tube as a reference for comparison and defines some of the unique technological features of matrix-addressed displays generally and ac gas discharge panels specifically.

Introduction

The following text is intended to introduce the series of nine papers on ac plasma display panels that follow, to provide some perspective on why this emerging technology looks attractive, and to point up key issues that require resolution in order for it to achieve its full potential. Some of these issues are common to matrix-addressed displays generally, e.g., the cost of fabricating arrays of electrodes, while others are specific to gas panels, e.g., guaranteeing the hermeticity of a gas envelope containing a large surface to volume ratio.

When considering the pros and cons of developing the technical base for a relatively large area, new display technology whose main area of applications is in alphanumerics, and perhaps graphics, the reference for comparison must be the cathode ray tube. When only a limited number of display spots (picture elements, pixels) are required for a display, i.e., up to a few thousand, which translates into 20–30 alphanumeric character boxes, several useful technologies are available. These include liquid crystals, light emitting diodes, and electroluminescents. When a larger number of character boxes are required, technological and/or cost considerations make these technologies unattractive. It is in this regime that the CRT is pervasive. However, this device has certain shortcomings, which has led to a continuing search for alternatives, the gas panel being preeminent amongst them.

The areas in which the gas panel looks good in comparison to the CRT are that:

1. CRT's exhibit marginal contrast ratios, about 3 to 7, and pixel stability leaves much to be desired. Both of these factors contribute to eye fatigue.
2. When pixel count increases to the 10^6 range, flicker becomes a problem due to the difficulty in refreshing the scanned area. While this deficiency can probably be overcome, it can only be done by incurring a significant cost erosion.
3. CRT's are most suitable from a cost point for displays that are geometrically square. When display aspect ratios are high, e.g., a two-line, 80-character display, the fixed electronics and packaging costs lead to under-utilization of the device.
4. CRT's are structurally bulky, and because of restrictions on beam deflection techniques, increasing face plate size requires a proportionate increase in the third dimension.
5. Finally, because of the difficulty of increasing the number of lines/inch in the vertical direction in the CRT, increasing face plate size normally results in decreased line/inch resolution in this direction.

The ac plasma panel, on the other hand, has high contrast ratios (in the 25 to 30 range), extremely stable pixel location because it is matrix addressed, is free of flicker because it has intrinsic memory, is useful for square and high aspect ratio applications without under-utilization problems, and can be increased in size in two dimensions without requiring an increase in size in the third dimen-

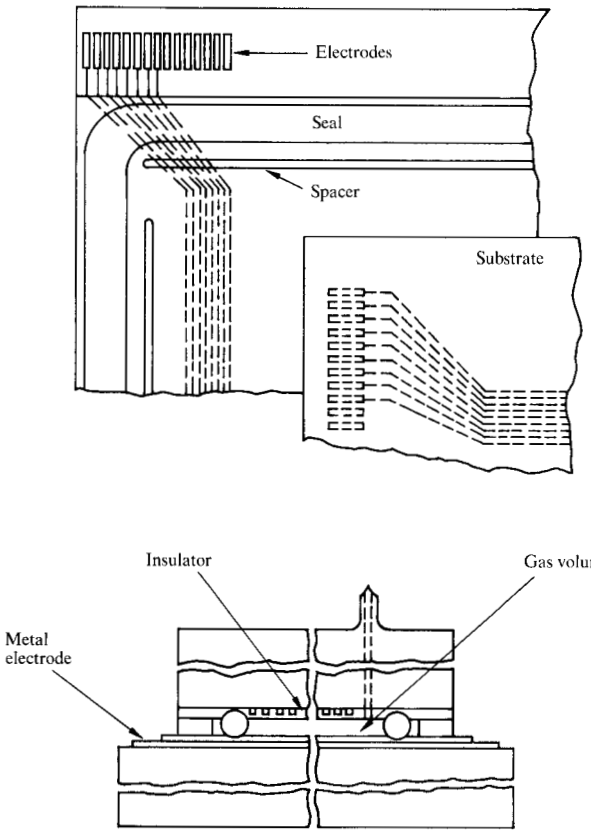

Figure 1 Schematic representation of an ac display panel [4].

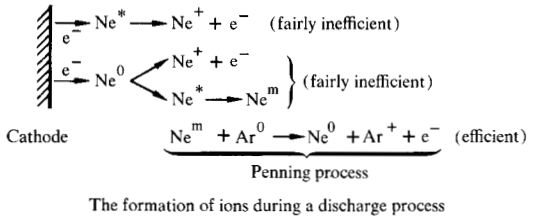

Figure 2 Reactions leading to a Penning process where Ne* is an activated neon atom and Ne^m is a metastable neon atom.

sion. The basic device was invented at the University of Illinois in 1964 [1, 2], and is depicted schematically in Fig. 1. It consists of two glass plates spaced several thousandths of an inch apart, which form a hermetic envelope. On the interior of this envelope, orthogonal arrays of electrodes are formed whose ends pass through the seal of the envelope for contacting purposes. These electrode arrays are overcoated in turn with insulating and secondary-electron emission layers, respectively, and the interior of the envelope is filled with a gas discharge mixture. While many gases are suitable potentially, plasma panels exhibiting intrinsic memory make use of Penning mixtures [3] such as neon-argon, the latter being present in the low parts per thousand concentration range. Because of the geometrical arrangement of the panel interior, discharge is achieved via capacitive coupling of applied ac voltages, and unlike dc panel designs where electrodes are exposed to the discharge, sputter erosion of the electrodes is not a problem. Further, if one chooses a refractory secondary-electron emission layer such as MgO, erosion of this surface is essentially zero. Schematically, a Penning process is depicted in Fig. 2.

When ac voltages are applied to chosen electrodes, the field is coupled capacitively to the gas mixture, initiating the discharge process, which is relatively inefficient except for the Penning process itself, which is described in the last equation. The generated argon and neon ions bombard the secondary-electron emission layer of opposite polarity during each ac cycle causing emission of secondary electrons. These electrons plus those generated by the other processes described in Fig. 2 are in turn stored on the alternating anode surface generating an internal wall voltage which is added to the applied voltage. Since the gas capacitance is significantly smaller than the insulator capacitance, i.e., ca. 10% of the latter, most of the field drops across the gas. Consequently, once the discharge is initiated, the application of a simple sustain voltage waveform is sufficient to keep the discharge going at those pixels which were ignited initially by applied write pulses. Thus, the device exhibits intrinsic memory and is free of flicker.

The effectiveness of initiating and then sustaining the discharge are functions of the secondary-electron emitter used, the field-dependent secondary-electron emission coefficient, and the nature of the bombarding gas. Details of these interdependencies and the effects of surface contaminants have been discussed earlier [4, 5].

In the use of a gas panel, one distinguishes between two voltage levels referred to as maximum and minimum sustain voltages, where it is to be recalled that the sustain voltage is that voltage which when continuously applied will keep a previously lit pixel in the lit state. This sustain voltage waveform is applied continuously to each electrode and might be thought of as a bias voltage. It is only when a write or erase pulse is superimposed over this constantly applied sustain voltage that a pixel is lit or erased.

The maximum sustain voltage, V_s^{max}, is akin to the breakdown voltage of the discharge gas. It is the maximum voltage that can be used to bias the device which will enable permanent erasure of a lit pixel via superposition of an erase pulse. The minimum sustain voltage, V_s^{min}, on the other hand, is the smallest bias which will sustain a discharge following application of a write pulse.

In a simplified fashion we can think of the maximum sustain voltage as that voltage which requires little or no stored wall charge to initiate gas breakdown, and the minimum sustain voltage as the smallest bias which together with stored wall charge provides a sufficient field for gas breakdown to occur.

The voltage difference, ΔV, between maximum and minimum sustain voltages is a key electrical parameter referred to as voltage margin or operating window. As shown schematically in Fig. 3, the margins for each of the pixels comprising the panel display must overlap or else the panel as a whole will not exhibit a useable margin, i.e., a single sustain waveform of defined amplitude will not serve as a bias for the entire panel. On the left-hand side of Fig. 3, for example, it is seen that application of a single voltage in the region of overlap is sufficient to provide the necessary bias which enables write and erase operations. Such a window does not exist in the case shown on the right-hand side of Fig. 3. For example, if a sustain voltage lying between V_s^{max} and V_s^{min} of the left pixel is applied to the panel, the right pixel cannot be maintained in a lit state since the sum of stored and applied voltage would lie below V_s^{max} of the right pixel. Similarly if a voltage lying between V_s^{max} and V_s^{min} of the right pixel is used for biasing, the left pixel is not permanently erasable since this bias voltage exceeds the breakdown voltage of the gas.

Panel margin is affected by surface cleanliness, surface homogeneity, insulator thickness uniformity, interplate spacing uniformity, secondary-electron emission characteristics of the emitter, linewidth uniformity, gas pressure, and gas composition. Panel margin dependencies and related questions are discussed in the papers by O'Hanlon et al. [6], Ahearn and Sahni [7], Schlig and Stilwell [8], Lanza and Sahni [9], and O'Hanlon [10]. Fabrication of panels to control these parameters is described in the papers by Reisman et al. [11], Park and Weitzman [12], Brusic et al. [13], and Hammer [14].

With this simplified description of gas panel operation, let us now consider some of the technology questions involved in fabricating reliable, cost competitive ac plasma panels and possible answers to these questions. In order to provide some orientation let us first examine what might be considered a conventional gas panel fabrication process such as is described in Fig. 4.

1. In the first step, cleaned glass plates are metallized, preferably using thin film deposition techniques. Then electrode arrays are photolithographically delineated.
2. Next a fine glass frit suspended in a suitable vehicle is sprayed onto the plates, and the latter are taken through a thermal cycle during which time the frit flows out over the electrodes. The maximum temperature during this dielectric reflow cycle must be less than that which would cause deformation of the glass plates themselves, and the electrodes and molten glass must be compatible during the reflow cycle.
3. A secondary-electron emission layer is then applied to each plate.
4. A top and bottom plate pair are joined together in a sealing cycle using a suitable sealing glass. The maximum temperature in the sealing operation must be less than that at which the dielectric would soften, to avoid crazing of the secondary-electron emission layer, thereby destroying its homogeneity. During this sealing cycle, a glass tube is simultaneously joined to one of the plates to enable subsequent evacuation at elevated temperature to clean the panel interior, followed by gas filling of the discharge gas to a desired pressure prior to tipping off the filling port. The end result is shown in Fig. 5. It is essentially a gas sandwich be-

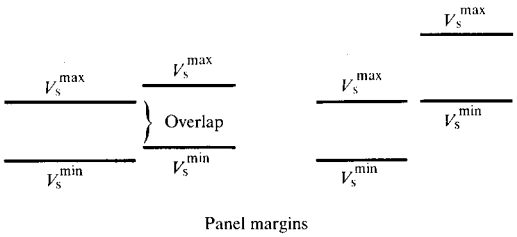

Figure 3 Schematic representation of voltage operating margins where V_s^{max} is the maximum sustain voltage and V_s^{min} is the minimum sustain voltage.

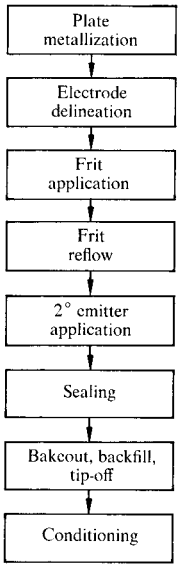

Figure 4 Block processing diagram of a panel fabrication process.

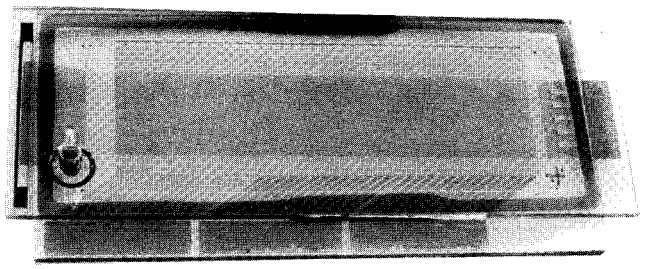

Figure 5 Photograph of an ac gas discharge panel.

N_2 leak rate		Time (h) for three panel volumes		
(Tl/s)	(Pa-m^3/s)	*1 cc*	*3 cc*	*5.5 cc*
10^{-8}	1.3×10^{-9}	1	3	5.5
10^{-10}	1.3×10^{-11}	100	300	550
10^{-12}	1.3×10^{-13}	10 000	30 000	55 000
10^{-14}	1.3×10^{-15}	1 000 000	3 000 000	5 500 000

Assume 3-cc panel has ≈600 lines; leak rate/line ≈1.66×10^{-17} Tl/s (≈2.2×10^{-18} Pa-m^3/s) in the last case.

Figure 6 Seal leak integrity relationships. Assume an end of life = 100 ppm N_2 contamination.

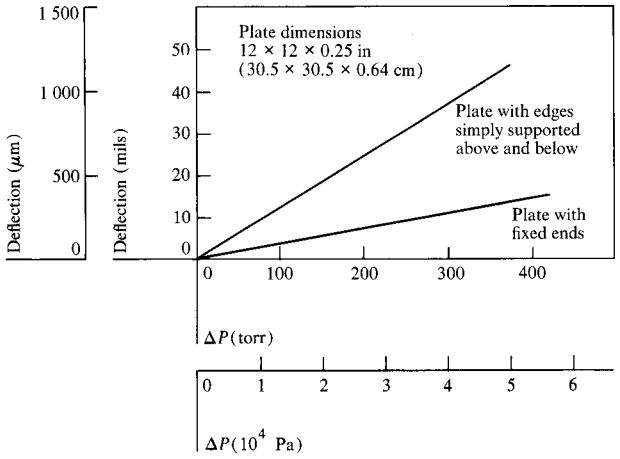

Figure 7 Pressure-deflection relationships for 30.5 × 30.5 × 0.64-cm glass plates. Maximum deflection per plate is shown as a function of change in atmospheric pressure.

tween two plates of glass with several cubic centimeters of gas looking at many square inches of surface, and hundreds of electrodes passing through the seal to the outside world where each must be connected to a driver circuit.

The greatest starting cost penalty in the outlined process is the formation of the array of electrodes. Not only are there yield questions, particularly as the panel gets larger and larger, but there is simply the unyielded cost of metal delineation to be contended with, a costly process by comparison when it is remembered that the CRT has only a few wires passing through its neck. Another problem is that the electrodes must be able to withstand the rigors of elevated-temperature-air processing, thereby limiting the choice of electrode materials and/or their configuration.

Another concern is the melting point hierarchy involved in fabrication. Outwardly, one has a large number of glass systems to choose from, but if a constraint is invoked that thermal mismatch within such systems must not lead to stresses in excess of 10^9 dynes/cm^2 (10^8 Newtons/m^2) (preferably compressive), the number of useable glasses shrinks to a very small number indeed. This number shrinks further if glass-metal interactions must be taken into account.

Next we are confronted with the requirement of leak integrity. Let us assume that gas contamination by as little as 100 ppm of contaminant will cause serious degradation of panel characteristics. Quantitative data are presented by Ahearn and Sahni [7]. Figure 6 shows how this 100 ppm number translates into required leak integrity values for panels containing different realistic quantities of gas. If one requires 30–40 thousand hours of operating life plus shelf life, it is necessary to achieve overall panel leak rates of the order of 10^{-13} torr liters/s (≈10^{-14} Pa-m^3/s), and individual electrode leak rates of 10^{-16}–10^{-17} torr liters/s (≈10^{-17}–10^{-18} Pa-m^3/s). These are rather demanding ground rules. Measurement techniques for studying panel absolute leak rates are discussed by O'Hanlon et al. [6].

Since the pressure inside a completed panel is generally less than atmospheric, it is necessary in larger panels to employ spacers in their interior to prevent elastic deformation of the plates under this differential, ΔP. Figure 7 shows the extent of such deformation, as measured by Reisman and Berkenblit [15] in 0.25-in.-thick, 12 × 12-in. (0.64 × 30.5 × 30.5-cm) plate glass as a function of ΔP. Approximately 10–30 torr (1.3×10^3 to 4×10^3 Pa) pressure differentials, depending on edge pinning of the plates, causes a collapse of approximately one mil (25 μm) in each plate, with panel spacing normally being only 2–4 mils (50–100 μm) in the first place. Maintaining panel interplate spacing is important, since operating margin is dependent critically on the *Pd* product. This relationship is shown in Fig. 8, which depicts the sustain voltages as functions of the pressure, *P*, interplate spacing, *d*, product, the Paschen curve [16]. With the pressure uniform, as it would be in a sealed panel, the *Pd* product is a function of the value of *d*. If *d* varies over a panel,

then it is evident that neither the overall panel voltage margin nor the actual operating voltages will be constant. In fact, margin may cease to exist entirely. In practice, a pressure near the Paschen minimum is used to reduce panel-to-panel and intrapanel margin fluctuations. Scaling considerations relative to the minimum in the Paschen curve are discussed by O'Hanlon [10].

Having completed the recounted fabrication process steps, one might expect the end result to be an operable panel. However, employing these more or less conventional steps it may be found that:

1. The panel is difficult to ignite;
2. Once ignited the panel must be maintained in a lit state at excessive voltages for an extended time period to allow the surface to be sputter-cleaned by the action of the bombarding ions.

During this so-called "burn-in" conditioning process, normally involatile contaminants are presumably relocated to the inactive peripheral regions of the panel interior. This assumption has yet to be verified and is difficult to verify because of the inability to probe the panel interior *in situ*. Questions concerning panel stabilization are discussed by O'Hanlon et al. [6].

For a number of years a group at the IBM Thomas J. Watson Research Center has been attempting to evolve an overall fabrication technology which overcomes some of the cost and/or technical deficiencies associated with the more or less conventional process just outlined.

Cost and yield questions associated with electrode delineation via photolithographic techniques have already been mentioned. Alternatives to photolithographic delineation methods, such as, for example, through-mask deposition, must be relatively inexpensive, durable, process-stable, capable of supporting free-standing structures, and useable with line forming methods that are essentially immune from dust particle effects. One possible solution to this aspect of fabrication is discussed by Hammer [14].

Along with the development of this potentially inexpensive electrode delineation method, the effects of linewidth variation on panel operation have been examined. These effects, on margin particularly, are not trivial and are discussed by O'Hanlon [10].

A second area of intensive study has involved the development of a single-layer, high-temperature, oxidation-resistant metallurgy that is able also to withstand the corrosive environment associated with molten seal glasses. Such an alloy based on copper doped aluminum has been developed, and details concerning this corrosion-resistant metallurgy are given by Brusic et al. [13].

A third area of intensive study has been concerned with formation of the insulating dielectric layer which encompasses the electrode arrays. The intent has been aimed at breaking up the melting point hierarchy, and making this

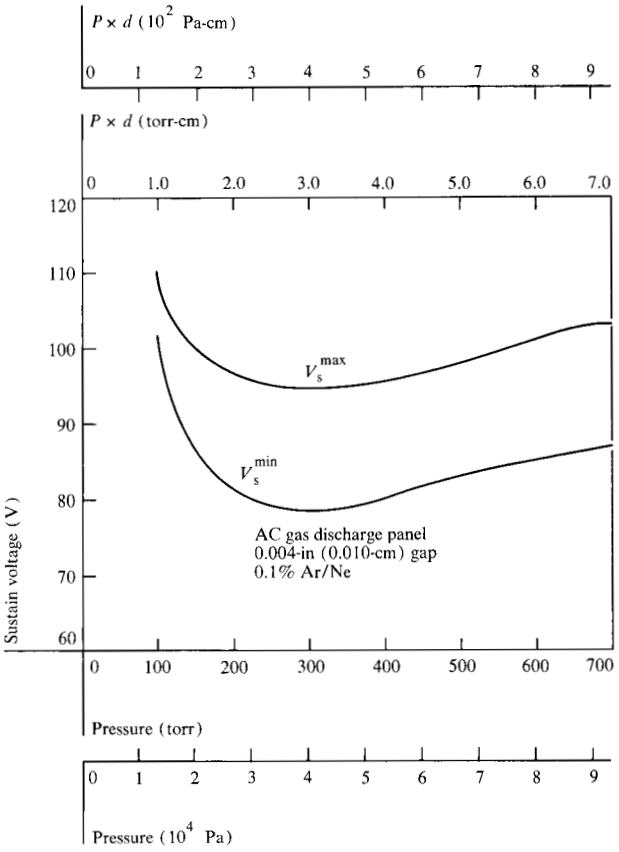

Figure 8 Maximum and minimum sustain voltages as a function of pressure at constant interplanar spacing and for constant *Pd* product values.

part of the process less susceptible to contamination. To do this, it was essential to eliminate frit application and reflow. Also, because of the interrelationships amongst seal glass, substrate, and dielectric in a conventional fabrication process, it was decided to separate the dielectric and seal regions. In conventional panel fabrication, the dielectric and seal both contribute to panel hermeticity since the dielectric is continuous right through the seal region to the outside of the panel, the seal being made to the dielectric rather than the electrodes. Furthermore, the dielectric serves somewhat as an electrode protection during processing. With the Cu-Al metallurgy, however, the latter was no longer called for. In addition, if successful, the panel materials compatibilities would be less troublesome since the structure would consist of an independent envelope and isolated active regions, the latter being alterable without perturbing the integrity of the former.

A key feature of a dielectric layer, in addition to its electrical characteristics, is its stress level, and great attention was devoted to developing an essentially zero-stress dielectric technology. The results of the successful

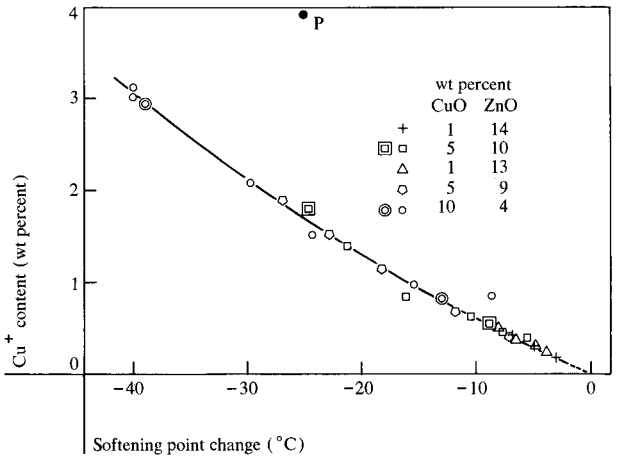

Figure 9 Softening points vs Cu^+ content of a family of solder glasses having fixed CuO-ZnO combined weight percent.

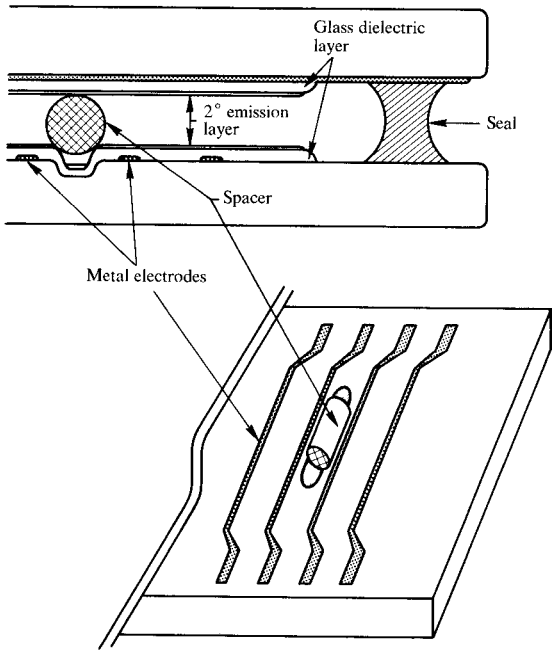

Figure 10 Schematic representation of a spacer technology.

attempts at evolving a suitable dielectric technology are discussed by Park and Weitzman [12].

Intertwined with all of the above is the development of a controlled seal technology. Having separated seal and dielectric, and having broken the softening point hierarchy, the seal constraints are somewhat alleviated. The main effort then was to evolve seal glass processes which were reproducible, free of precipitates, resistant to spontaneous crystallization, and which provided hermeticity values of the kind discussed. Takamori et al. [17] have found in a study of lead-copper-zinc seal glasses that the controlling factor in their temperature-viscosity behavior traces back to their Cu^+ content. Thus, while the softening point was found to be totally dependent on Cu^+ concentration, thermal coefficient of expansion was not. In Fig. 9, the effect of varying Cu^+ content on softening points for a family of glasses is shown. This family of glasses has a combined copper-zinc content of 15 weight percent, and when the copper is all present as Cu^{++}, the softening points and thermal coefficients of expansion of each of the glasses in this family are essentially the same. This "universal" softening point curve indicates that in all of these glasses a change of approximately 1% in Cu^+ content in any one of the glasses causes a change in softening point of about 14°C. Data such as these have provided us with the wherewithal to use a single seal glass over a range of temperatures by simply controlling the Cu^+ concentration of the glass. Details of seal glass studies are given elsewhere [17].

The final question addressed in relation to panel fabrication involved reduction of the number of processing steps to minimize susceptibility to contamination and to reduce the pieces of fabrication gear involved. For example, it appears feasible, ultimately, to conduct electrode deposition, dielectric deposition, and secondary-electron emission layer deposition sequentially in a single vacuum system, in a single pump-down.

Another sequence that lends itself to combination is that involving sealing, outgassing, discharge gas backfilling, and panel tip-off. Such a sequence would serve also to minimize exposure of the sensitive secondary-electron emission layer to attack by environmental agents such as H_2O, CO_2, and carbonaceous matter. An apparatus to accomplish this sequence is discussed by Reisman et al. [11]. Panel characteristics obtained using single-cycle processing are described by O'Hanlon et al. [6].

The spacer problem in gas panel operation has been alluded to in the discussion of plate deformation under a pressure differential. Ideally, one would like to employ a spacer technology which is simple and which is invisible in a lit panel. Figure 10 shows schematically the implementation of such a technology. It involves the formation of grooves between the metal lines on the face plate of the panel and insertion of 50-mil- (1.3-mm)-long spacer rods in these grooves. In its fullest implementation, the grooves are formed on the blank plates; masked electrode, dielectric, and secondary-electron emission layer depositions are conducted; spacers are dropped into the grooves; and the panel parts are sealed together. The key to the success of this spacer approach is that the grooves must lie parallel to the electrode array. Since the evaporated dielectric conforms to the groove contours, there is no problem of leveling off of the grooves, as would occur in a reflow process.

Figure 11 shows a test panel with four spacers present in its interior. The spacer locations are circled in black and, as can be seen, the spacers are almost invisible.

While much progress has been made since the invention of the ac panel in evolving a technology that produces reliable devices, more remains to be done. Chronologically, the current status is probably analogous to planar silicon technology. The transition to the equivalent of integrated circuit technology has still to be made, and the equivalency to large scale integration is not yet in sight. A major aspect of the next technological transition may focus more on questions relating to the packaging of driver and logic circuits than in improvement in the panel itself. For example, at present each electrode must be interconnected to the outside world via a hierarchy of package elements. Such package costs can exceed the cost of the electronic components significantly. Packaging the electronics directly on the panel could reduce such costs dramatically. Another focus, applicable primarily to lower character count applications, is the use of the panel in a scan mode where its intrinsic memory is not utilized, and basically the device is refreshed using electronic memory. This should result in improved yields and could lead to lower driver-package costs. Following this next stage, depending on innovation to a great extent, we might expect the focus to change to incorporating color and gray scale capabilities into ac panels, areas in which present panel technology is lacking.

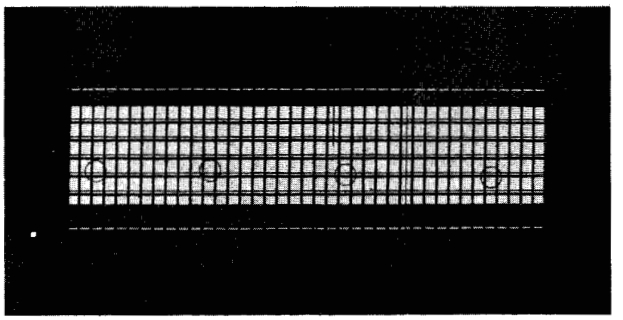

Figure 11 Photograph of a lit experimental panel using an invisible spacer technology.

References

1. D. L. Bitzer and H. G. Slottow, "The Plasma Display Panel—A Digitally Addressable Display with Inherent Memory," *AFIPS Conf. Proc.*, Fall Joint Computer Conference, San Francisco, **29,** 41 (1966).
2. For a historical description of the ac plasma panel, see H. G. Slottow, *IEEE Trans. Electron Devices* **ED-23,** 760 (1976).
3. M. J. Druyvesteyn and F. M. Penning, *Rev. Mod. Phys.* **12,** 87 (1940); see in particular the discussion on p. 122; F. M. Penning, *Phil. Mag.* **11,** 961 (1931); J. R. Acton and J. D. Swift, *Cold Cathode Discharge Tubes*, Academic Press, Inc., New York, 1963, pp. 222, 223.
4. P. H. Haberland, *J. Vac. Sci. Technol.* **10,** 796 (1973).
5. O. Sahni and C. Lanza, *J. Appl. Phys.* **47,** 1337 (1976).
6. John F. O'Hanlon, K. C. Park, A. Reisman, R. Havreluk, and J. G. Cahill, *IBM J. Res. Develop.* **22,** 613 (1978, this issue).
7. W. E. Ahearn and O. Sahni, *IBM J. Res. Develop.* **22,** 622 (1978, this issue).
8. E. S. Schlig and G. R. Stilwell, Jr., *IBM J. Res. Develop.* **22,** 634 (1978, this issue).
9. C. Lanza and O. Sahni, *IBM J. Res. Develop.* **22,** 641 (1978, this issue).
10. John F. O'Hanlon, *IBM J. Res. Develop.* **22,** 626 (1978, this issue).
11. A. Reisman, M. Berkenblit, and S. A. Chan, *IBM J. Res. Develop.* **22,** 596 (1978, this issue).
12. K. C. Park and E. J. Weitzman, *IBM J. Res. Develop.* **22,** 607 (1978, this issue).
13. V. Brusic, F. M. d'Heurle, R. D. MacInnes, E. I. Alessandrini, J. Angilello, J. J. Dempsey, and M. Sampogna, *IBM J. Res. Develop.* **22,** 647 (1978, this issue).
14. R. Hammer, *IBM J. Res. Develop.* **22,** 601 (1978, this issue).
15. A. Reisman and M. Berkenblit, unpublished results.
16. F. Paschen, *Wied. Ann.* **37,** 69 (1889); J. D. Cobine, *Gaseous Conductors*, Dover Publications, New York, 1958, p. 163.
17. T. Takamori, A. Reisman, and M. Berkenblit, *J. Amer. Ceram. Soc.* **59,** 312 (1976).

Received September 6, 1977; revised February 2, 1978

The authors are located at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598.