

Two-Dimensional Analysis of High-Voltage Power Transistors

Abstract: The internal behavior of a typical n - p - n^- - n^+ high-voltage power transistor is presented for several specific steady-state operating conditions obtained from a two-dimensional mathematical model. Internal self-heating and avalanche multiplication effects are taken into account. Poisson's equation, electron and hole continuity equations, and the heat flow equation are solved numerically in a two-dimensional region with the input parameters of device dimensions, doping profile, boundary conditions for external contacts, and various material constants for silicon. The collector n^- - n^+ interface is the region of high electrical and thermal stress that causes second breakdown failure at high-voltage and high-current operating conditions. The combined effects of various high-injection levels are illustrated.

Introduction

The second breakdown failure mode, which has been known for some time [1], continues to be the major cause of failure of bipolar transistors in high-power circuits. Nonuniformity of temperature and current density distributions within the device [2] and the avalanche injection from the collector n^- - n^+ interface [3] are believed to be the cause of second breakdown. In many switching applications of high-voltage n - p - n^- - n^+ power transistors, second breakdown failures have been observed in turn-off and turn-on transients where the device is subjected to high-voltage and high-current operating conditions for a part of the switching time. A clear understanding of the internal behavior of transistors is important for their proper circuit applications as well as for the development of new transistor designs for improved power handling capability. An analytical solution of transport equations governing the internal behavior of semiconductor devices cannot be obtained easily without making various assumptions and simplifying approximations. Recently, numerical methods [4–11] have been used to analyze the internal behavior of bipolar transistors. Previous analyses by the author [6, 9, 11] have taken into account internal self-heating effects by assuming that the charge carriers are in thermal equilibrium with the lattice, which has a nonuniform temperature distribution, and assuming also the generation of carriers due to avalanche multiplication.

The purpose of this paper is to present the internal behavior of a typical high-voltage power transistor at operating conditions obtained by an existing mathematical model [6, 9]. Poisson's equation, electron and hole continuity equations, and the heat flow equations are

solved numerically in two dimensions. Input parameters required are device dimensions, doping profile, and boundary conditions for external contacts; various material constants for silicon are also specified. The results are presented for a power transistor structure with a current capability of about 5 A and a breakdown voltage (BV_{CB0}) of about 900 V. Computed electric field, current density, and temperature distributions within the device are presented for various time-independent operating conditions, providing an insight into the electrical and thermal stresses causing transistor failure. Predictions from this mathematical model compare favorably with failure analysis observations of stressed transistors, indicating that the damage in n - p - n^- - n^+ high-voltage power transistors does begin at the n^- - n^+ interface. The combined influence of various high injection level effects [12–15] is predicted.

Theory

The set of equations used to obtain the steady-state behavior of high-voltage power transistors for specified operating conditions is listed in Table 1. Internal self-heating is taken into account by solving the heat flow equation to obtain nonuniform lattice temperature distribution, and by assuming that the charge carriers are in thermal equilibrium with the lattice. Avalanche multiplication is represented by the carrier generation resulting from the electric field and current density which have different ionization coefficients for electrons and holes.

Equation (1), in Table 1, is Poisson's equation relating the electrostatic potential (ψ) to the mobile hole (p) and mobile electron (n) and ionized impurity density

Table 1 Equations.

$$\nabla^2 \psi = -\frac{q}{\epsilon} [p - n + N] \quad (1)$$

$$\nabla \cdot \mathbf{J}_p = q(G - R) \quad (2)$$

$$\nabla \cdot \mathbf{J}_n = -q(G - R) \quad (3)$$

$$\nabla \cdot K \nabla T + Q = 0 \quad (4)$$

with auxiliary equations:

$$\mathbf{J}_p = -q\mu_p p \nabla \psi - qD_p \nabla p \quad (5)$$

$$\mathbf{J}_n = -q\mu_n n \nabla \psi + qD_n \nabla n \quad (6)$$

$$D_p/\mu_p = D_n/\mu_n = kT/q \quad (7)$$

$$G = [\alpha_n(E) |J_n| + \alpha_p(E) |J_p|]/q \quad (8)$$

$$R = \frac{pn - n_i^2}{\tau_{n0}(p + n_i) + \tau_{p0}(n + n_i)} \quad (9)$$

$$Q = \mathbf{J}_T \cdot \mathbf{E} \quad (10)$$

$$\mathbf{J}_T = \mathbf{J}_p + \mathbf{J}_n \quad (11)$$

$$\mathbf{E} = -\nabla \psi \quad (12)$$

$$n = n_i \exp [q(\psi - \phi_n)/kT] \quad (13)$$

$$p = n_i \exp [q(\phi_p - \psi)/kT] \quad (14)$$

$$n_i(T) = 3.88 \times 10^{16} T^{1.5} \exp (-7000/T) \quad (15)$$

$$\alpha_p(E) = 2.25 \times 10^7 \exp (-3.2 \times 10^6/|E|) \quad (16)$$

$$\alpha_n(E) = 3.80 \times 10^6 \exp (-1.75 \times 10^6/|E|) \quad (17)$$

$$\left(\frac{480}{\mu_p}\right)^2 = 1 + \frac{N}{(N/81) + 4 \times 10^{16}} + \frac{(E/6.1 \times 10^3)^2}{(E/6.1 \times 10^3) + 1.6} + (E/2.5 \times 10^4)^2 \quad (18)$$

$$\left(\frac{1400}{\mu_n}\right)^2 = 1 + \frac{N}{(N/350) + 3 \times 10^{16}} + \frac{(E/3.5 \times 10^3)^2}{(E/3.5 \times 10^3) + 8.8} + (E/7.4 \times 10^3)^2 \quad (19)$$

$$K = 3110/T^{4/3} \quad (20)$$

($N = N_D^+ - N_A^-$). The impurity atom distribution N is obtained from a two-dimensional solution of the diffusion equations [16]. Table 2 gives the impurity atom density at the emitter, base, and collector contacts and in the epitaxial collector region of the transistor design used in the present analysis.

Equations (2) and (3) are the hole and electron continuity equations under steady-state conditions. Hole current density J_p and electron current density J_n are given by Eqs. (5) and (6) respectively. Equation (7) gives the Einstein relations between hole and electron mobilities (μ_p , μ_n) and diffusion coefficients (D_p , D_n). The dependence of the carrier mobilities on the electric field and the impurity atom density is taken into account by utilizing the empirical expressions (18) and (19) from Reference [17]. It has been pointed out [18] that the validity of the empirical relations to describe the field dependence of the mobility in the vicinity of a forward-biased emitter-base junction may be questionable. For the present analysis, therefore, the carrier mobilities are assumed to be independent of the electric field in the forward-biased emitter-base junction region. Term G in Eqs. (2) and (3) is the generation of carriers due to the

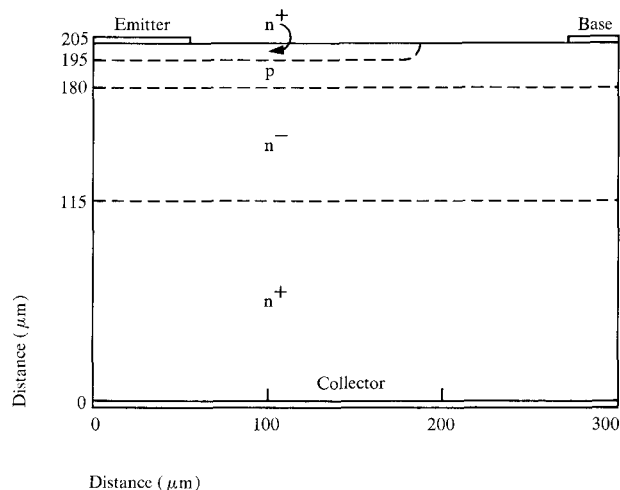


Figure 1 Two-dimensional n-p-n-n⁺ transistor structure.

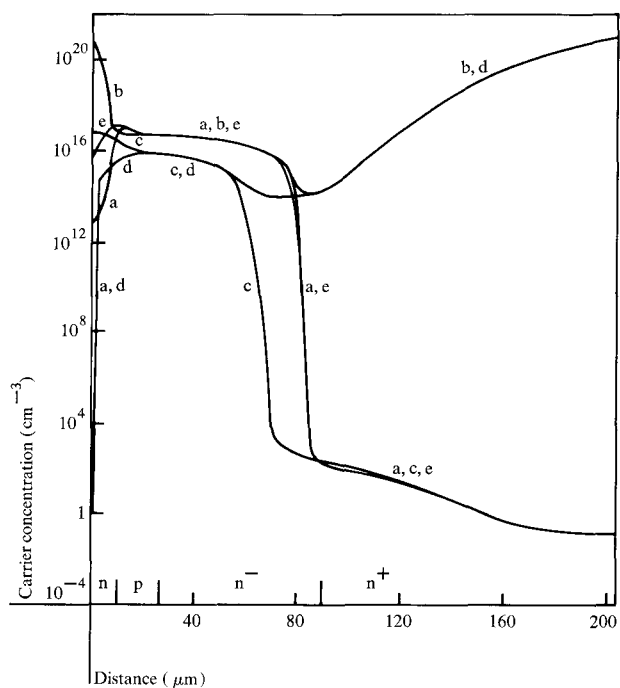


Figure 2 Mobile hole and electron concentration distributions along the line $x = 0$ in Fig. 1 (curves a and b respectively), along the line $x = 300 \mu\text{m}$ (curves c and d respectively) and hole concentration distribution along the line $x = 185 \mu\text{m}$ (curve e) for $V_{CB} = 4.5 \text{ V}$ and $V_{BE} = 0.9 \text{ V}$.

Table 2 Device design parameters.

n^+ collector surface impurity concentration	$1.0 \times 10^{21} \text{ cm}^{-3}$
n^- collector bulk impurity concentration	$1.1 \times 10^{14} \text{ cm}^{-3}$
Base surface impurity concentration	$6.0 \times 10^{16} \text{ cm}^{-3}$
Emitter surface impurity concentration	$1.0 \times 10^{21} \text{ cm}^{-3}$
Lifetime parameter τ_{p0}	$3.0 \times 10^{-6} \text{ sec}$
Lifetime parameter τ_{n0}	$1.0 \times 10^{-5} \text{ sec}$
Emitter area	0.065 cm^2

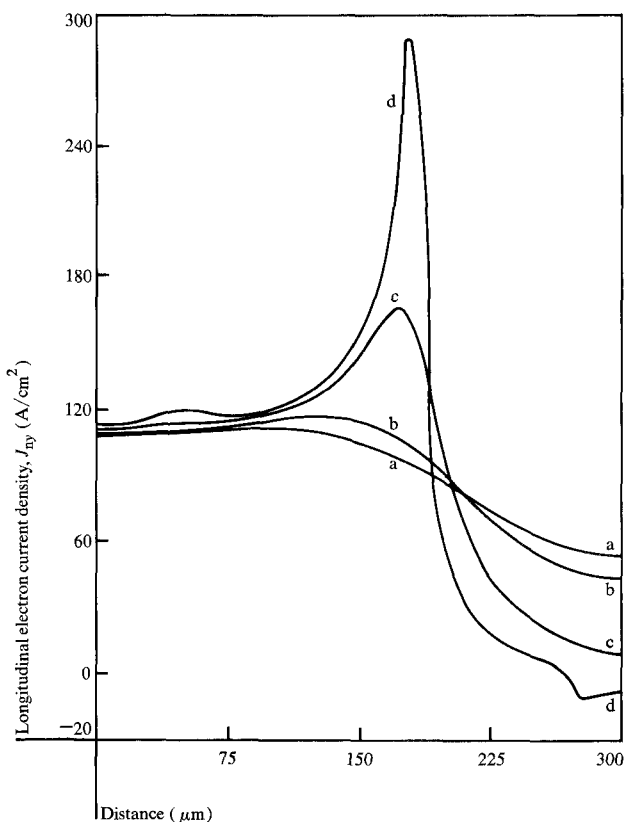


Figure 3 Longitudinal electron current density distribution along the collector contact (curve a), along the n^-n^+ interface (curve b), along the base-collector junction (curve c), and along the emitter-base junction (curve d) for $V_{CB} = 4.5$ V and $V_{BE} = 0.9$ V. The total collector current is 2.8 A/cm.

electric field and current density as given by Eq. (8). Hole and electron ionization coefficients used in the present analysis are given by Eqs. (16) and (17) respectively [17]. The generation-recombination term R is assumed to follow the Shockley-Read-Hall steady-state recombination law [19] corresponding to uniformly distributed recombination centers with a single energy level in the center of the band gap [Eq. (9)]. The parameters τ_{n0} and τ_{p0} are electron and hole lifetimes and n_i is the intrinsic carrier concentration. The temperature dependence of n_i for silicon used in this analysis is given by Eq. (15), of [20].

Equation (4) is the heat flow equation that determines the lattice temperature T under steady-state conditions. The temperature dependence of the thermal conductivity K for silicon [21] is approximated by Eq. (20). Term Q in Eq. (4) is the heat generated per unit volume and is represented in Eq. (10) by the dot product of total current density J_T [Eq. (11)] and the electric field E [Eq. (12)], neglecting the heat generation due to

carrier recombination. In the vicinity of the forward-biased emitter-base junction, Q becomes negative and is assumed to be zero.

Equations (13) and (14) are Boltzmann approximations of Fermi statistics between the potential and carrier densities. Quantities ϕ_p and ϕ_n are hole and electron quasi-Fermi potentials.

The effect of heavy doping on the transport equations [22, 23] has not been included in the present analysis. It has been pointed out [24] that this effect may not be important for large power transistor structures.

Equations (1)–(4) are normalized into dimensionless form [6] and are solved for variables ψ , p , n and T by the finite difference for a two-dimensional region shown in Fig. 1. The set of equations (1)–(4) is solved in a cyclic manner, individually, for one unknown with the known values of the other three variables from previous iterations. A nonuniform rectangular grid covering the region of analysis shown in Fig. 1 is chosen, and the difference approximations associated with each of the equations (1)–(4) are written for every node with its four nodal neighbors. The resulting set of algebraic equations is of the form

$$A\theta = b, \quad (21)$$

where A is a five-diagonal matrix, θ is one of the four unknowns, and b is a column vector [6]. Equation (21) is solved by an iterative method of Stone [25].

• Boundary conditions

The boundary conditions assumed for the variables ψ , p , n and T for a typical high-voltage power transistor structure as shown in Fig. 1 are as follows:

$$\frac{\partial \psi}{\partial x} = \frac{\partial p}{\partial x} = \frac{\partial n}{\partial x} = \frac{\partial T}{\partial x} = 0$$

along the lines $x = 0$ and $x = 300$ μm (axes of symmetry),

$$\partial T / \partial y = 0$$

along the line $y = 205$ μm ,

$$\frac{\partial \psi}{\partial y} = \frac{\partial p}{\partial y} = \frac{\partial n}{\partial y} = 0$$

along the line $y = 205$ μm between the emitter and base contact metallization, and

$$T = \text{constant}$$

along the line $y = 0$.

The emitter, base, and collector contacts are assumed to be ideal ohmic contacts. The semiconductor is in thermodynamic equilibrium at these contacts and charge

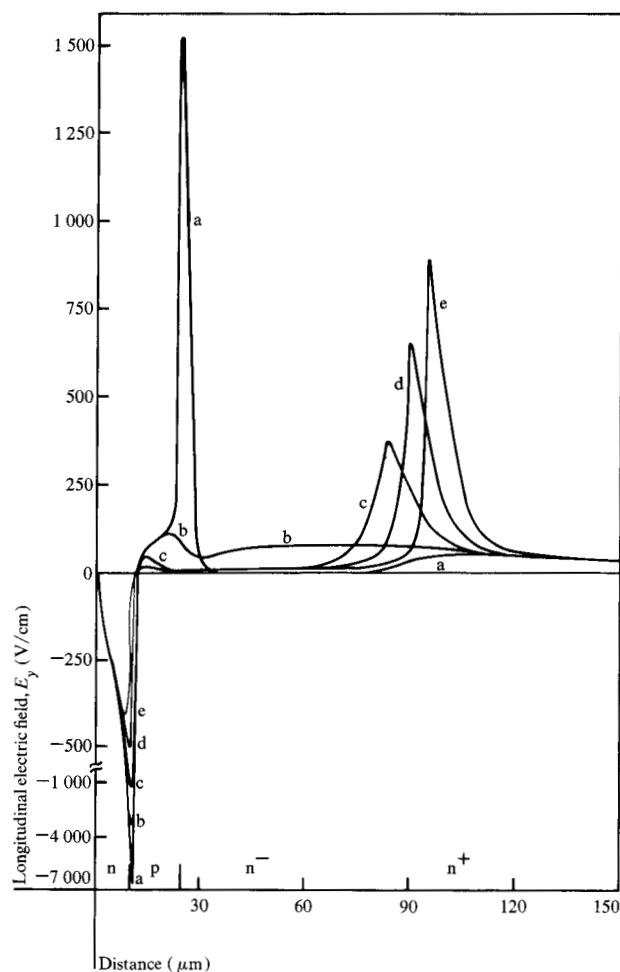


Figure 4 Longitudinal electric field distribution along the line $x = 0$ in Fig. 1 for $V_{CB} = 0$ and $V_{BE} = 0.5$ V (curve a), 0.6 V (curve b), 0.7 V (curve c), 0.8 V (curve d), and 0.9 V (curve e).

neutrality conditions are valid. Under these assumptions, the normalized carrier concentrations at the emitter and collector contacts are specified as

$$n = N/2 + [(N/2)^2 + n_i^2]^{1/2}, \quad (22)$$

$$p = n_i^2/n, \quad (23)$$

where N is the net donor density. The carrier concentrations at the base contact are given by

$$p = -(N/2) + [(N/2)^2 + n_i^2]^{1/2}, \quad (24)$$

$$n = n_i^2/p, \quad (25)$$

where the net donor density N is negative. From Eqs. (13), (14), (22), and (24), the electrostatic potentials at the emitter, base, and collector contacts under zero bias conditions are obtained as

$$\psi = \ln(n_i/p) = (\ln(n/n_i)), \quad (26)$$

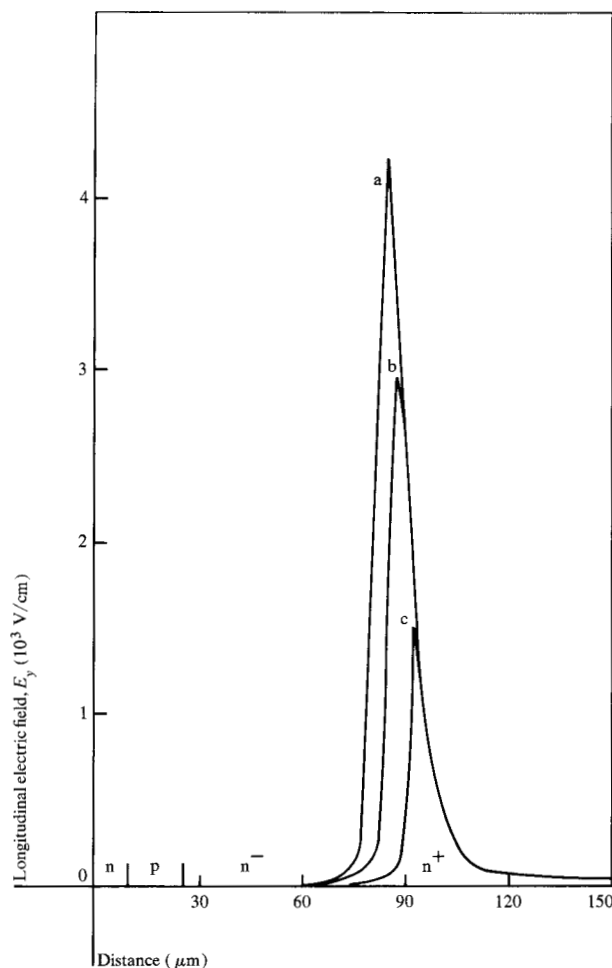


Figure 5 Longitudinal electric field distribution along the line $x = 0$ in Fig. 1 for $V_{BE} = 0.9$ V and $V_{CB} = 4.5$ V (curve a), 2.5 V (curve b), and 0.5 V (curve c).

where the value of the Fermi potential level is arbitrarily assumed to be zero. In order to specify certain operating conditions, the applied voltage values at the emitter, base, and collector contacts are added to their zero bias potential values.

Results and discussion

The geometric structure of the analyzed bipolar n-p-n⁻-n⁺ silicon high-voltage power transistor is shown in Fig. 1. Some of the design parameters assumed for this structure are listed in Table 2. The breakdown voltage BV_{CB0} for this structure is about 900 V. BV_{CE0} of this transistor is about 425–450 V, and the current capability is about 5 A. Lifetime parameters τ_{n0} and τ_{p0} are chosen in such a manner that the predicted $I_C - V_{BE}$ characteristic correlates well with experimental observations. Figures 2–7 depict the internal behavior of the transistor

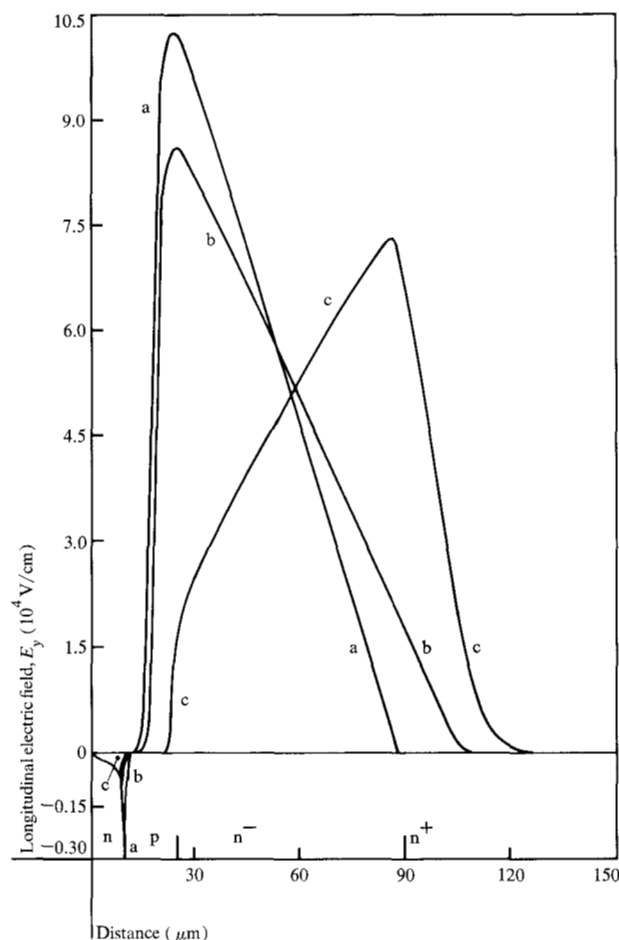


Figure 6 Longitudinal electric field distribution along the line $x = 0$ in Fig. 1 for $V_{CB} = 400$ V and $V_{BE} = 0.6$ V (curve a), 0.7 V (curve b), and 0.8 V (curve c).

for various operating conditions, after assuming a constant temperature of 300 K everywhere within the device. Figure 2 shows the distribution of electron and hole concentrations from the emitter contact to the collector contact along the lines $x = 0$ and $x = 300$ μm (Fig. 1), and the distribution of hole concentration along the emitter edge ($x = 185$ μm in Fig. 1) for $V_{CB} = 4.5$ V and $V_{BE} = 0.9$ V. At this operating condition, the electrical base region extends into the n^- collector region right up to the n^- - n^+ interface under the emitter finger as illustrated by the stored hole charge in the n^- region in Fig. 2 (curves a and e). The extent of base widening in the inactive base region under the base contact is illustrated by curve c in Fig. 2.

Figure 3 shows the distribution of the longitudinal electron current density along the collector contact, n^- - n^+ interface, base-collector junction and emitter-base junction at $V_{CB} = 4.5$ V and $V_{BE} = 0.9$ V. At the emitter-base junction, the crowding ratio of the longitudinal elec-

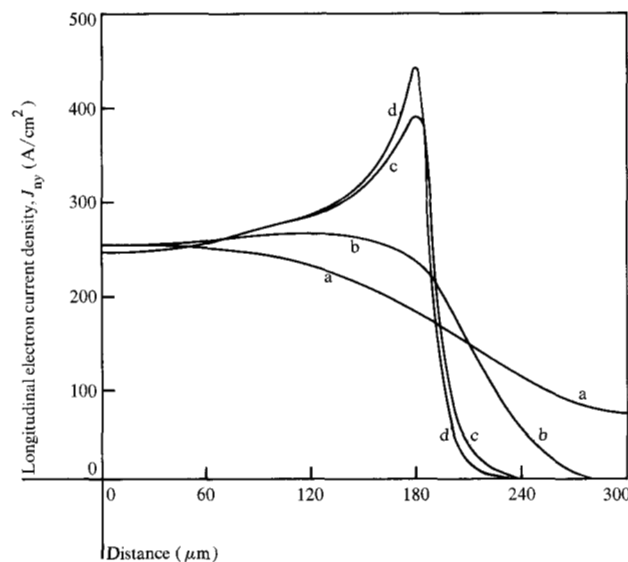


Figure 7 Longitudinal electron current density distribution along the collector contact (curve a), along the n^- - n^+ interface (curve b), along the base-collector junction (curve c), and along the emitter-base junction (curve d) for $V_{CB} = 400$ V and $V_{BE} = 0.8$ V. The total collector current is 5.57 A/cm.

tron current densities at the emitter edge and at the emitter center is about 2.5 (curve d in Fig. 3). Curves c, b, and a show the reduction in this crowding ratio due to current spreading effects. Curve d in Fig. 2 shows that there is an appreciable amount of injected electron charge stored in the base region under the base contact. It is seen from curve d of Fig. 3 that the longitudinal electron current density under the base contact is in the negative y direction, implying that some of the injected electrons from the emitter are being collected at the base contact. This causes an increase in the base current and the subsequent degradation of current gain with increasing total current [7].

Figure 4 depicts the electric field distribution from the emitter contact to the collector region along the $x = 0$ line as shown in Fig. 1. At a constant collector-to-base voltage ($V_{CB} = 0$) and different base-to-emitter voltages (increasing values of V_{BE} corresponding to increasing current levels), the shift in the electric field peak from the base-collector junction to the n^- - n^+ junction illustrates the base widening in the n^- collector region with increasing current level. Figure 5 shows the electric field distribution also along the $x = 0$ line, as shown in Fig. 1, for a constant current level and different values of V_{CB} . The electric field distribution ($V_{CB} = 400$ V) at different current levels is shown in Fig. 6. Steady-state solution of Figs. 4–6 provides some insight into the electric field distribution within inductively loaded transistors in high-power circuits during turn-off and turn-on transient con-

ditions. For "on" conditions where the V_{CB} is small (a few volts) and the current through the device is high (4–5 A), the electric field peaks at the n^-n^+ interface, as seen from Fig. 4. As the device is subjected to high-voltage and high-current operating conditions during turn-off transient, the electric field peak at the n^-n^+ interface increases sharply (Fig. 5 and curve c of Fig. 6), and as the current level of the device decreases, the electric field distribution will change to that of curve a as shown in Fig. 6. The reverse order corresponds to the electric field distribution within the transistor during turn-on transient where the operation of the device changes from high-voltage low-current to low-voltage high-current operating conditions. However, there will be a larger and sharper peak electric field at the n^-n^+ interface, and for a longer duration during turn-off transient, because the electric field peaks at the n^-n^+ interface before the transient and is subjected to a higher V_{CB} during turn-off than during turn-on transient.

Figure 7 depicts the longitudinal electron current density distributions along the collector contact, n^-n^+ interface, base-collector junction, and emitter-base junction at operating conditions of $V_{CB} = 400$ V and $V_{BE} = 0.8$ V. At the emitter-base junction, the crowding ratio of the current densities at the emitter edge and emitter center is about 1.8 (curve d in Fig. 7). It is seen from Figs. 3 and 7 that the current density along $x = 0$ (see Fig. 1) remains approximately constant. The base widening in the n^- collector region and the associated electric field (peaking in the collector region, rather than at the base-collector junction) begins with the increasing current level operation of the transistor [26]. The values of current density at the base-collector junction under the center of the emitter for curves a, b, c, d, and e of Fig. 4 are 0.05, 1.93, 8.95, 30.6 and 91.8 A/cm² respectively; for curves a, b, and c of Fig. 6, the values are 1.85, 58.1, and 248 A/cm² respectively.

The electric field and current density distributions within the transistor structure suggest that at high-current and high-voltage levels of operation, the n^-n^+ interface is the region of high electrical stress; because of internal self-heating, the temperature at the n^-n^+ interface may be very high. Figure 8 shows the temperature distribution along the n^-n^+ interface and the emitter-base junction for steady-state operation of the device at $V_{CB} = 400$ V and $V_{BE} = 0.6$ V. They are obtained by the nonisothermal analysis, and assume the temperature along the line $y = 0$ (see Fig. 1) to be 300 K. Due to higher temperature, the electron current density value at the base-collector junction under the center of the emitter, as predicted by the nonisothermal analysis, is 3.70 A/cm² compared to 1.93 A/cm² of the isothermal analysis. Even at low current levels, there are significant temperature gradients within the device.

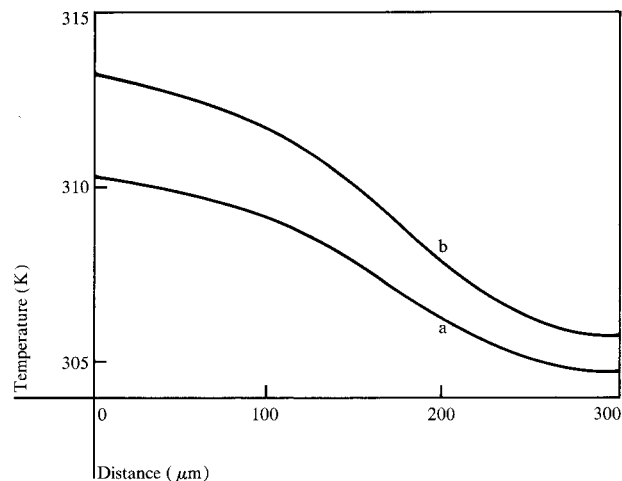


Figure 8 Temperature distribution along the n^-n^+ interface (curve a), and along the emitter-base junction (curve b) for $V_{CB} = 400$ V and $V_{BE} = 0.6$ V. The temperature along the line $y = 0$ in Fig. 1 is assumed to be 300 K.

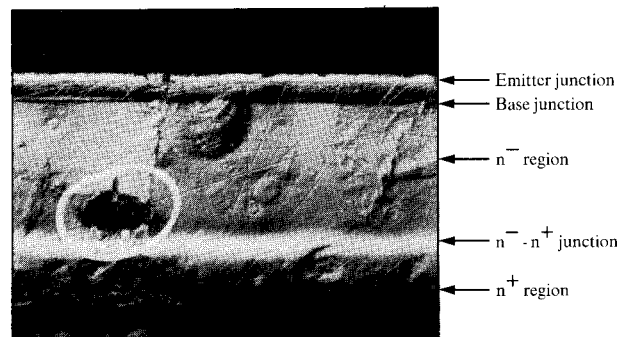


Figure 9 Cross-sectional view of power transistor chip showing internal crystal damage.

A time-dependent solution of transport equations provides quantitative estimates of the temperature distribution within the transistor structure during switching applications. The steady-state solution indicates the possibility of very high temperature values at the n^-n^+ interface during switching because the time constant for thermal conduction is much larger when compared to the electrical carrier transport. Internal crystal damage has been observed in a power transistor with design parameters of Table 2, after on/off switching in a circuit with an inductive load. Infrared scanning and cross-sectioning and visual inspection of the chip revealed the crystal damage at the n^-n^+ interface under the center of the emitter [27]. The transistor, however, showed no degradation in electrical parameters after about 1000 hours of operation. Figure 9 is a cross-sectional view of the transistor chip showing the defect location. The diameter of the defect is about 38 μ m (1.5 mil). It is believed [27] that the crystal damage is due to local heat-

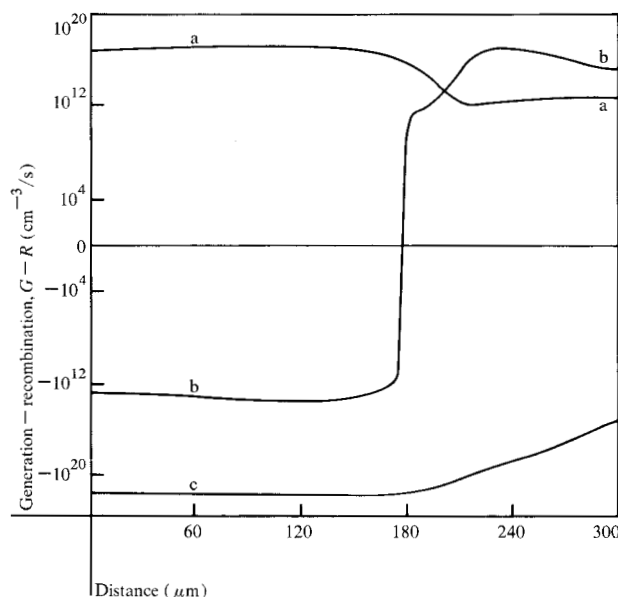


Figure 10 Distribution of carrier generation minus recombination along the n^-n^+ interface (curve a), along the base-collector junction (curve b), and along the emitter-base junction (curve c) for $V_{CB} = 400$ V and $V_{BE} = 0.8$ V.

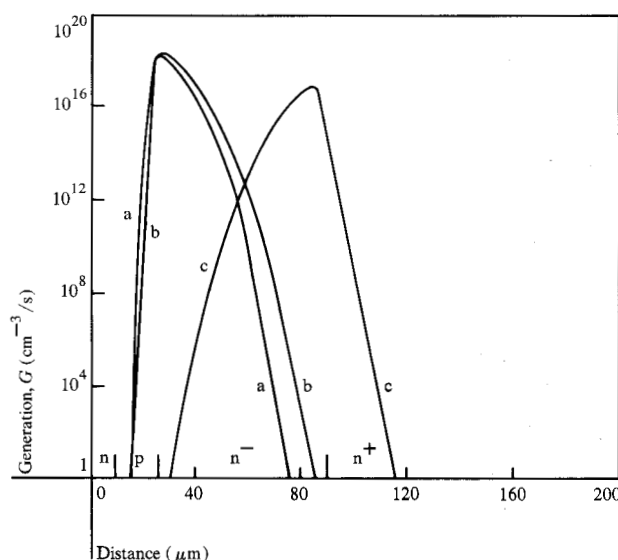


Figure 11 Distribution of carrier generation due to avalanche multiplication along the line $x = 0$ in Fig. 1 for $V_{CB} = 400$ V and $V_{BE} = 0.6$ V (curve a), 0.7 V (curve b), and 0.8 V (curve c).

ing and may be an early stage of the failure. Operating conditions that create high electrical and thermal stresses within the device could eventually cause its destruction.

Figures 10–12 depict the generation and recombination of carriers within the transistor structure, and avalanche-generated current density at different current lev-

els as obtained by isothermal analysis. Figure 10 shows the distribution of carrier generation minus recombination along the n^-n^+ interface (curve a), base-collector junction (curve b), and emitter-base junction (curve c) at $V_{CB} = 400$ V and $V_{BE} = 0.8$ V. Along the n^-n^+ interface, generation of carriers due to avalanche multiplication is dominant under the emitter finger, while under the base contact, the generation of carriers due to the Shockley-Read-Hall generation-recombination term is dominant. Along the base-collector junction ($y = 180$ μm in Fig. 1), the electric field is small under the emitter finger ($x = 0$ to $x = 185$ μm), and there is a net recombination of carriers. Under the base contact ($x = 275$ to $x = 300$ μm), the electric field is high at the base-collector junction ($y = 180$ μm), and there is a net generation of carriers due to avalanche multiplication. Along the emitter-base junction ($y = 195$ μm), there is also a net recombination of carriers. Figure 11 shows the generation of carriers due to avalanche multiplication along the line $x = 0$ (Fig. 1) for $V_{CB} = 400$ V, and $V_{BE} = 0.6$ V, 0.7 V, and 0.8 V (representing different current levels of operation). As the current level increases, electric field distribution changes (Fig. 6): Consequently, the distribution of the generation of carriers due to avalanche multiplication changes, peaking at the n^-n^+ interface at high-current levels. Figure 12 shows the distribution of the avalanche-generated current density [$J_g(x) = \int qG(x,y)dy$] for $V_{CB} = 400$ V and $V_{BE} = 0.6$ V, 0.7 V, and 0.8 V. Since the generation of carriers depends on the electric field and current density [Eq. (8)], increases in current level account for increases in J_g from $V_{BE} = 0.6$ V to 0.7 V, while a reduction in peak electric field (Fig. 6) causes a reduction in J_g from $V_{BE} = 0.7$ V to 0.8 V. Results for even higher reverse-bias base-collector voltages are needed to obtain total base current in the positive y direction (Fig. 1) due to avalanche generation of carriers and current crowding in the center of the emitter finger [28].

The computation time required to solve Eqs. (1)–(4) (Table 1) depends on the number of nodes in the grid and the operating conditions [6], and becomes excessively large at high-current high-voltage operating conditions. A multigrid method [29, 30] of solution of Eqs. (1)–(4) is under consideration, where the set of equations is solved on a two-dimensional nonuniform grid with constant interactions with a hierarchy of coarse grids. The multigrid method of solution has been reported to be very efficient and takes advantage of the relation between various discrete representations of the same continuous problem.

Summary

A two-dimensional mathematical model, which includes avalanche multiplication and internal self-heating effects,

has been utilized to analyze the internal behavior of a high-voltage power transistor at various steady-state operating conditions. The magnitude and location of electrical and thermal stresses within the device which cause transistor failure have been presented.

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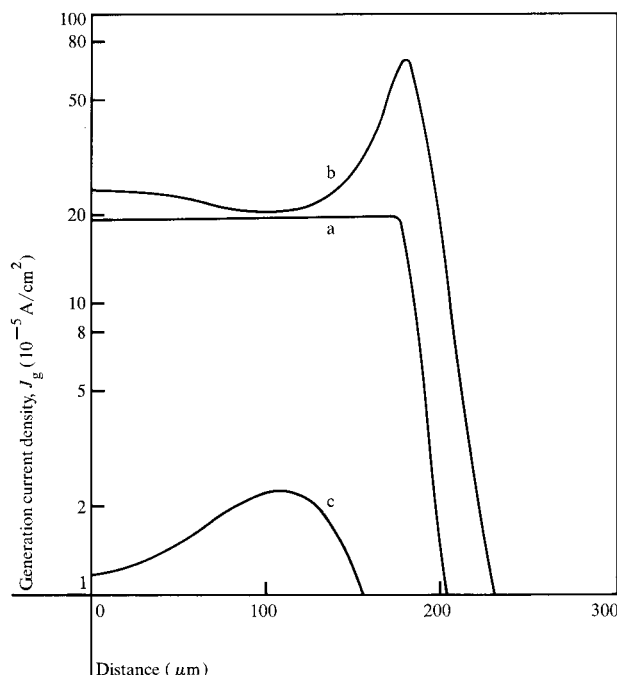


Figure 12 Avalanche-generated current density distribution along the x -axis in Fig. 1 ($J_g(x) = \int qG(x,y) dy$) for $V_{CB} = 400$ V and $V_{BE} = 0.6$ V (curve a), 0.7 V (curve b), and 0.8 V (curve c). The total avalanche generated current for curves a, b, and c is 3.73×10^{-6} A/cm, 5.94×10^{-6} A/cm, and 3.05×10^{-7} A/cm respectively.

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