

LSI Yield Modeling and Process Monitoring

Abstract: This paper describes an analytical technique for quantifying and modeling the frequency of occurrence of integrated circuit failures. The method is based on the analysis of random and clustered defects on wafers with defect monitors. Results from pilot line data of photolithographic defects, insulator short circuits, and leaky pn junctions are presented to support the practicality of the approach. It is shown that, although part of the yield losses are due to the clustering of defects, most product loss is from random failures. The yield model shows good agreement with actual product yields.

Introduction

Relatively little has been published about the actual causes of yield losses in large scale integrated circuits. Yet the successful production of LSI semiconductor products depends on the elimination of failures caused by simple open circuits in conductors, short circuits between conductors, and missing or misaligned contact holes in integrated circuits.

This paper describes a statistical method for quantifying the components of the product yield in a semiconductor process. Estimates are made for the yields associated with open and short circuits in various conductive layers, short circuits in insulator layers, and the breakdown of junctions. The estimates result from statistical manipulation of data obtained using defect monitors that are sensitive only to a particular type of defect. Therefore, the data can be used to estimate the defect densities causing the various types of open and short circuits. The defect densities, in turn, can then be used to calculate the corresponding product yields.

The yield for each yield detractor was calculated using known techniques [1-8]. In most of these cases, however, the yield models were applied to some total defect density, which tended to mask the major yield detractors and obscure the sources of yield losses. Measuring and modeling each type of defect individually, as described in this paper, allows the evaluation of all yield detractors. Major yield problem areas are thus exposed, and solutions to these problem areas can be sought. To study the statistics of failure mechanisms, the special defect monitors were used to detect short circuits and open circuits in conductors and pinholes in the dielectrics between the conductive layers. This detection was done by measuring the conductivity of the monitors with an automatic tester. Back-biased diffusions were used to study the pn junction leakage in diffused conductors. Alignment

detectors, such as those described by Thomas and Presson [9], were also used to study losses due to misalignment. But because these losses were negligible in the study presented here, they are not addressed further.

In this paper we first examine the theoretical basis for the analysis. Next we consider the critical areas in which a defect must be centered in order to cause a failure. The experimental procedure is then described, followed by a discussion of results. Finally, a less tedious method is described for obtaining quick estimates of yield.

Theoretical basis

It was recognized in 1964 by Murphy [1] that integrated circuit yields did not follow simple Poisson statistics. His approach using mixed Poisson statistics has been extended by Seeds [2], Ansley [3], Moore [4], Warner [5], and Stapper [6]. Yanagawa [7] and Gupta, et al. [8] believed that the non-Poisson behavior of LSI failures was due to a radial variation of defect densities, with the higher defect densities causing more failures toward the outer area of the wafers. The Poisson statistics were assumed valid only for local regions on the wafer. It is shown here that there is merit in both methods of yield modeling but that the actual conditions appear to be far more complex in practice than anticipated in any of the theories. However, the data can be handled with a simple extension to existing theory.

In a previous study [6] it was shown that the number of failing monitors x per wafer could be modeled by the mixed or compound Poisson distribution

$$\text{Prob}(X = x) = \int_0^\infty \frac{e^{-\lambda} \lambda^x}{x!} f(\lambda) d\lambda. \quad (1)$$

In that study Eq. (1) was used for the entire wafer. In our analysis, (1) is used independently for the inner and

outer zones of the wafer. Therefore, the distribution of λ represents a variation in the expected number of failures per zone, rather than in the expected number of failures per wafer, as in [6].

Distribution (1) has the useful property that

$$\bar{x} = \bar{\lambda}, \quad (2)$$

$$\text{var}(x) = \bar{\lambda} + \text{var}(\lambda). \quad (3)$$

The derivations of these equations are presented in Appendix A.

Our results show that the mean and variance for x in the data are directly related to the mean and variance of the unknown distribution $f(\lambda)$. Distribution (1) turns into a simple Poisson distribution when $\text{var}(\lambda) = 0$ or $\bar{x} = \text{var}(x)$. Therefore, the first test on our data is to determine whether the mean number of failures is less than or equal to the variance of x . When $\text{var}(x) \leq \bar{x}$, Poisson statistics are assumed. But in most cases, $\text{var}(x) > \bar{x}$, indicating the need to use the mixed Poisson statistics of Eq. (1).

The next step is to scale the yield of monitors per wafer to a yield of product chips per wafer. We did this by making the assumption that there is a defect density responsible for each type of failure. According to this approach, yield Y_m for the monitors is given by Murphy's yield formula [1]:

$$Y_m = \int_0^\infty \exp(-A_m D) f(D) dD, \quad (4)$$

where A_m is the critical area of the monitor and D the defect density producing Y_m . (We use the term "critical area" rather than "susceptible area" as used by Murphy [1], because we feel that the latter has the connotation of attracting defects.) Similarly, the product would have a yield

$$Y_p = \int_0^\infty \exp(-A_p D) f(D) dD, \quad (5)$$

where A_p is the critical area in the product for the defect type being monitored. The defect density distribution $f(D)$ is the same for product and monitors, but each type of defect has its own distribution.

The sample size available for the experiment described in this paper was too small to determine the precise form of the various defect density distributions. We did, however, have access to data obtained from a larger sample, produced with the same processes. Those results were described in the previous paper [6] already mentioned. The defect density distributions in that case could be modeled by gamma distributions. That paper also showed that the yield for an integrated circuit can be expressed as

$$Y = [1 + A \text{var}(D) / D]^{-\bar{D}^2 / \text{var}(D)}, \quad (6)$$

where $\bar{D}$ is the mean defect density. The derivation of this equation is shown in Appendix B. The ratio

$$\sigma / \mu = \frac{[\text{var}(D)]^{1/2}}{\bar{D}} \quad (7)$$

is the coefficient of variation for the defect density distribution. It is referred to as the sigma-to-mu ratio in this paper. A high σ / μ value implies significant variance in the defect densities among wafers, often indicating that the process is under poor control. A value of $\sigma / \mu = 0$ implies a pure Poisson process, something rarely experienced in practice.

Now we have to relate the number of failing monitors to the defect density. In practice, the monitor yield tends to be high. Our monitors produced about 95 percent yield for each type of defect. In this case, Eq. (6) for the monitor yield can be approximated by

$$Y_m \approx 1 - A_m \bar{D}. \quad (8)$$

But this yield is also given by

$$Y_m = 1 - \bar{x} / N, \quad (9)$$

where $\bar{x}$ is the average number of failing monitors per zone and N the total number of monitors per zone. Combining (8) and (9) with (2) and (3) results in

$$\bar{D} = \bar{x} / N A_m, \quad (10)$$

$$\text{var}(D) = [\text{var}(x) - \bar{x}] N^2 A_m^2. \quad (11)$$

These are approximate relationships. More exact procedures require iterative computer calculations. Suitable programs exist for this, but their accuracy is not required for interpretation of the data presented here.

Critical areas

In Eqs. (4), (5), (6), (8), (10), and (11), A_p , A_m , and A are the critical areas. The center of a defect must be located in these areas to cause a failure. In the case of dielectric pinholes, this is simply the area of the dielectric between the conductors. Area A_p is the sum of all these areas on the product chip. Similarly, A_m is the sum of the same areas on the monitor. For junction leakage the critical area was similarly defined as the sum of the diffused junction areas.

A more difficult problem exists with certain photolithographic patterns. The critical area calculations made for this paper used methods developed by Dennard and Chang [10], with subsequent changes by the author. Earlier work on the sensitivity of photolithographic patterns to defects was mentioned by Lawson [11].

It is known that open circuits occur far more frequently on narrower conductive lines than on wide lines. Similarly, more short circuits tend to occur between closely spaced conductors than between those with wider spac-

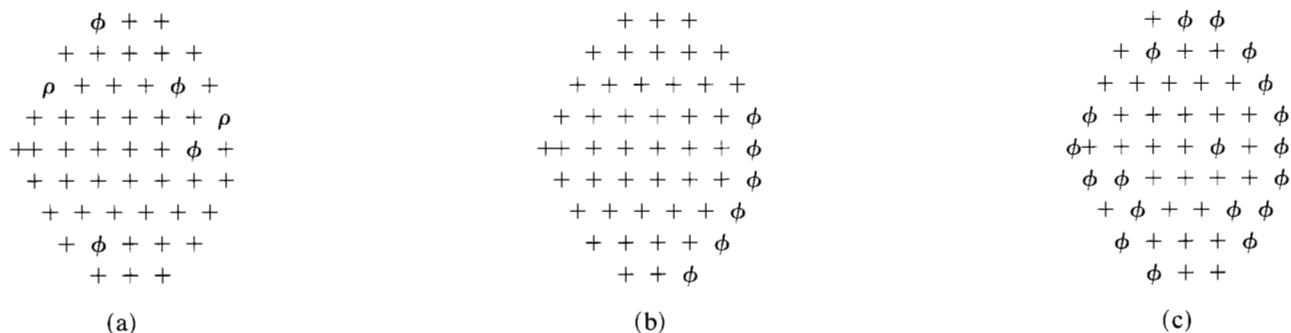


Figure 1 Wafer maps of the test pattern. Failures are indicated by ϕ , repeaters by ρ , and sites passing the test by $+$. At (a) a random defect pattern is shown in a diffusion open circuit monitor. The cluster pattern at (b) came from polysilicon open circuit detectors. Clusters near the wafer edge are typical, this one being due to over-etched polysilicon. One of the worst cluster-patterns observed is shown at (c). This one is due to under-etched polysilicon.

ings. These effects can be modeled by using size-dependent critical areas. The critical area in that case is defined as the area in which a defect of a given size must fall in order to cause a failure. This area not only depends on the defect size but also on the circuit dimensions and the failure modes. Mathematical expressions describing this area as a function of defect size were derived for the monitors. For the product chip, a computer model was used to determine the critical area as a function of size. Calculations were made independently for short circuits and open circuits on each photographic level.

The average critical area is obtained by taking the defect size distribution into account. The nature of this distribution can be deduced from the yields for monitors of different widths or spacings. This method showed that in most cases a $1/x^3$ dependency, for defects of size x , best fit the data. This dependence could only be deduced for defects greater than the minimum monitor width or spacing, which was $2.5 \mu\text{m}$. All average critical areas were calculated for defects above this size. The results of these calculations are shown in Table 1.

Experimental procedure

Monitor wafers were introduced into the process for manufacturing the 8-K memory chips described by Hoffman and Kalter [12]. Four sets with forty memory wafers per set were made. Each set also contained three monitor wafers with photo defect detectors and three wafers with leakage and pinhole detectors.

The patterns on the photo monitor wafers were detectors for open and short circuits. Long serpentine lines were used to measure open circuits. Patterns with parallel lines were used for detecting short circuits. Structures with different widths were designed to test sensitivities to various defect sizes. All of these patterns were combined into a test site. One-hundred-twenty such

test sites were printed on each wafer, and a pattern of fifty test sites was tested. Twenty-nine of these were designated for the inner zone; the other twenty-one were assigned to the outer zone. And, of course, the defect detectors were tested for open and short circuits.

For the open and short circuit detectors the data analysis was somewhat complex. Both clusters and random defects occurred. Both defect types also exhibited a strong radial variation. Any group of three or more failing sites adjacent to each other on the wafer was assumed to be a cluster. Such clusters were found to be an area phenomenon. The percentage of monitors lost due to such effects should correspond directly to the percentage of the product expected to be lost due to clustering.

Random defect failures were counted after the clusters were removed from the sample, and each defect type was analyzed independently of the others. An equivalent product yield was calculated from the results for both inner and outer zones, using the critical areas of Table 1.

The leakage and pinhole test sites were produced on wafers separate from the defect detectors. Thirty-seven monitors were tested on each wafer. Large diffused areas were used for leakage test patterns, the leakage monitors consisting of reverse-biased junctions. Leakage currents were measured and assumed to be failures when they exceeded a predetermined value. Strings of FET gates and conducting patterns, separated by thin or thick oxides, were designed for pinhole measurements. The pinhole detectors were tested for conductance through the insulators.

The leakage and pinhole monitor data were converted into defect densities and standard deviations using Eqs. (10) and (11). The yield for the product was then calculated by means of Eq. (6), or, in those cases where the standard deviation of the defect density was zero, by

$$Y = \exp(-A\bar{D}). \quad (12)$$

Results

The photographic process suffered from clustering due to poor resolution and uneven etching. The latter problem was primarily responsible for destroying a large number of polysilicon defect detectors. An example of the distribution of these failures is shown on the wafer maps in Fig. 1. The percentage of the test sites lost due to clustering is shown in Table 2. The data have been separated for the inner and outer zones. The results show that this effect occurs predominantly in the outer zone.

The yield losses in each column in Table 2 can be added to give an estimate of the total yield loss. The total cluster-limited yield is the complement of this loss. The results shown in Table 2 indicate a total loss of 12.6%, which is somewhat pessimistic, however, in that some of the clusters overlap. By constructing composite wafer maps, a better estimate can be derived for the losses. A distribution for the number of sites lost per wafer from such a composite is shown in Fig. 2. This distribution has an average of 5.9 failing test sites per wafer. The yield loss due to clusters is therefore 11.8%.

The distribution in Fig. 2 is extremely wide. Unfortunately, not enough data are available to describe it by an analytical expression. It is clear, however, that clustering causes large variations in yield from wafer to wafer.

This result also suggests that clustering with its associated radial effect is, to a large extent, responsible for the non-Poisson behavior of the yield statistics in this product.

Although the clustered failure patterns tend to look very impressive on the failure maps, it is the few random failures that lead to the significant yield losses in our experiment. The total cluster-limited yield was 87%. We next show that the total random defect-limited yield for photographic defects, leakage, and pinholes was 5%. These random defects caused the major losses.

To calculate the random defect densities, single repeating failures due to mask defects were removed from the samples. The total number of these failures was small, insufficient for determining the quality of the masks. The defect densities calculated from the remaining open and short circuit detector data are shown in Table 3. The densities are in defects per square centimeter for defects that are greater than 2.5 μm . In most cases, the standard deviation of the defect densities is greater than zero, suggesting that Poisson statistics are not applicable for modeling the defect-limited yield in these cases. The sample in this experiment was too small to determine a precise model for the random defect-limited yield. The results described in [6] were obtained from the same pilot line process described here. Those data were obtained from a larger sample so that the use of Eq. (6) for the yield model appears appropriate.

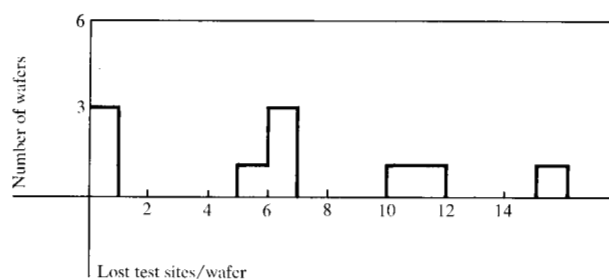


Figure 2 Distribution of number of test sites lost per wafer due to clustering.

Table 1 Critical areas for photodefects calculated using a $1/x^3$ defect size distribution. Some monitors had more than one pattern available. The critical areas are in mm^2 for defects larger than 2.5 μm .

Type of defect	Monitor	Product
Diffusion opens	0.0283	0.1884
Diffusion shorts	0.0094	0.7587
Polysilicon opens	0.0139	0.1628
	0.0143	
	0.0211	
Polysilicon shorts	0.0152	0.3466
	0.0153	
	0.0153	
Metal opens	0.0133	0.5059
	0.0171	
Metal shorts	0.0177	0.0492
	0.0102	
	0.0105	

Table 2 Percent losses due to clusters and the resulting cluster-limited yield.

Type of defect	Inner zone	Outer zone	Total wafer
Diffusion opens	1.0	2.9	1.8
Diffusion shorts	0	5.7	2.4
Polysilicon opens	0.1	9.3	4.0
Polysilicon shorts	1.4	5.1	3.0
Metal opens	0	2.9	1.2
Metal shorts	0.2	0.3	0.2
Totals	2.7	26.2	12.6
Cluster-limited yield	97.3	73.8	87.2

Table 3 Densities for random defects calculated from monitor data. Defect densities are in defects/ cm^2 for defects greater than 2.5 μm .

Type of defect	Inner zone		Outer zone	
	$\bar{D}$	σ_D	$\bar{D}$	σ_D
Diffusion opens	146	0	168	107
Diffusion shorts	74	184	102	0
Polysilicon opens	87	160	255	23
Polysilicon shorts	136	213	335	63
Metal opens	0	0	177	202
Metal shorts	53	21	298	0

Table 4 Limiting yields in percent calculated from monitor data. Final product test yield is shown at the bottom.

Defect type	Inner zone	Outer zone	Total wafer
Diffusion opens	76	74	75
Diffusion shorts	78	46	65
Polysilicon opens	89	66	79
Polysilicon shorts	73	32	56
Metal opens	100	55	81
Metal shorts	97	86	92
Total random photo	37	3.4	16
Photo clustering	97	74	87
Junction leakage ^a	55	55	55
Thin oxide pinholes ^a	67	67	67
Thick oxide shorts ^a	80	80	80
Total model	10.6	0.7	4.2
Actual yield	6.2	0.8	3.26

^aResults not available for inner and outer zone so total wafer yield is calculated and applied to both zones.

Table 5 Limiting yields in percent for different yield models. The Poisson model (e^{-AD}) appears to be the worst. Actual final test yield was 3.26%.

Yield detractor	Total limited yield from method in this paper	$\frac{1}{1 + AD}$	e^{-AD}
Diffusion opens	72	71	67
Diffusion shorts	63	42	25
Polysilicon opens	76	75	71
Polysilicon shorts	54	42	25
Metal opens	80	62	55
Metal shorts	92	93	92
Total photo	14	5.4	1.5
Leakage/pinholes	29	29	29
Total model	4.0	1.6	0.4

Table 6 Yield tracking with monitors. Although measurements were based on two or three monitor wafers per lot, results are good. Improvement in leakage was the result of an experiment.

Defect type	Lot 1	Lot 2	Lot 3	Lot 4
Diffusion leakage	33	26	59	100
Diffusion opens	75	79	70	65
Diffusion shorts	24	100	35	59
Thin oxide pinholes	44	58	82	84
Polysilicon opens	84	77	83	63
Polysilicon shorts	64	39	87	74
Thick oxide shorts	70	100	75	75
Metal opens	88	83	70	43
Metal shorts	92	90	93	95
Total model yield	0.8	2.7	4.2	4.6
Actual product yield	1.7	3.1	4.0	4.6

The resulting yields are shown in Table 4. The outer zone again shows the lowest yield. The most severe problems occur with short circuits between polysilicon patterns and short circuits between diffused patterns. Unfortunately, the 100% yield for metal open circuits in the inner zone was offset by a large number of open circuits in the outer zone. Also included in Table 4 are the equivalent product yields calculated for pinholes and leakage. These results were used to determine the indicated total model yield. The yields for the actual product that was produced at the same time as the test sites is given at the bottom of Table 4.

The model should have a higher yield than the actual product. Losses due to parametric variations, for example, threshold voltages, transconductance, and diffusion resistance, were not modeled in this experiment. Also omitted were alignment losses and missing contact holes. Inspection of the product showed that these effects combined should result in less than 10% yield loss.

Approximate yield prediction

The method of analysis used in this paper is rather tedious. For quick estimations of yield, one would like to be able to use simpler calculations. Most yield modelers tend to use the Poisson approximation given in Eq. (12), but the data in this paper show clearly that this is inappropriate. A better approach is the use of Seeds' formula [2]:

$$Y = 1 / (1 - \overline{AD}). \quad (13)$$

This equation is obtained by introducing an exponential defect density distribution into either Eq. (4) or (5). Such a density distribution has a σ/μ ratio with a value of one.

A second set of defect densities was calculated using Eq. (10) without removing the clusters from the data. The yields in Table 5 were obtained from these defect densities by using Eq. (13). The results agreed well with the actual product yield, which indicates that the errors were averaged out. Also shown in Table 5 is the yield calculated by the Poisson distribution of Eq. (12). The result indicates a much lower yield than that actually observed. This is in agreement with Murphy's original observations [1].

The above success led to further evaluation of the data. The defect densities were calculated for the defect monitors in each lot. No attention was given to clustering. Seeds' formula was then used to calculate an equivalent product yield for each yield detractor. The results are shown in Table 6. The product yields for each lot are given on the line with total model yields. The agreement between this yield and the model is quite good. Apparently, errors are small enough and cancel each other, on the average, to give dependable results. It thus appears that Eq. (13) provides an approximate yield model.

Conclusions

It has been shown that each yield detractor in a semiconductor product can be measured and modeled independently, and a total measurement of the yield losses can be obtained. The results of using this approach show that, although clustering may affect large areas of the wafers, isolated random defects cause the major yield losses. The process under investigation in this paper appeared to suffer from radial variation in random defect densities as well as clusters.

Results obtained by the technique described here are peculiar to the process under investigation. However, this method does make it possible to measure process differences between manufacturing lines and to quantify manufacturing techniques. It is also possible to develop cost versus yield strategies for the major yield detractors.

Appendix A: Mean and variance of a mixed Poisson distribution

Let the probability of having x failing monitors per zone be given by

$$\text{Prob}(X = x) = \int_0^\infty \frac{e^{-\lambda} \lambda^x}{x!} f(\lambda) d\lambda. \quad (\text{A1})$$

The mean value of x can then be derived by

$$\begin{aligned} \bar{x} &= \sum_{x=0}^\infty x \int_0^\infty \frac{e^{-\lambda} \lambda^x}{x!} f(\lambda) d\lambda \\ &= \int_0^\infty \left(\sum_{x=0}^\infty x \frac{e^{-\lambda} \lambda^x}{x!} \right) f(\lambda) d\lambda \\ &= \int_0^\infty \lambda f(\lambda) d\lambda = E(\lambda) = \bar{\lambda}. \end{aligned} \quad (\text{A2})$$

Similarly the mean value for x^2 is found to be

$$\begin{aligned} E(x^2) &= \sum_{x=0}^\infty x^2 \int_0^\infty \frac{e^{-\lambda} \lambda^x}{x!} f(\lambda) d\lambda \\ &= \int_0^\infty \left(\sum_{x=0}^\infty x^2 \frac{e^{-\lambda} \lambda^x}{x!} \right) f(\lambda) d\lambda \\ &= \int_0^\infty (\lambda + \lambda^2) f(\lambda) d\lambda \\ &= E(\lambda) + E(\lambda^2). \end{aligned} \quad (\text{A3})$$

Using this result, it is possible to derive our expression for the variance by

$$\begin{aligned} \text{var}(x) &= E(x^2) - E^2(x) \\ &= E(\lambda) + E(\lambda^2) - E^2(\lambda) \\ &= \bar{\lambda} + \text{var}(\lambda). \end{aligned} \quad (\text{A4})$$

Results (A2) and (A4) are the same as Eqs. (2) and (3) in the text.

Appendix B: Yield expression for a mixed Poisson distribution

If in the average yield equation

$$Y = \int_0^\infty \exp(-AD) f(D) dD, \quad (\text{B1})$$

where $f(D)$ is given by the gamma distribution,

$$f(D) = \frac{D^{\alpha-1} e^{-D/\beta}}{\Gamma(\alpha) \beta^\alpha}. \quad (\text{B2})$$

The integral in (B1) can be evaluated to give

$$Y = (1 + A\beta)^{-\alpha}. \quad (\text{B3})$$

The mean and variance of (B2) are given by

$$\bar{D} = \alpha\beta, \quad (\text{B4})$$

$$\text{var}(D) = \alpha\beta^2. \quad (\text{B5})$$

Solving these equations for α and β gives

$$\alpha = \bar{D}^2 / \text{var}(D), \quad (\text{B6})$$

$$\beta = \text{var}(D) / \bar{D}. \quad (\text{B7})$$

Substituting these results into (B3) gives

$$Y = [1 + A \text{var}(D) / \bar{D}]^{-\bar{D}^2 / \text{var}(D)}, \quad (\text{B8})$$

which is the same as Eq. (6) in the text.

Acknowledgments

The defect monitors used in these experiments were designed by D. Thomas and R. W. Douse. The leakage and pinhole monitors were designed by A. I. Wager and E. M. Wait. The author was helped with the data analysis and critical area calculations by G. F. Guhman and J. W. Hennessey. The many discussions with A. N. McLaren on statistics are gratefully acknowledged.

References

1. B. T. Murphy, "Cost-size Optima of Monolithic Integrated Circuits," *Proc. IEEE* **52**, 1537 (1964).
2. R. B. Seeds, "Yield, Economic, and Logistic Models for Complex Digital Arrays," *1967 IEEE Int. Conv. Rec.*, Part 6, 60 (October 1967).
3. W. G. Ansley, "Computation of Integrated-Circuit Yields from the Distribution of Slice Yields for the Individual Devices," *IEEE Trans. Electron Devices* **ED-15**, 405 (1968).
4. G. E. Moore, "What Level of LSI is Best for You?," *Electronics* **43**, 126 (February 1970).
5. C. H. Stapper, "Defect Density Distribution for LSI Yield Calculations," *IEEE Trans. Electron Devices* **ED-20**, 655 (1973).
6. R. M. Warner, Jr., "Applying a Composite Model to the IC Yield Problem," *IEEE J. Solid-State Circuits* **SC-9**, 86 (1974).
7. T. Yanagawa, "Yield Degradation of Integrated Circuits Due to Spot Defects," *IEEE Trans. Electron Devices*, **ED-10**, 190 (1972).
8. A. Gupta, W. A. Porter, and J. W. Lathrop, "Defect Analysis and Yield Degradation of Integrated Circuits," *IEEE J. Solid-State Circuits* **SC-9**, 96 (1974).

9. D. R. Thomas and R. D. Presson, "An Electrical Photolithographic Alignment Monitor," *Govt. Microcircuit Appl. Conference Digest*, 196 (1974).
10. R. Dennard and I. F. Chang, private communication.
11. T. R. Lawson, Jr., "A Prediction of the Photoresist Influence on Integrated Circuit Yield," *Solid State Technology* 7, 22 (1966).
12. W. K. Hoffman and H. L. Kalter, "An 8K Random-Access Memory Chip Using the One-Device FET Cell," *IEEE J. Solid-State Circuits*, SC-8, 298 (1973).

Received August 21, 1975; revised December 18, 1975

The author is located at the IBM System Products Division Laboratory, Burlington (Essex Junction), Vermont 05452.