

High Speed Transistor with Double Base Diffusion

Abstract: A high speed bipolar transistor has been fabricated by using double base diffusion to reduce the base resistance R_B . The base resistance forms two important time constants, $R_B C_D$ and $R_B C_C (R_L/R_E)$ with the emitter diffusion capacitance C_D and collector capacitance C_C dominating the switching delay of the circuits. We demonstrate that the base resistance of a single base diffused device can be reduced by a factor of four by using double base diffusion without affecting its cut-off frequency $f_t = 7$ GHz. The double base diffusion also increases the punchthrough voltage of the device from 3 to 7V.

Introduction

The general trend in bipolar integrated circuits is to increase circuit speed. Most current high speed transistor switching circuits are voltage driven; device base resistance thus plays a very important role in limiting circuit speed [1]. The base resistance R_B forms two important time constants, $R_B C_D$ and $R_B C_C (R_L/R_E)$, with the emitter diffusion capacitance C_D and the collector capacitance C_C , respectively. The collector capacitance, however, has to be multiplied by the voltage gain R_L/R_E , which usually has a range of 10 to 20 (R_L is the collector load resistance and R_E the emitter diode resistance). These two time constants dominate the switching delay of the circuit about equally, at least at low current levels.

The emitter diffusion capacitance is approximately

$$C_D = \frac{1}{2\pi f_t R_E}, \quad (1)$$

where f_t is the cut-off frequency and R_E can be expressed as

$$R_E = \frac{kT}{qI_E}, \quad (2)$$

where k is the Boltzmann constant, T the absolute temperature, q the electronic charge, and I_E the emitter current; C_D is usually 2 to 6 pF. The collector capacitance C_C can be reduced to about 0.1 pF with a pedestal type structure [2], and a method is described to reduce the base resistance while keeping C_D and C_C at their lowest possible levels.

The base resistance R_B is dominated by the resistance of the intrinsic base region underneath the emitter. The intrinsic base resistance can be reduced without increasing C_D by increasing the doping concentration in the intrinsic base region. Another possibility, reducing the emitter width with electron beam processing [3], is not discussed here.

Conceptual analysis

The pedestal collector is not essential for the base resistance reduction and is used only to reduce C_C to its lowest possible level. Figure 1 shows the structure and impurity profiles for a conventional pedestal-collector transistor [2]. Sections A-A and B-B depict the profiles in the intrinsic base and on the surface of the extrinsic base through the emitter, respectively. One obvious method for increasing the impurity concentration in the intrinsic base would be to increase the surface concentration of the base diffusion. The emitter-base breakdown voltage BV_{EBO} , however, sets an upper limit on the surface concentration of the base. The breakdown voltage is always lower on the surface than in the intrinsic base region, for two reasons. First, the doping concentration at the emitter-base junction is highest at the surface, as can be seen by comparing Section B-B with Section A-A. Second, the presence of surface states lowers the breakdown voltage [4]. For an ideal transistor, it would be desirable for the impurity concentration at the surface of the emitter-base junction to be somewhat lower than that in the intrinsic base region.

The impurity concentration in the intrinsic base can be increased without reducing the emitter-base breakdown voltage by adding a second base diffusion to the process as shown in Fig. 2. The first base diffusion is identical to that in Fig. 1. The second base diffusion, with a surface concentration higher than the first one, is made into the emitter window and is thus restricted to the intrinsic base region. Then the emitter window is enlarged in order that the emitter diffusion, which follows, will overlap the second base diffusion, as shown in Fig. 2. Due to this overlap, the sidewall and the surface of the emitter-base junction, where the reverse breakdown takes place, are formed in the less doped extrinsic base region. Section A-A of Fig. 2 shows the increased intrinsic base doping and also the steeper base

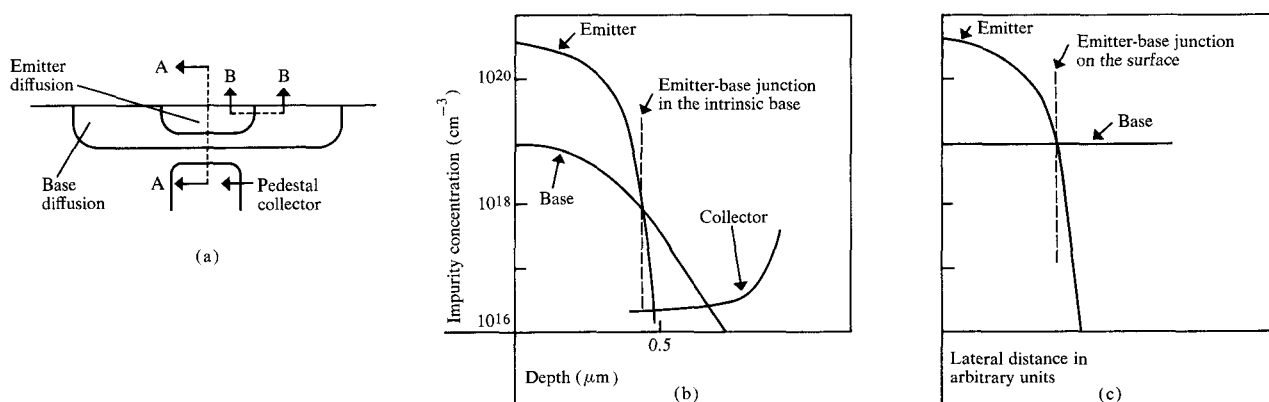


Figure 1 Impurity profile for pedestal-collector transistor. (a) Cross-sectional view of the pedestal-collector transistor; (b) impurity profile in the emitter, intrinsic base and pedestal-collector regions (A-A); (c) impurity profile in the emitter and extrinsic base regions on the surface (B-B).

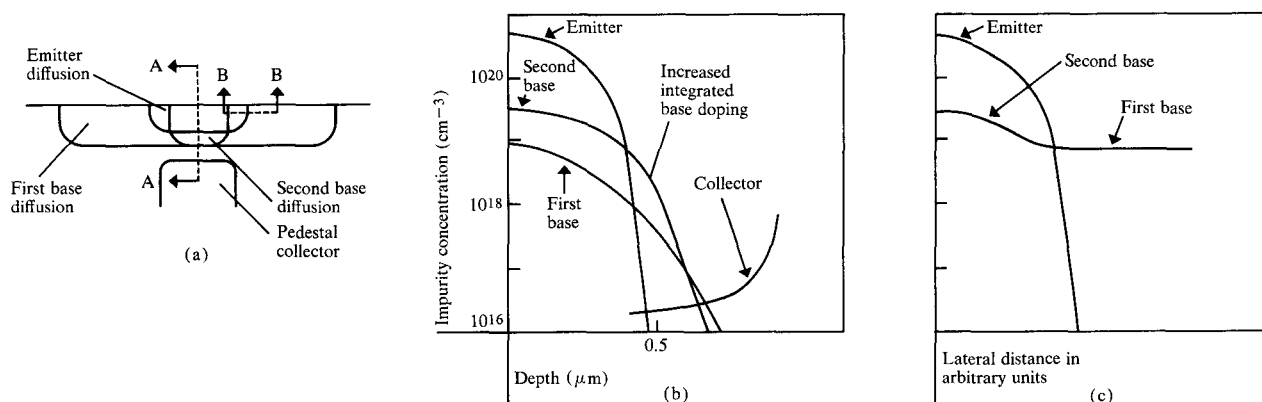


Figure 2 Impurity profile for double base diffused pedestal-collector transistor. (a) Cross-sectional view of the double base diffused transistor showing first and second base diffusion; (b) impurity distribution in emitter, intrinsic base and pedestal-collector regions (A-A); (c) impurity profile in the emitter and extrinsic base regions on the surface (B-B). The emitter intersects only the first base diffusion profile at the surface.

profile due to the second base diffusion. It can be seen by comparing Section B-B of Fig. 1 with Section B-B of Fig. 2 that the second base diffusion did not increase the impurity concentration of the surface of the emitter-base junction.

The double base diffused transistor has a further advantage over the single base diffused one: Its punch-through voltage V_p is increased due to the increased impurity concentration in the intrinsic base region. The punch-through voltage limits the supply voltage to about one half of its value [5]. The variation of electrical characteristics, like current gain, also increases with decreasing punch-through voltage. Since both C_D and V_p are proportional to the square of the base width W , V_p sets a lower limit on C_D . With increased intrinsic base concentration, this lower limit can be reduced, resulting in an additional decrease of the $R_B C_D$ time constant.

The steep base profile increases the built-in field in the intrinsic base [6] and reduces the base transit time. The advantage of the higher built-in field is, however, counterbalanced by the decreased mobility [7] due to the increased impurity concentration in the intrinsic base. Thus, the expected f_t is about the same as in the single base diffused transistor with equal base width.

Structure and processing

The processing starts with the diffusion of an arsenic-doped buried layer into a p-type substrate, followed by the growth of the first epitaxial layer to about $2 \mu\text{m}$ thick. After the first epitaxial growth, two arsenic-doped buried layers are diffused simultaneously. One of them forms the pedestal collector while the other forms a connection between the buried collector and the collector contact as shown in Fig. 3, in which both the horizontal

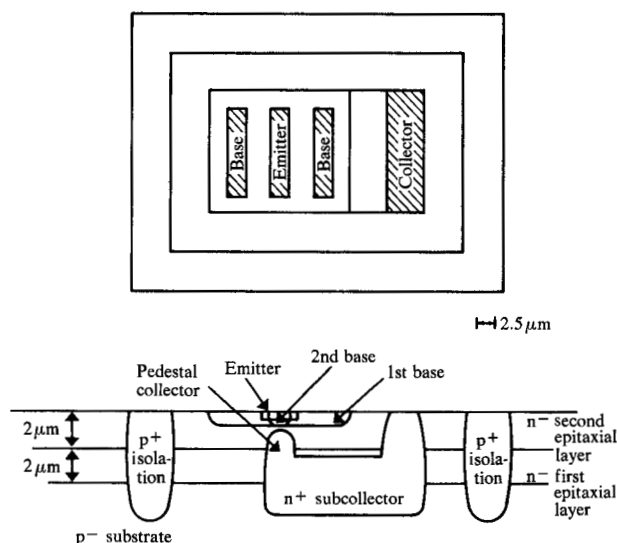


Figure 3 Horizontal and vertical structure of the pedestal-collector transistor with double diffused base.

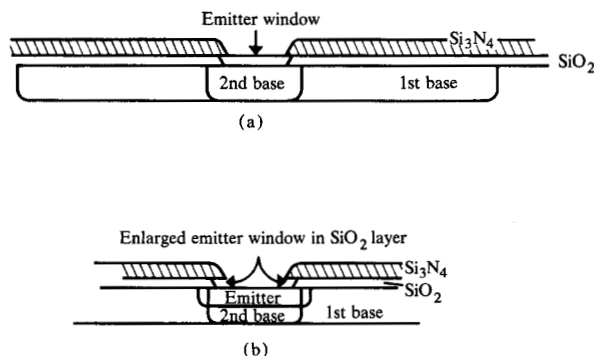


Figure 4 Processing of the double base diffused transistor. (a) Second base diffusion into the emitter window; (b) emitter window enlarged using dip etch (buffered HF), followed by emitter diffusion.

and vertical structures are shown for a pedestal-collector transistor with a double diffused base. Boron is then diffused into the isolation area and a second epitaxial layer about $2\text{ }\mu\text{m}$ thick is grown. A phosphorus diffusion is made into the second epitaxial layer to provide the collector contact. Then the first base diffusion goes into the entire base area. This diffusion is carried out in an open tube with boron tri-bromide (BBr_3) at 950°C for 20 minutes. The resulting sheet resistance, ρ_s , is $133\text{ }\Omega/\square$. This is followed by a drive-in cycle of 8 minutes at 970°C in argon. The sheet resistance after the drive-in cycle drops to about $69\text{ }\Omega/\square$ which shows that the boron glass formed during BBr_3 diffusion acts as a source. The base junction depth at this stage is about $0.22\text{ }\mu\text{m}$. A steam re-oxidation cycle at 970°C for 11 minutes follows. The re-

sulting sheet resistance is $200\text{ }\Omega/\square$ which indicates that a large amount of boron was removed from the silicon during growth of the oxide due to the low (0.3) segregation coefficient of boron [8]. A silicon nitride layer about $0.16\text{ }\mu\text{m}$ thick is deposited over the entire surface of the wafer. Emitter windows are opened in both the silicon nitride and the underlying SiO_2 . The second base diffusion is performed through the emitter window as shown in Fig. 4(a). The diffusion and drive-in cycles are the same as those used for the first base diffusion, except that the reoxidation cycle has been omitted. Thus the final sheet resistance of the second base diffusion is $69\text{ }\Omega/\square$ with a junction depth of $0.22\text{ }\mu\text{m}$. The corresponding surface concentration is much higher than that of the first base diffusion. The boron glass formed during the second base diffusion is removed with a dip etch. This dip etch also enlarges the emitter window in the underlying SiO_2 layer as shown in Fig. 4(b), which assures that the subsequent emitter diffusion overlaps the second base diffusion. The emitter diffusion process in this case uses an arsenic capsule at 1000°C for 150 minutes. During this long emitter diffusion time, both first and second base diffusions move ahead of the emitter. This redistribution results in a higher impurity concentration and a steeper profile in the intrinsic base, as compared to the extrinsic base, because of the higher surface concentration of the second base diffusion. Finally, all contact windows are opened and aluminum is deposited and defined.

The resulting transistor structure shows the sidewall of the emitter-base junction is formed in the first base diffusion with the lower surface concentration. Thus, the higher surface concentration of the second base diffusion does not degrade the breakdown of the emitter-base junction. The impurity profiles of the completed structure are shown in Fig. 2.

Figure 3 also shows that the buried collector diffused into the substrate extends from the collector contact region only to the pedestal-collector region, which reduces the collector-substrate capacitance. Punchthrough between base and substrate in the lightly doped, $\approx 5 \times 10^{15}\text{ cm}^{-3}$, epitaxial regions does not occur under normal operating conditions because the separation between base and substrate is about $3.5\text{ }\mu\text{m}$. In a non-pedestal structure, with a $2\text{ }\mu\text{m}$ single epitaxial layer, the buried collector region has to be extended beyond the base region to avoid base-to-substrate punchthrough that would render the device useless.

Electrical characteristics

The base width of the double base diffused transistor can be varied to obtain the highest possible f_t with an acceptable punchthrough voltage, thus minimizing C_D . It was found that the best compromise is an f_t of 7 GHz

with $V_p = 7$ V, which is acceptable for most circuit applications. The resulting double base diffused transistor compares favorably in every respect with the single base diffused device with an identical f_t of 7 GHz. The $R_B C_C$ time constant was measured [9] to compare the base resistance of the double and single base diffused transistors.

The electrical characteristics of both double and single base diffused transistors are shown in Table 1. The emitter-base breakdown voltage is 3.1 V for both cases and thus it was not affected by the second base diffusion. A control experiment with single base diffusion, but using the second base diffusion cycle, yielded $BV_{EBO} \approx 0$. The double base diffusion resulted in a decrease of the sheet resistance in the intrinsic base region from 15 to 5.6 k $\Omega/\square$ with a corresponding increase in V_p from 3 to 7 V. The most pronounced effect of the double base diffusion was on the $R_B C_C$ time constant, which was reduced from 10 to 2.3 ps at 5 mA collector current. Since the collector capacitances C_C of both structures are 0.094 pF, the base resistance R_B was reduced by a factor of more than four. The other electrical parameters are the same for both structures, as shown in Table 1.

Figure 5 shows the $R_B C_C$ time constant as a function of emitter current for both double and single base diffused transistors. It should be noted that the collector capacitance C_C in the $R_B C_C$ time constant is not the same as the C_C measured on a capacitance bridge, even if the bias on the collector junction is the same. The capacitance bridge gives a C_C value for zero emitter current, whereas the emitter current during the $R_B C_C$ measurement is non-zero, and thus C_C increases [10]. This increase in C_C is about 10 percent in our case, for a 5-mA (1.6×10^4 A/cm²) emitter current, and is linearly proportional to the current. Using this correction for the collector capacitance measured on a capacitance bridge, we can calculate the base resistance R_B from the $R_B C_C$ time constant for any emitter current level. The base resistance values at 5 mA, calculated for the double and single base diffused transistors, are 22 Ω and 96 Ω , respectively. The emitter diffusion capacitance C_D at 5 mA is about 4.3 pF for both structures, according to Eq. (1). Thus the $R_B C_D$ time constants at $I_E = 5$ mA are about 95 and 413 ps for the double and single base diffused transistors, respectively. Assuming a voltage gain R_L/R_E of 15, the $(R_L/R_E)R_B C_C$ time constants are 35 and 150 ps for the double and single base diffused transistors, respectively. It can be seen that the dominant time constant $R_B C_D$ is reduced from 413 to 95 ps, but it still dominates the switching delay of the transistor. By going through the same calculation one can show that reducing the current level of the switching circuit from 5 to 2 mA reduces $R_B C_D$ of the double base diffused transistor from 95 to about 54 ps, assuming a decrease of 10 percent in f_t . The corresponding $(R_L/R_E)R_B C_C$ time constant is 42 ps as

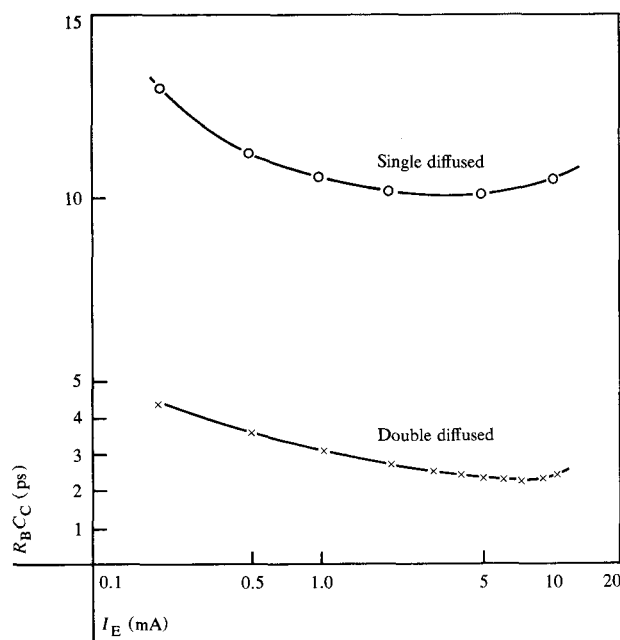


Figure 5 Time constant vs emitter current. The double base diffused transistor has an $R_B C_C$ time constant about four times lower than that of the single base diffused transistor.

Table 1 Electrical characteristics of double and single base diffused transistors.

Electrical parameters	Double base diffused transistor	Single base diffused transistor
BV_{CBO} at 10 μ A	10.0 V	6.0 V
BV_{EBO} at 10 μ A	3.1 V	3.1 V
V_p at 10 μ A	7.0 V	3.0 V
β at $I_E = 5$ mA, $V_{CB} = 0$	≈ 150	≈ 150
$R_B C_C$ at $I_E = 5$ mA, $V_{CB} = 0$	2.3 ps	10 ps
f_t at $I_E = 5$ mA, $V_{CB} = 0.5$ V	7 GHz	7 GHz
C_C at $V_{CB} = 0$	0.094 pF	0.094 pF
ρ_s of the first base diffusion	200 $\Omega/\square$	200 $\Omega/\square$
ρ_s of the second base diffusion	69 $\Omega/\square$	-----
R_{DB} (ρ_s in the intrinsic base)	5.6 k $\Omega/\square$	15 k $\Omega/\square$

determined from Fig. 5. It can be seen that both time constants are about equal at a current level of 2 mA.

It should be pointed out that both time constants, $R_B C_D$ and $(R_L/R_E)R_B C_C$, are small-signal parameters. Thus they can be used only in comparison with each other as a figure of merit and cannot be used to calculate directly the switching delay of the circuit.

Summary

We have demonstrated that the base resistance of a narrow-base transistor can be reduced by a factor of about four by increasing the doping concentration in the intrinsic base region, which was achieved by using double base diffusion. As a result of base resistance reduction, the two important time constants dominating the switching delay of the circuit were also reduced in proportion to the base resistance. The double base diffused transistor compares favorably in every respect with the single base diffused device. The optimum current level of the double base diffused transistor is about 2 mA, at which both time constants contribute equally to the circuit delay.

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