

Device Design Considerations for Ion Implanted n-Channel MOSFETs

Abstract: Device design considerations are presented for ion implanted, n-channel, polysilicon gate, enhancement-mode MOSFETs for dynamic switching applications. A shallow channel implant is used to raise the magnitude of the gate threshold voltage while also maintaining a low substrate sensitivity (i.e., without substantially increasing the dependence of the threshold voltage on the source-to-substrate "backgate" bias). Design trade-offs between channel implantation energy and dose and substrate bias were examined using both computer analyses and experimental devices. The design objective was to identify the combination of these three parameter values that gives both a low substrate sensitivity and a steep subthreshold conduction characteristic under the conditions of a gate threshold voltage of 1 V and a substrate bias range of 0 to -1 V. One-dimensional and two-dimensional computer analyses were performed to predict the effect of the device parameters on the electrical characteristics. MOSFETs were then fabricated to investigate the extremes of the design parameter range, and the experimental and predicted device characteristics were compared. An enclosed device structure proved particularly useful in evaluating the subthreshold characteristic at very low values of drain current.

Introduction

In this paper we consider some aspects of device design for ion implanted enhancement-mode MOSFET switching devices. This work is part of a research program to develop a very high density FET technology for digital integrated circuits. A cross section of the n-channel polysilicon gate MOSFET chosen for this study is shown in Fig. 1(a). The physical feature of the design that we are primarily concerned with is the vertical doping profile of the silicon in the region beneath the gate. This doping profile can be altered by an implanted surface layer which extends below the shallow inversion layer that forms the conducting channel between source and drain. For convenience we will refer to this implantation as the channel implant. The reason for using a channel implant in these enhancement-mode devices is to raise the gate threshold voltage, V_T , while also maintaining a low substrate sensitivity. By a low substrate sensitivity we mean that V_T should be relatively insensitive to changes in the source-to-substrate (backgate) bias, V_{S-sub} , as illustrated in Fig. 1(b). Another device characteristic of concern is the subthreshold conduction or "turn-on" characteristic shown in Fig. 1(c). The subthreshold conduction characteristic must be as steep as possible so that the gate voltage excursion, ΔV_G , between the device "off" condition and the device "on" condition will be minimized [see Fig. 1(c)].

The device design parameters available for manipulation include the gate oxide thickness, the channel doping profile (i.e., the channel implantation energy and dose),

the substrate doping, and the substrate bias. The p-type doping concentration of the silicon in the region beneath the gate was increased by using low energy (20 to 40 keV), low dose (2 to $8 \times 10^{11} \text{ cm}^{-2}$) B^{11} ions implanted through the gate oxide. The shallow n^+ source and drain regions were high energy (100 keV), high dose ($4 \times 10^{15} \text{ cm}^{-2}$) As^{75} implants which are self-aligned with respect to the polysilicon gate. The choice of a 2000-Å source and drain junction depth, 350-Å gate oxide thickness, and 2 ohm-cm ($7.5 \times 10^{15} \text{ cm}^{-3}$) substrate resistivity were dictated by short channel considerations described elsewhere [1]. When the channel length of an FET becomes comparable to the source and drain depletion layer widths, smaller gate voltages are required to form a conducting channel under normal operating conditions, and the threshold voltage becomes dependent on both channel length and drain voltage [2]. In the extreme these detrimental short channel effects cause the FET to become a depletion-mode (normally-on) type of device. The channel lengths of the FETs investigated in our device design study (2 to 10 μm) are long enough, that short channel effects such as source-to-drain depletion layer punchthrough can be neglected for drain voltages as high as 4 V.

The device parameters that remain at our disposal are the channel implantation energy and dose (i.e., the vertical doping profile under the gate oxide), and the substrate bias. The design objective was to identify the combination of these three device parameter values that

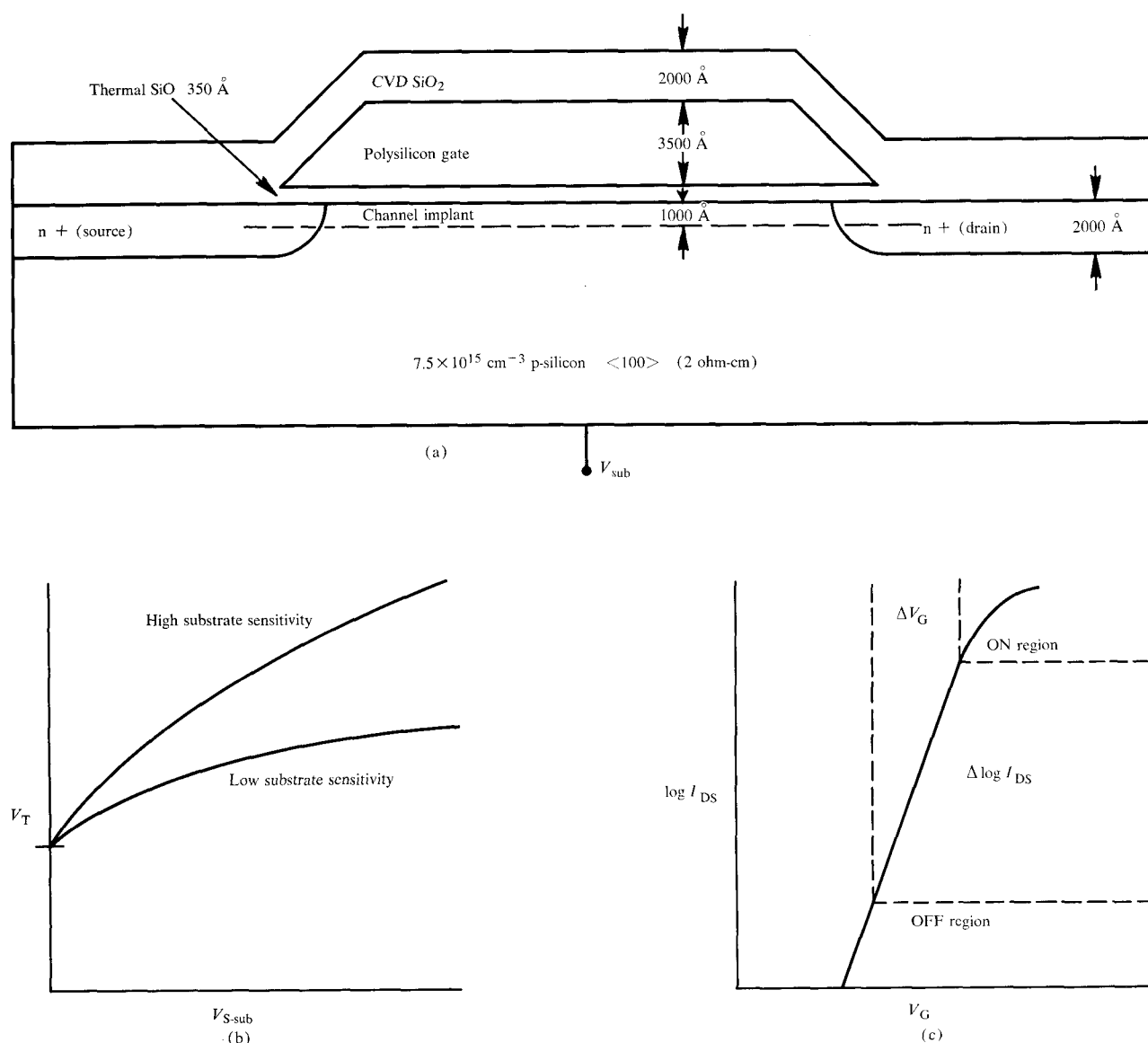


Figure 1 (a) Cross section of an n-channel polysilicon gate MOSFET. (b) Typical substrate sensitivity characteristic. (c) Typical subthreshold conduction characteristic.

yields both a low substrate sensitivity and a steep subthreshold conduction characteristic. In other words, we designed for a threshold voltage that is relatively insensitive to source voltage variations and for a small gate voltage swing during turn-on [cf. Figs. 1(a) and 1(b)].

Two analytical tools were utilized in this study. The first is a one-dimensional analysis based on Poisson's equation that predicts the effect of the three design parameters on the substrate sensitivity. The second is a two-dimensional computer model for current transport

that predicts the effect of the design parameters on the subthreshold conduction characteristic. The predictions of these analyses were used to establish the useful range of device parameters. Then MOSFETs were fabricated to investigate the extremes of the design parameter range, and the experimental and predicted device characteristics were compared.

Vertical doping profile

The vertical doping profile of the implanted region beneath the gate oxide is shown in Figs. 2(a) and 2(b) for

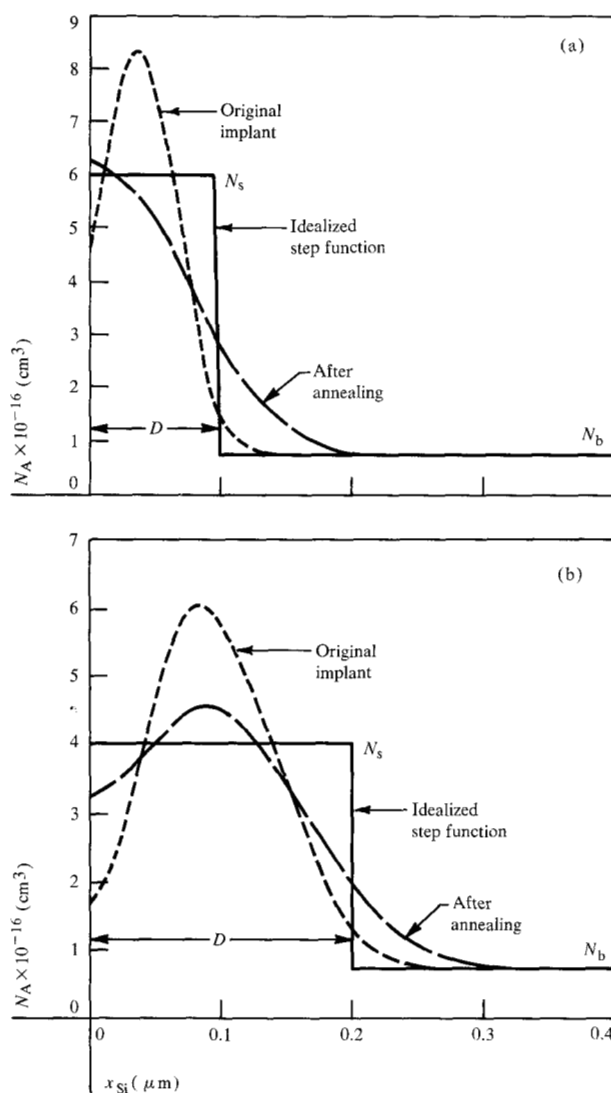


Figure 2 Vertical doping profile of implanted region beneath the gate for 20 keV (a) and 40 keV (b) implantation energies. Idealized step functions of width D have the same active dose as the actual implantation profiles. Values used in the profile calculations were (a) $R_p = 700 \text{ \AA}$, $\Delta R_p = 300 \text{ \AA}$, and $t_{ox} = 350 \text{ \AA}$, and (b) $R_p = 1300 \text{ \AA}$, $\Delta R_p = 500 \text{ \AA}$, and $t_{ox} = 350 \text{ \AA}$.

implantation energies of 20 and 40 KeV respectively. A computer program developed by F. F. Morehead of our laboratory was used to predict the shape of the implantation profiles after their subsection to the heat treatments used in device processing. The heat treatments were 34 minutes at 870°C , 20 minutes at 900°C , and 11 minutes at 1000°C . Before heat treatment the shapes of the profiles are Gaussian, but during thermal processing the profiles become distinctly non-Gaussian because of the reflection at the oxide-silicon interface of boron atoms diffusing primarily during the 11-minute 1000°C step. Doping tails on the implanted Gaussian distributions

resulting from channeling were neglected because the implants were performed 7 degrees off axis from the vertical.

The 20 to 40 keV range of channel implantation energy was established as follows. In order to minimize thermal spreading of the implanted profile, we implanted through the gate oxide. The active dose fractions that penetrate the $350\text{-\AA}$ -thick gate oxide were calculated to be 88 and 97 percent for the 20 and 40 keV cases, respectively. For implantation energies below 20 keV the oxide begins to absorb an intolerably large fraction of the implanted ions, whereas above 40 keV the profile becomes so deep that high substrate sensitivity results.

To first order, a step function of depth D having the same active dose can be used to approximate the actual implantation profile. For example, after heat treatment, step depths of 1000 and 2000 $\text{\AA}$ correspond quite well to implants with a range and straggle of 700 and 300 $\text{\AA}$ (20 keV) and 1300 and 500 $\text{\AA}$ (40 keV), respectively [see Figs. 2(a) and 2(b)]. In the analytical work that follows we use a step profile because its effects on the device characteristics are easy to model and understand, and also because we find that the calculated results using the step profile and the actual profile are very close in value.

Substrate bias

The MOSFET is a four terminal device (source, gate, drain, and substrate), and the magnitude of the substrate bias is an important and useful parameter that must be considered in device design. The one-dimensional threshold voltage analysis based on Poisson's equation is described in detail in the Appendix. In the simple case of uniform substrate doping, the gate threshold voltage, V_T , is proportional to $[(V_{S\text{-}sub} + \psi_s) N_b]^{1/2}$ [3] where $V_{S\text{-}sub}$ is the source-to-substrate (back gate) bias, ψ_s the total band bending in the silicon at the onset of strong inversion [2] (i.e., the surface potential), and N_b the bulk semiconductor doping concentration. A similar form of dependence of threshold voltage on source-to-substrate bias and doping concentration occurs when a nonuniform (i.e., implanted) doping profile is used (see Appendix). The V_T versus $V_{S\text{-}sub}$ relationship (i.e., the substrate sensitivity characteristic) is of particular importance in source-follower applications. Examples include the FET switch in a one-device memory cell, and other memory and logic circuits in which an FET is used as a load device. In the source-follower mode of operation the drain voltage is held constant and the source voltage swings or follows the gate voltage variation. As a result the source voltage also varies with respect to the fixed substrate bias (i.e., $V_{S\text{-}sub}$ also varies). Consequently, the threshold voltage increases as the FET is turned on, and if the substrate sensitivity is too large the device turn-on can be impaired.

Threshold equations

The one-dimensional threshold voltage equations used in this analysis are derived in the Appendix using the basic threshold equation [3];

$$V_T = V_{FB} + \psi_s + V_{bulk}. \quad (1)$$

The flat-band voltage, V_{FB} , for an n^+ polysilicon gate is given by

$$V_{FB} = -E_g/2 - \psi_s/2 - q N_{ox}/C_{ox}, \quad (2)$$

where E_g is the energy gap, N_{ox} the equivalent oxide charge per unit area at the oxide-silicon interface, C_{ox} the oxide capacitance per unit area, and q the electronic charge. With an n^+ polysilicon gate and uniform substrate doping concentration, the band bending in the silicon at the onset of strong inversion is given by [4]

$$\psi_s = (2kT/q) \ln(N_b/n_i), \quad (3)$$

where k is Boltzmann's constant, T the absolute temperature, N_b the bulk doping concentration, and n_i the intrinsic carrier concentration. The bulk voltage term, V_{bulk} , from Poisson's equation is given by

$$V_{bulk} = (q/C_{ox}) \int_0^{w_d} N_a(x) dx, \quad (4)$$

where w_d is the depletion layer width in the silicon substrate beneath the gate oxide, and $N_a(x)$ the concentration profile of ionized acceptors in the depletion region.

The one-dimensional threshold voltage expression, Eq. (1), and the flat-band voltage expression, Eq. (2), can be obtained from consideration of the energy-band diagram at the oxide-silicon interface. Modification of the magnitude of the threshold voltage occurs primarily through the term V_{bulk} (which depends strongly on both the silicon doping profile and on the source-to-substrate bias), although minor changes also arise from the logarithmic dependence of the silicon band bending on the doping concentration. Equation (3) represents the strong inversion criterion originated by Brown [4], which defines the magnitude of the band bending at the silicon surface relative to the bulk (i.e., the surface potential) when the concentration of minority carriers at the surface equals the concentration of majority carriers in the bulk [2]. In this study we have chosen not to incorporate the effect of a nonuniform doping profile into Brown's criterion in order to facilitate comparison between the threshold voltage equations for different doping profiles. As derived in the Appendix, the threshold equations of interest are

Uniform doping profile (nonimplanted) [3]

$$V_T = V_{FB} + \psi_s + [(2q N_b \epsilon_{Si}/C_{ox}^2)(V_{S-sub} + \psi_s)]^{1/2}. \quad (5)$$

Impulse doping profile (step depth $D = 0$, active implanted dose = DOSE)

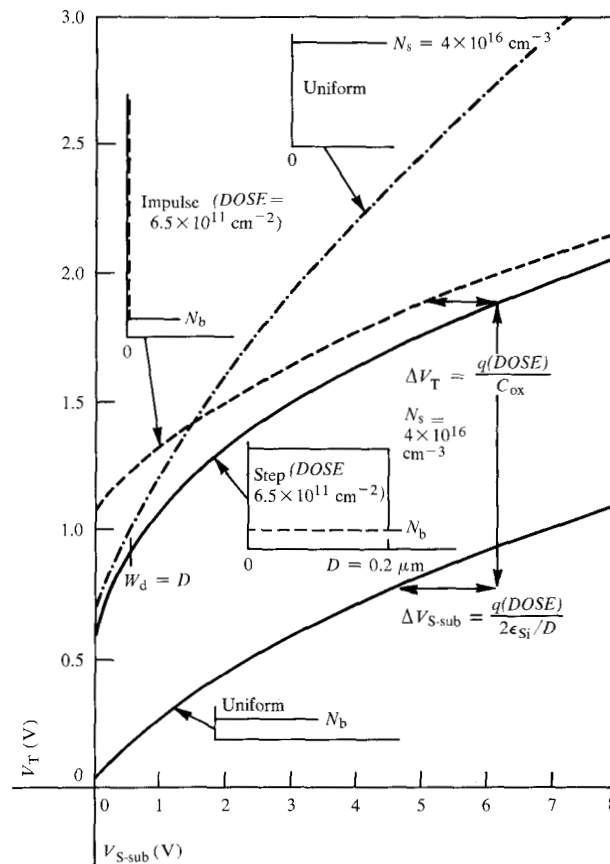


Figure 3 Calculated substrate sensitivity characteristics for various doping profiles; uniform (nonimplanted) low substrate doping $\cdots\cdots$, uniform (nonimplanted) high substrate doping --- , impulse doping --- , and step doping --- . The impulse and step profiles have equal active doses of $6.5 \times 10^{11} \text{ cm}^{-2}$. Shifting up the uniform low doping characteristic by $\Delta V_T = q(\text{DOSE})/C_{ox}$ yields the impulse profile characteristic. The uniform high doping and impulse cases yield asymptotes for the step profile. For $w_d > D$, the step profile characteristic is obtained by shifting the uniform low doping profile up by $\Delta V_T = q(\text{DOSE})/C_{ox}$ and to the right by $\Delta V_{S-sub} = q(\text{DOSE})/(2\epsilon_{Si}/D)$ (see text); N_b , the bulk doping concentration, is equal to $7.5 \times 10^{15} \text{ cm}^{-3}$ in all cases.

$$V_T = V_{FB} + \psi_s + q(\text{DOSE})/C_{ox} + [(2q N_b \epsilon_{Si}/C_{ox}^2)(V_{S-sub} + \psi_s)]^{1/2}. \quad (6)$$

Step doping profile ($w_d \leq D$)

$$V_T = V_{FB} + \psi_s + [(2q N_s \epsilon_{Si}/C_{ox}^2)(V_{S-sub} + \psi_s)]^{1/2}. \quad (7)$$

Step doping profile ($w_d \geq D$)

$$V_T = V_{FB} + \psi_s + q(N_s - N_b)D/C_{ox} + \{(2q N_b \epsilon_{Si}/C_{ox}^2) \times [V_{S-sub} + \psi_s - q(N_s - N_b)D/(2\epsilon_{Si})]\}^{1/2}. \quad (8)$$

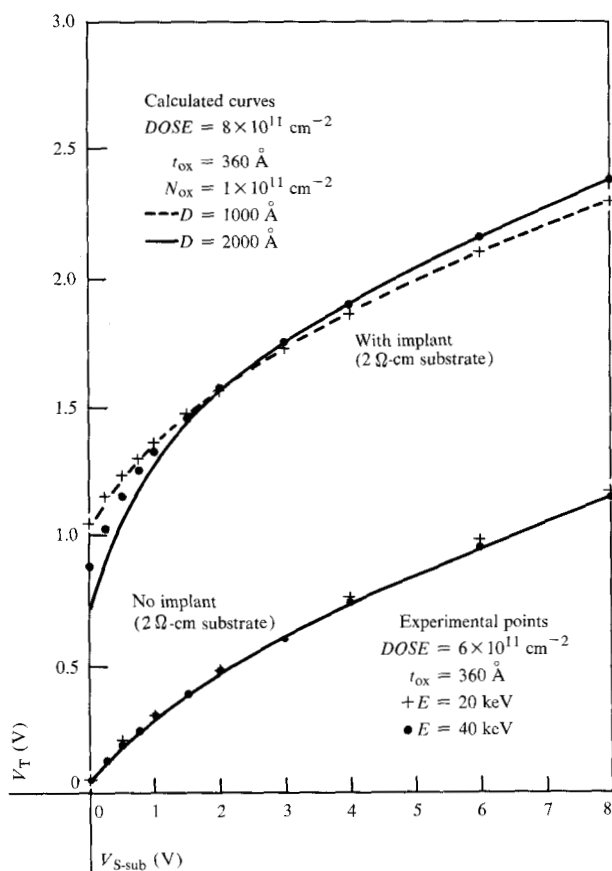


Figure 4 Correlation of experimental and calculated substrate sensitivity characteristics. The lower curves are for nonimplanted 2 ohm-cm ($7.5 \times 10^{15} \text{ cm}^{-3}$) substrates. The upper curves are for 20 and 40 keV B^{11} channel implantation energies with the same substrate doping. During implantation, half of the wafer was masked by a metal foil so that implanted and nonimplanted MOSFETs could be fabricated on the same wafer.

In the threshold equations above, ϵ_{Si} is the dielectric constant for silicon, and N_s the step doping concentration.

Figure 3 shows the substrate sensitivity characteristics for various doping profiles calculated using Eqs. (5) through (8). Let us first examine the characteristics for the light and heavy uniform doping cases shown in Fig. 3. Notice that a light uniform substrate doping concentration of $7.5 \times 10^{15} \text{ cm}^{-3}$ (2 ohm-cm resistivity) yields a low substrate sensitivity, but the threshold voltage is also low; so low, in fact, that the FET is almost a depletion mode device. A heavier uniform doping of $4 \times 10^{16} \text{ cm}^{-3}$ ($\frac{1}{2}$ ohm-cm resistivity) raises the threshold voltage as shown, but only at the expense of a greatly increased substrate sensitivity. The obvious solution is to use a lightly doped substrate and a shallow channel implant to increase the substrate doping in the region beneath the

gate oxide, thereby raising the threshold voltage while still maintaining a low substrate sensitivity over the operating source-to-substrate bias range.

For any given active implantation dose, the maximum attainable increase in the threshold voltage and the minimum substrate sensitivity occur when the dose is completely concentrated at the oxide-silicon interface, as exemplified by the impulse profile. In comparing Eqs. (5) and (6) it is apparent that an impulse of negative charge (e.g., ionized boron acceptors) localized at the interface simply shifts the nonimplanted characteristic up by $\Delta V_T = q(\text{DOSE})/C_{\text{ox}}$ [5, 6]. Thus the impulse doping profile increases the threshold voltage without changing the substrate sensitivity associated with the bulk doping (see Fig. 3).

In a reality a true impulse doping profile is impossible to obtain with ion implantation and thus the profile has some finite shape. Figure 3 also shows the substrate sensitivity for a step profile of width $D = 0.2 \mu\text{m}$ having the same active dose as the impulse profile. As shown in Fig. 3, the uniform high doping profile and the impulse profile represent the two extremes of the step profile, and thus they yield asymptotes for the substrate sensitivity curve of the step profile. As $V_{\text{S-sub}}$ is increased, the depletion layer width, w_d , exceeds the step depth, D , and the character of the substrate sensitivity curve for the step profile changes from high uniform doping behavior [Eq. (5)] to impulse doping behavior [Eq. (6)]. For the step profile the active implanted dose is $\text{DOSE} = (N_s - N_b) D$. In comparing Eqs. (5) and (8) we see that for $w_d > D$ the effect of the step is to shift the characteristic of the unimplanted profile up by $\Delta V_T = q(\text{DOSE})/C_{\text{ox}}$ as in the impulse case, and to the right by $\Delta V_{\text{S-sub}} = q(\text{DOSE}) (D/2\epsilon_{\text{Si}})$. The term $D/2\epsilon_{\text{Si}}$ represents the capacitance per unit area of half of the step width. Thus ΔV_T is determined by the magnitude of the implanted dose, and $\Delta V_{\text{S-sub}}$ by the moment of the dose, i.e., the dose multiplied by one half of its width. Although somewhat idealized, the step function profile offers a simple and direct first-order understanding of the influence of channel implantation step height and width (i.e., implantation dose and energy) on substrate sensitivity.

The rationale for performing the channel implant after growing the gate oxide should now be clear. By minimizing the thermal spreading of the implanted profile we keep the implant bunched and as close as possible to the oxide-silicon interface so that it more nearly resembles the preferred impulse profile. This helps to minimize the degradation of substrate sensitivity as we raise the threshold voltage with a channel implantation.

Substrate sensitivity

We now consider the degree of correlation between experimental results and the predictions of the one-

dimensional threshold analysis using the step profile. The experimental threshold voltage was determined by extrapolating the linear (below pinchoff) I_{DS} versus V_G characteristic to zero current [3]. As a check, the $(I_{DS})^{1/2}$ versus V_G characteristic of the above-pinchoff region was also extrapolated to zero current and was found to give the same threshold value. Figure 4 shows the results for device runs with an experimental dose of $6 \times 10^{11} \text{ cm}^{-2}$ B¹¹ for implantation energies of 20 and 40 keV. In each case half of the wafer was masked so that some devices would not receive a channel implant. The experimental results for both 20 and 40 keV cases are matched very well by a calculated dose of $8 \times 10^{11} \text{ cm}^{-2}$. This discrepancy between the calculated and experimental doses is believed to be caused by an inaccuracy in the dose calibration of the particular implantation machine used. We have consistently observed that the calculated dose exceeds the experimental dose by about 30 percent.

In Fig. 4 the slight deviation of the calculated and experimental curves near $V_{S-sub} = 0 \text{ V}$ occurs because we ignore the effect of the implanted doping layer on the silicon band bending [5, 6] (see Appendix). For the same dose, the deviation is larger for deeper implants because $w_d = D$ occurs at a larger value of V_{S-sub} . The nonimplanted (i.e., uniform doping) characteristic can, of course, be fitted more precisely because the band bending can be more accurately defined.

Two important circuit requirements that our device design must meet are the threshold voltage of approximately 1 V and a substrate bias range of 0 to -1 V. During a source-follower switching operation, the source voltage swing is from ground potential up to +4 V; hence the operational range of V_{S-sub} is at least 0 to +4 V and at most +1 to +5 V. Note from Fig. 4 that the substrate sensitivity is higher for the 40 keV case than for the 20 keV case, especially near $V_{S-sub} = 0$. This means that if the 40 keV implant is used, some substrate bias must be employed to reduce the substrate sensitivity.

We now examine substrate sensitivity with respect to the three design parameters of channel implantation energy and dose, and substrate bias. Figure 5 shows calculated substrate sensitivity curves for three different step profiles of interest, identified as cases A, B, and C in the figure. Case A is a step of $0.1 \mu\text{m}$ intended for use at a substrate bias of zero volts. Cases B and C are step depths of 0.1 and $0.2 \mu\text{m}$ intended for use at -1 V substrate bias. All three cases give the required threshold of approximately 1 V for zero source voltage, but they use three different surface dopings and three different channel doses. Note that the two $0.1 \mu\text{m}$ cases exhibit less substrate sensitivity than the $0.2 \mu\text{m}$ case, which reiterates our earlier conclusion that one must use some substrate bias for deeper implants in order to maintain low substrate sensitivity.

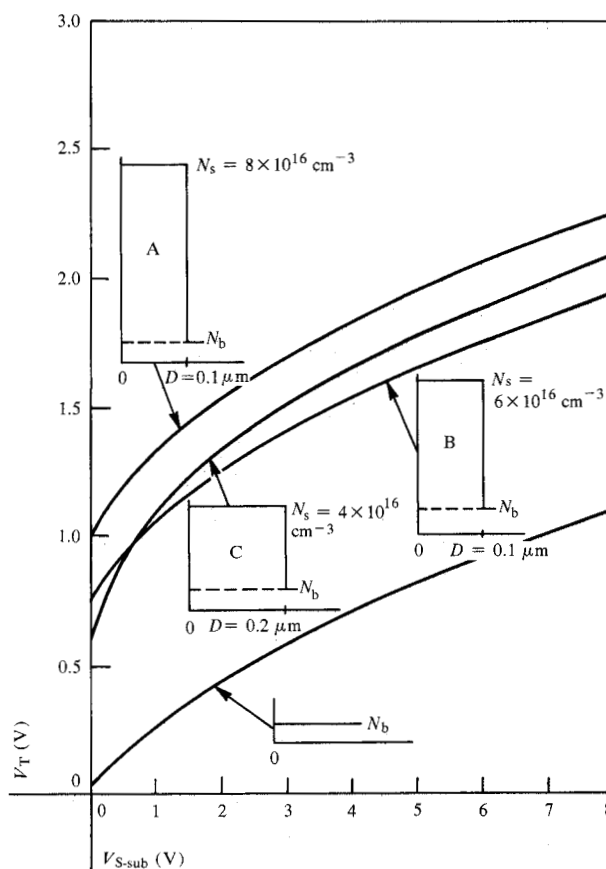


Figure 5 Calculated substrate sensitivity characteristics for the uniform low doping case and for three different step implantation profiles of interest. Case A is a $0.1 \mu\text{m}$ step intended for use with zero applied substrate bias. Cases B and C have step depths of 0.1 and $0.2 \mu\text{m}$, respectively, and are intended for use with -1 V applied substrate bias. All three cases give the required gate threshold voltage, V_T , of approximately 1 V for zero source voltage, but they use three different surface dopings and three different active channel doses; N_b is equal to $7.5 \times 10^{15} \text{ cm}^{-3}$ in all cases.

Subthreshold conduction

A test chip containing enclosed and the conventional open MOSFET structures with various channel lengths was designed and fabricated using polysilicon gate technology. Figure 6 is a scanning electron microscope photograph of an enclosed FET structure. In this enclosed device the polysilicon gate surrounds the central source region, and the drain in turn surrounds the gate. When the source is completely surrounded by the gate, source-to-drain leakage currents resulting from parasitic channels or sneak paths are eliminated. In a conventional open structure, adjacent devices are isolated from each other by a field oxide that also contacts the edges of the source, channel and drain regions of each FET. In n-channel devices in particular, unless very effective field shields or parasitic channel stoppers are provided,

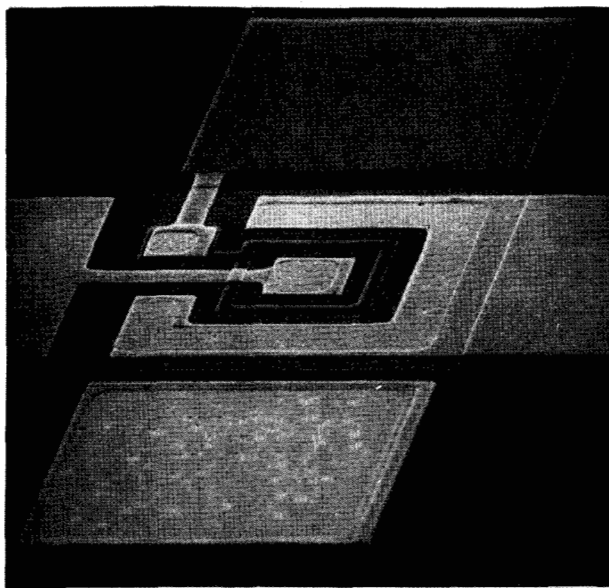


Figure 6 Scanning electron microscope photograph of an enclosed FET. The aluminum pads measure 4 mils by 4 mils ($100 \mu\text{m} \times 100 \mu\text{m}$) [2] and the channel length is $2.4 \mu\text{m}$. Clockwise from the bottom the pads connect to the substrate, source, gate, and drain regions.

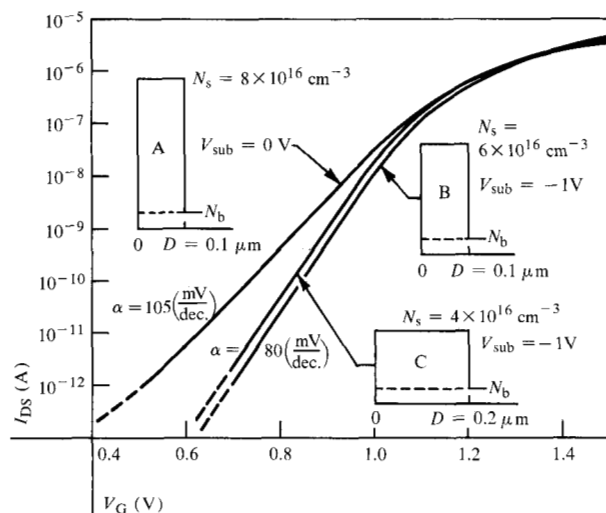


Figure 7 Calculated subthreshold conduction characteristics for the three different step implantation profiles used earlier in the substrate sensitivity analysis (see Fig. 5). The subthreshold characteristics for cases B and C have a steeper slope (i.e., smaller α) than that of case A because of both a larger substrate bias and a smaller active channel dose [see Eqs. (9) and (10)]; N_b is equal to $7.5 \times 10^{15} \text{ cm}^{-3}$ in all cases.

source-to-drain leakage current paths can occur along the surfaces of the field oxide. For experimental purposes, the enclosed structure is useful in determining the subthreshold conduction characteristic at very low drain currents. The subthreshold or turn-on characteristic

[7, 8] is of particular importance to dynamic memory and logic circuits because those circuits require very low leakage currents when the FET switch is turned off [6].

The step doping profile was incorporated [9] into the two-dimensional FET computer model of Kennedy and Murley [10] and the logarithmic I_{DS} versus V_G characteristics were generated. Figure 7 shows the calculated subthreshold behavior for the three step profiles used earlier in analyzing the subthreshold behavior (see Fig. 5). To obtain the data of Fig. 7 we have assumed a $10 \mu\text{m}$ channel length and a width to length ratio of one to one. The two-dimensional current transport model was used to confirm that channel lengths as short as $2 \mu\text{m}$ cause no significant perturbation of these characteristics, and that replacing the step doping profile with the actual profile also has little effect on the predicted results.

The inverse semilogarithmic slope, α , of the subthreshold characteristic for weak inversion is given by [6, 8]

$$\alpha \left(\frac{\text{mV}}{\text{decade}} \right) = \frac{dV_G}{d \log_{10} I_{DS}} = \left(\frac{kT}{q} \right) \left(\frac{1}{\log_{10} e} \right) \left(1 + \frac{\epsilon_{\text{Si}} t_{\text{ox}}}{\epsilon_{\text{ox}} w_d} + \frac{C_{\text{fs}} t_{\text{ox}}}{\epsilon_{\text{ox}}} \right), \quad (9)$$

where t_{ox} is the thickness of the gate insulator, ϵ_{ox} the dielectric constant of the insulator, and C_{fs} the capacitance per unit area due to fast surface states. In our design the only variable at our control in Eq. (9) is the depletion layer width, which is a function of the source-to-substrate bias, the silicon band bending, and the doping profile in the depletion region. Again ignoring the effect of doping concentration on the band bending, we are left with our original three design parameters; substrate bias, and channel implantation depth and dose. Then, because $w_d > D$ for the three cases considered in Fig. 7, we may utilize Eq. (A-10) of the Appendix:

$$w_d = \left\{ (2\epsilon_{\text{Si}}/qN_b) [V_{\text{S-sub}} + \psi_s - q(N_s - N_b)D(D/2\epsilon_{\text{Si}})] \right\}^{1/2}. \quad (10)$$

Note from Eqs. (9) and (10) that an increase in the magnitude of the substrate bias, or a decrease in the active channel dose, $(N_s - N_b)D$, or step width, D , causes w_d to increase with a resultant reduction in α (i.e., a steeper slope). In Fig. 7, the subthreshold characteristics for cases B and C have a steeper slope than that of case A because of both a larger substrate bias and a smaller channel dose. In order to obtain the required threshold voltage of approximately 1 V one can either increase the dose or the substrate bias (see Fig. 5). From the point of view of subthreshold behavior, the largest allowable substrate bias magnitude (-1 V) and the shallowest practical channel implant (20 keV) are preferred because they yield the steepest turn-on characteristic.

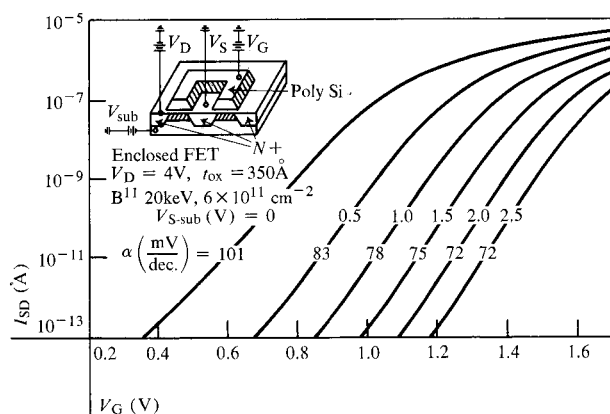


Figure 8 Experimental subthreshold conduction characteristics with V_{S-sub} as parameter for a channel implantation energy of 20 keV. The inset shows a cross section of the enclosed FET structure used in these measurements. The enclosed device has a channel length of $2.4 \mu\text{m}$ and a width-to-length ratio of 65 to 1. The current scale has been reduced by a factor of 65, which is equivalent to a channel width-to-length ratio of one to one, to facilitate comparison with the computed results shown in Fig. 7.

Figures 8 and 9 show the effect of the substrate bias on the slope of the experimental subthreshold characteristic for 20 and 40 keV implants, respectively. (A cross section of the enclosed FET used in these measurements is shown in the inset of Fig. 8.) The enclosed devices had a channel length of $2.4 \mu\text{m}$ and a width to length ratio of 65 to one. The magnitude of the current in Figs. 8 and 9 was reduced by a factor of 65, which is equivalent to a channel width to length ratio of one to one, to facilitate comparison with the computed results of Fig. 7. Both Figs. 8 and 9 confirm that increasing the substrate bias decreases α (i.e., increases the slope) as predicted in Fig. 7. From Eq. (10), because w_d is proportional to $(V_{S-sub})^{1/2}$, the rate at which α decreases decays as V_{S-sub} increases. Figures 8 and 9 represent almost equal active doses (88 and 97 percent of $6 \times 10^{11} \text{ cm}^{-2}$ respectively) but their respective step depths are approximately 1000 and 2000 Å. As expected from Eqs. (9) and (10), at any given value of V_{S-sub} the 20 keV implant (which corresponds to the smaller step depth) yields a steeper subthreshold characteristic than the 40 keV implant.

Summary

In this paper we have examined the design trade-offs between three device design parameters for normally-off n-channel FETs. The three parameters are channel implantation energy and dose and substrate bias. A shallow channel implant was used in these enhancement-mode devices to raise the gate threshold voltage while still maintaining a low substrate sensitivity. The design objective was to identify a combination of device parameter values that gives both a low substrate sensitivity

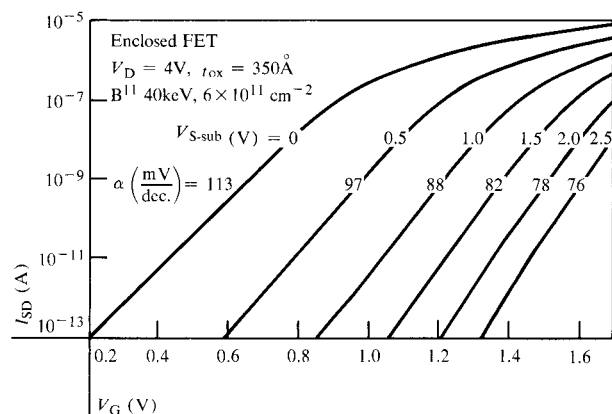


Figure 9 Experimental subthreshold conduction characteristics with V_{S-sub} as a parameter as in Fig. 8 but for a channel implantation energy of 40 keV. The 40 keV implant does not yield as steep a subthreshold characteristic as the 20 keV case [see Eqs. (9) and (10)].

and a steep subthreshold characteristic under the requirements of a threshold voltage of 1 V and a substrate bias range of 0 to -1 V . One-dimensional and two-dimensional analyses were performed to predict the effect of the design parameters on the device characteristics and reasonable agreement between calculated and experimental results was observed.

For our dynamic source-follower applications the preferred design choice is a 20 keV channel implant with a dose of about $6 \times 10^{11} \text{ cm}^{-2}$, and a substrate bias of -1 V . Implantation energies as high as 40 keV can be used if one is willing to pay the penalty of a slight increase in substrate sensitivity.

Acknowledgments

We acknowledge the processing support of the silicon technology facility under the direction of H. N. Yu, the ion implantation support of B. L. Crowder and F. F. Morehead, and the many helpful discussions with R. H. Dennard, J. J. Walker and V. DiLonardo assisted with the mask design and device testing.

Appendix: Derivation of threshold equation

• Case 1—uniform (nonimplanted) doping profile

The one-dimensional threshold equation for a uniformly doped substrate is [3]

$$V_T = V_{FB} + \psi_s + V_{bulk}, \quad (\text{A-1})$$

where the flat-band voltage, V_{FB} , for an n^+ polysilicon gate is given by

$$V_{FB} = -E_G/2 - \psi_s/2 - q N_{ox}/C_{ox}, \quad (\text{A-2})$$

and the silicon band bending, ψ_s , is given by [4]

$$\psi_s = (2kT/q) \ln(N_b/n_i). \quad (\text{A-3})$$

To calculate the bulk voltage term, V_{bulk} , we need to know the depletion layer width. Given $V_{\text{S-sub}}$ and ψ_s we can obtain the expression for w_d from Poisson's equation,

$$V_{\text{S-sub}} + \psi_s = (q/\epsilon_{\text{Si}}) \int_0^{w_d} \left[\int_0^{w_d} N_a(x) dx \right] dx. \quad (\text{A-4})$$

Again employing Poisson's equation we obtain V_{bulk} ,

$$V_{\text{bulk}} = (q/C_{\text{ox}}) \int_0^{w_d} N_a(x) dx. \quad (\text{A-5})$$

For a uniform (nonimplanted) doping profile, Eqs. (A-4) and (A-5) yield

$$\begin{aligned} V_{\text{bulk}} &= qN_b w_d / C_{\text{ox}} \\ &= [(2qN_b \epsilon_{\text{Si}} / C_{\text{ox}}^2) (V_{\text{S-sub}} + \psi_s)]^{1/2}. \end{aligned} \quad (\text{A-6})$$

• *Case 2—impulse doping profile (step depth $D=0$)*

An impulse of negative charge (ionized boron acceptors) localized at the oxide-silicon interface is equivalent to decreasing the oxide charge in Eq. (A-2) by the amount q (DOSE) where DOSE is the number of active implanted charges per unit area of the impulse. Therefore, for the impulse profile,

$$V_T = V_{\text{FB}} + q(\text{DOSE})/C_{\text{ox}} + \psi_s + V_{\text{bulk}}. \quad (\text{A-7})$$

The effect of the impulse is to simply increase the magnitude of the threshold voltage predicted by Eq. (A-1) by the amount $q(\text{DOSE})/C_{\text{ox}}$ [5, 6]. The impulse is assumed to have no effect on the magnitude of ψ_s .

• *Case 3—step doping profile ($w_d \leq D$)*

To adapt Eq. (A-1) to a step doping profile we must first define ψ_s (where ψ_s many now be a function of w_d) and then use Eqs. (A-4) and (A-5) to obtain the bulk voltage term. For $w_d \leq D$, Eq. (A-4) yields

$$w_d = [(2\epsilon_{\text{Si}}/qN_s)(V_{\text{S-sub}} + \psi_s)]^{1/2}, \quad (\text{A-8})$$

and then Eq. (A-5) gives

$$\begin{aligned} V_{\text{bulk}} &= qN_s w_d / C_{\text{ox}} \\ &= [(2qN_s \epsilon_{\text{Si}} / C_{\text{ox}}^2) (V_{\text{S-sub}} + \psi_s)]^{1/2}. \end{aligned} \quad (\text{A-9})$$

Eq. (A-9) has the same form as Eq. (A-6) except that now the step doping concentration N_s , replaces the bulk doping concentration, N_b .

• *Case 4—step doping profile ($w_d \geq D$)*

For $w_d \geq D$, Eq. (A-4) yields

$$\begin{aligned} w_d &= \{(2\epsilon_{\text{Si}}/qN_b)[V_{\text{S-sub}} + \psi_s \\ &\quad - q(N_s - N_b)D(D/2\epsilon_{\text{Si}})]\}^{1/2}, \end{aligned} \quad (\text{A-10})$$

and then Eq. (A-5) gives

$$\begin{aligned} V_{\text{bulk}} &= (q/C_{\text{ox}})[(N_s - N_b)D + N_b w_d] \\ &= q(N_s - N_b)D/C_{\text{ox}} \\ &\quad + \{(2qN_b \epsilon_{\text{Si}} / C_{\text{ox}}^2)[V_{\text{S-sub}} + \psi_s \\ &\quad - q(N_s - N_b)D(D/2\epsilon_{\text{Si}})]\}^{1/2}. \end{aligned} \quad (\text{A-11})$$

For $w_d = D$, Eqs. (A-8) and (A-10), and Eqs. (A-9) and (A-11) give identical results, as required.

We now consider the possible effect of the implanted doping step on the band bending at the silicon surface. For $w_d \gg D$, $\psi_s \rightarrow (2kT/q) \ln(N_b/n_i)$ and the substrate sensitivity will begin to resemble that of the impulse profile (see Fig. 3) [6, 7]. For $w_d \leq D$, however, ψ_s will become a function of both N_s and D . For example, for $w_d \leq D$ one could use [11] $\psi_s = (2kT/q) \ln[N_s(x=w_d)/n_i]$, but this would lead to a discontinuity in the magnitude of V_T at $w_d = D$. Another approach is to utilize some form of smoothing of ψ_s as w_d exceeds D , e.g., $\psi_s = (2kT/q) \ln(\int_0^{w_d} N_a(x) dx / w_d n_i)$. In this work, however, N_s and N_b differ by at most an order of magnitude, and the inclusion of the effect of the step on ψ_s causes a worst case perturbation (at $V_{\text{S-sub}} = 0$) of $(2kT/q) \ln(N_s/N_b) = 60$ mV in the predicted value of V_T (see Fig. 4). Consequently we have utilized $\psi_s = (2kT/q) \ln(N_b/n_i)$ in all of the calculations presented in this study. In using a singular value for ψ_s for in all cases, we ignore the small potential step in the band structure that arises due to the electronic dipole at $w_d = D$ resulting from the doping transition. Thus we have chosen to ignore the effect of the implanted ions on the silicon band bending in exchange for analytical simplicity and continuity of the substrate sensitivity characteristic.

References

1. R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. LeBlanc, "Design of Ion-Implanted MOSFET with Very Small Physical Dimensions," *IEEE T. Solid-State Circuits* SC-9, 256 (1974).
2. H. S. Lee, "An Analysis of the Threshold Voltage for Short Channel IGFET's," *Solid-State Electron.* 16, 1407 (1973).
3. D. L. Critchlow, R. H. Dennard, and S. E. Schuster, "Design and Characteristics of n-Channel Insulated-gate Field-effect Transistors," *IBM J. Res. Develop.* 17, 430 (1973).
4. W. L. Brown, "n-Type Surface Conductivity on p-Type Germanium," *Phys. Rev.* 91, 518 (1953).
5. M. Kamoshida, "Threshold Voltage and "Gain" Term β of Ion-implanted Enhancement-mode n-Channel MOS Transistors," *Appl. Phys. Lett.* 22, 404. (1973).
6. R. M. Swanson and J. D. Meindl, "Ion-Implanted Complementary MOS Transistors in Low-Voltage Circuits," *IEEE J. Solid-State Circuits* SC-7, 146 (1972).
7. M. B. Barron, "Low Level Currents in Insulated Gate Field Effect Transistors," *Solid-State Electronics* 15, 293 (1972).

8. R. R. Troutman and S. N. Chakravarti, "Subthreshold Characteristics of Insulated-Gate Field-Effect Transistors," *IEEE Trans. Circuit Theory* **CT-20**, 659 (1973).
9. F. H. Gaensslen and A. LeBlanc, "Simulation of Micron MOS Device Characteristics," presented at the European Solid-State Device Research Conference, Munich, Sept. 18, 1973.
10. D. P. Kennedy and P. C. Murley, "Steady State Mathematical Theory for the Insulated Gate Field Effect Transistor," *IBM J. Res. Develop.* **17**, 1 (1973).
11. G. Doucet and F. Van De Wiele, "Threshold Voltage of Nonuniformly Doped MOS Structures," *Solid-State Electronics* **16**, 417 (1973).

Received April 18, 1974

The authors are located at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598.