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Design and Characteristics of n-Channel Insulated-gate Field-effect Transistors

Abstract: An n-channel insulated-gate field-effect transistor technology established at IBM Research has served as the basis for further development leading to FET memory. Designs and characteristics of experimental devices of 500 and 1000 Å gate insulator thicknesses are presented, with particular attention to the effects of source-drain spacing.

Introduction

Because the insulated-gate field-effect transistor [1,2] shows great promise for applications in high-density memory and logic, there has been an effort in the IBM Research Center over the last decade to develop materials, devices, and circuit applications for this technology. An early choice was made to pursue n-channel devices because their mobility, which is higher by a factor of two to three than that of p-channel devices, offers a corresponding improvement in performance (delay-power product) [3]. The characteristics of experimental devices that were designed and fabricated during this period are described in this paper. The device technology was incorporated into integrated memory prototypes that provided experience for the development of the FET memory in IBM System/370, Models 158 and 168. Two different experimental device designs evolved, one using a 1000Å gate insulator thickness and the other using a 500Å thickness; these designs permitted an exploration of the advantages and problems of thinner insulators.

The next section of this paper gives an introductory description of the device operation and some of its main characteristics, using the 500Å device for illustration. The subsequent section gives a more thorough representation of the dc characteristics of both types of devices, including the effects of channel length (source-drain separation).

The conclusion one may draw is that the n-channel device offers very desirable properties for circuit design, having conduction characteristics approximating those predicted by the conventional equations with an effective mobility of 510 cm^2/volt-sec. The device threshold tends to be reasonably low, because of the negative work function difference between the aluminum gate and the p-type substrate, and can be adjusted to a desired value by choice of an appropriate substrate bias voltage. The threshold is particularly low, well-controlled and relatively insensitive to source-substrate voltage for the 500Å device. These devices allow the use of low circuit voltages with a correspondingly low power consumption if gate insulators of this thickness can be reliably fabricated.

Device description

The n-channel IGFET device, Fig. 1, consists of a p-doped substrate, n^+ diffusions to form the source and drain electrodes and a metal gate electrode insulated from the substrate by a thin layer of oxide. A set of grounded source characteristics of such a device with a 500Å gate oxide thickness is shown in Fig. 2(a).

The operation of the device can be studied under three distinct conditions as shown in Figs. 2(b),(c), and (d). The first condition, that of a turned-off device, occurs when the gate voltage measured with respect to the source, V_{GS}, is less than a critical threshold voltage, V_T. The charge in the channel region between the source and drain is depleted as shown in Fig. 2 (b), or may be accumulated (heavily p-type) in the case of a gate voltage that is much less than V_T. Because the p-type substrate is tied to a fixed bias potential below that of the grounded source, both source and drain are reverse-biased with respect to the substrate and are thus surrounded by depletion layers. In this condition there is no path for conduction between source and drain.

When the gate-to-source voltage, V_{GS}, is greater than V_T, the electric field causes the channel region between source and drain to be inverted to n-type as shown in

Fig. 2(c), which allows current conduction from the drain to the source (electron flow from source to drain) when a voltage is applied to the drain. The current increases nearly linearly with drain-source voltage, V_{DS}, for low values of V_{DS} as shown in Fig. 2(a).

This applied drain voltage causes an IR drop to be distributed along the channel, with the potential rising from ground to V_{DS} as the channel is traversed from source to drain. The voltage from gate to channel is thus diminished in the vicinity of the drain, and the reduced field causes the electron concentration to be less as expressed pictorially by the channel depth in Fig. 2(c). For a large drain voltage ($V_{DS} > V_{GS} - V_T$) the channel is "pinched off" completely near the drain as shown in Fig. 2(d) since there is insufficient field strength from the gate to turn on the channel. Current continues to flow through the space-charge region between the drain and the end of the channel. Further increases in drain voltage are dropped across the space charge region, and,

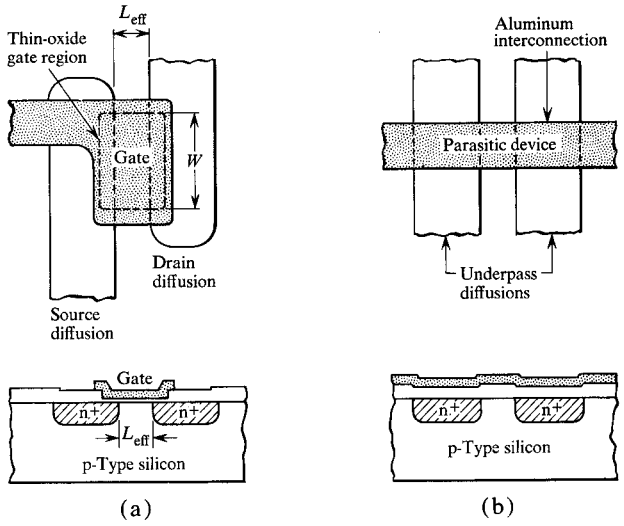
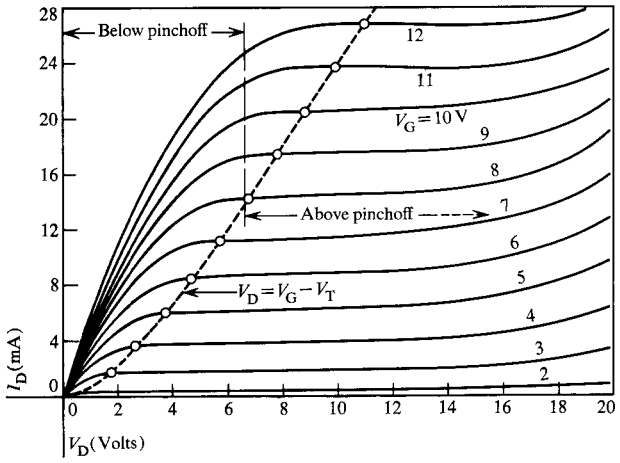
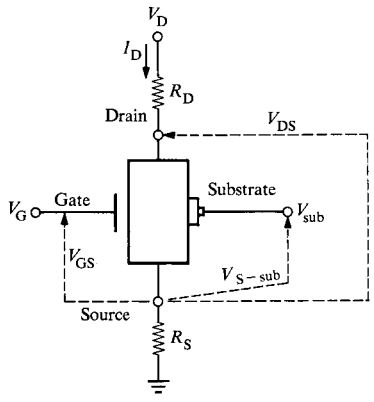


Figure 1 Structure of the IGFET thin-oxide device (a) and of the unwanted (parasitic) thick-oxide device (b).

Figure 2 Typical grounded-source characteristics for a 500Å device with illustrations and approximate device equations (not including R_D and R_S) for three different regions of operation. ($W = 4$ mil; $L_{eff} = 0.18$ mil; $V_{sub} = -7$V.)

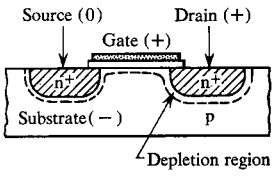




(a) Grounded-source characteristics

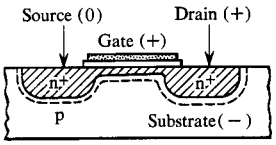
(b) Turned-off device ($V_{GS} < V_T$)

$I_D = 0$



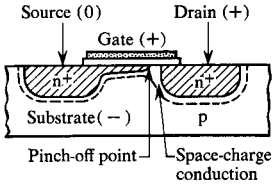
(c) Turned-on device ($V_{GS} > V_T$), below pinchoff ($V_{DS} < V_{GS} - V_T$)

$$I_D = \mu_{eff} \frac{\epsilon_{ox}\epsilon_o}{t_{ox}} \frac{W}{L_{eff}} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) V_{DS}$$



(d) Turned-on device ($V_{GS} > V_T$), above pinchoff ($V_{SD} > V_{GS} - V_T$)

$$I_D = \frac{\mu_{eff}}{2} \frac{\epsilon_{ox}\epsilon_o}{t_{ox}} \frac{W}{L_{eff}} (V_{GS} - V_T)^2$$



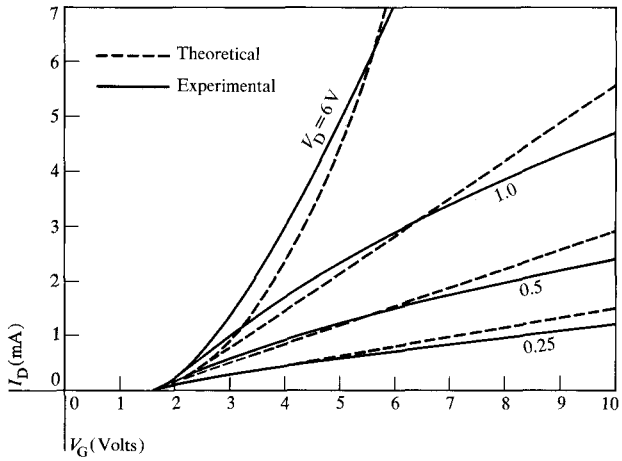
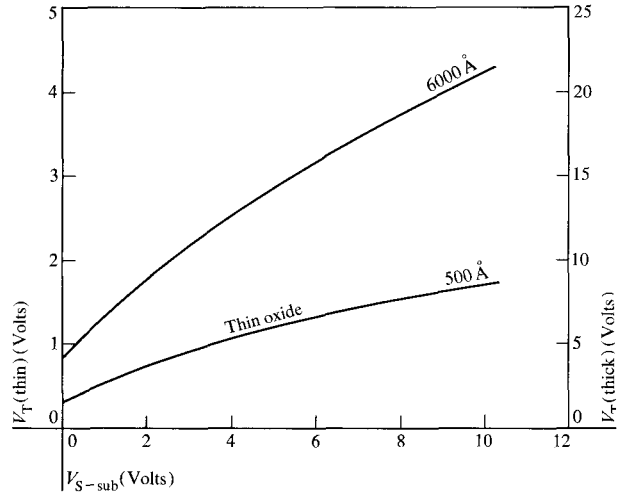


Figure 3 Transfer characteristics of a 500Å device compared with theoretical device equations for constant γ_m. ($W = 4$ mil; $L_{eff} = 0.18$ mil.)

since the voltage across the channel from the source to the pinch-off point is fixed, the current determined by this voltage and the channel resistance remains nearly constant as illustrated in the characteristics of Fig. 2(a) in the "above pinch-off" region of drain-source voltage. A small increase in current versus drain voltage is seen because the pinchoff point moves toward the source and lowers the effective channel resistance.

As shown in the theoretical equations for the device in Fig. 2, the current that flows for a given set of potentials is proportional to the effective channel mobility, μ_{eff}; the dielectric constant of the insulator, $\epsilon_0\epsilon_{ox}$; the inverse of the oxide thickness, t_{ox}; and the width-to-length ratio, W/L_{eff} of the device. W is the width of the channel as shown in Fig. 1 and L_{eff} is the length determined by the separation of the source and drain diffusion boundaries. The actual channel mobility is not a constant; it is at a peak for a gate voltage just above threshold and decreases gradually as the gate voltage is increased [4]. For purposes of digital circuit design an average or effective mobility, μ_{eff}, can be defined for the operating range of interest; in the equations of Fig. 2 this value is equal to 510 $cm^2V^{-1}s^{-1}$. The equations do not include the parasitic resistances R_D and R_S in the drain and source, respectively, due principally to the sheet resistance of the diffusion.

In order to simplify the equations and to give a practical set of units for design purposes; the transconductance has been normalized with respect to both the width-to-length ratio and the operating voltage of the device. The term $[\mu_{eff}(\epsilon_0\epsilon_{ox}/t_{ox})]$ has been defined as the normalized transconductance, γ_m, of the device. For the 500Å device, γ_m is about 36μmhos/V (and for the 1000Å device it is 18μmhos/V) measured under specified conditions.



$$V_T = \frac{t_{ox}}{\epsilon_0\epsilon_{ox}}\left[-Q_{ss} - Q_{ox} + \sqrt{2\epsilon_0\epsilon_{si}qN_{a,eff}(V_{s\text{-}sub} + \psi_s)}\right] + \Delta W_F + \psi_s + \Delta V_{DT}$$

V_T = Minimum gate to source voltage to turn device on
ϵ_{ox} = Relative dielectric constant of oxide under gate electrode ($\epsilon_{ox} = 4$ for SiO_2)
ϵ_{si} = Relative dielectric constant of silicon ($\epsilon_{si} = 12$)
ϵ_0 = Dielectric constant of free space (8.85×10^{-14} Farads/cm)
t_{ox} = thickness of oxide under gate
q = electronic charge (1.6×10^{-19} coulombs)
Q_{ox} = oxide charge (considered to be located at Si-SiO_2 interface)
Q_{ss} = surface state charges at Si-SiO_2 interface
$N_{a,eff}$ = effective impurity concentration level of substrate including allowance for boron depletion
$V_{S\text{-}sub}$ = voltage applied between source and substrate
ΔW_F = work function difference between aluminum and silicon (−0.8 V for p-type substrate)
ψ_s = voltage across depletion layer at the onset of conduction in the absence of a substrate potential (0.75 V for 2.3 ohm-cm p-type silicon)
ΔV_{DT} = shift in threshold due to boron depletion effect

Figure 4 Theoretical threshold characteristic vs applied source-substrate voltage (plotted for $Q_{ox} + Q_{ss} = 0.5 \times 10^{11}$ cm^{-2}, $N_{a,eff} = 5.0 \times 10^{15}$ cm^{-3}, $\Delta V_{DT} = -0.07$V).

The transfer characteristic, I_D vs V_G, of the device is shown in Fig. 3 for different values of drain voltage. The calculated curves using the equations of Fig. 2 are also shown, assuming that γ_m remains constant at the standard value discussed above.

The potential difference between the source and the substrate has an effect upon the threshold. Therefore the IGFET must be considered as a four-terminal device. The "substrate characteristic" of the 500Å device is illustrated in Fig. 4 along with the "threshold equation" [5]. This equation is fundamental to device design and is used to establish threshold tolerances and to make design trade-offs among substrate doping, oxide thickness and substrate voltage (factors which are, of course,

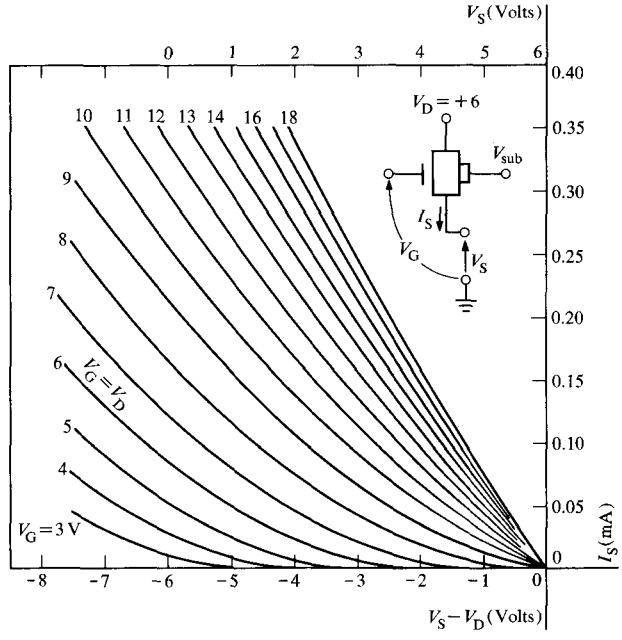


Figure 5 Grounded-drain (load device) characteristics. (500Å device; $W/L_{eff} = 1/4$.)

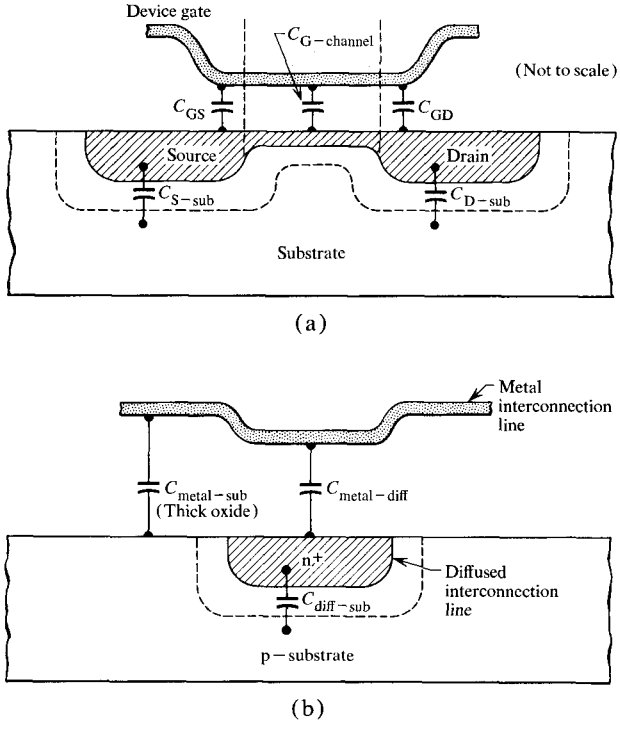


Figure 6 Illustration of (a) device capacitances and (b) interconnection capacitances.

common to all devices on an integrated circuit chip). Since devices in some applications have a source voltage that varies relative to substrate potential during circuit operation, the threshold equation is also one of the basic circuit design equations. The slope of the substrate characteristic, which determines the rate at which the threshold voltage changes with source-to-substrate voltage, is called the "substrate sensitivity." For a given gate oxide thickness and voltage the substrate sensitivity is affected mainly by the substrate doping level. A low doping level will minimize substrate sensitivity and junction capacitances, but will adversely affect the characteristics of small devices if the depletion depths become comparable to the source/drain separation. The doping level chosen in this case is a reasonable compromise. (In the derivation of the threshold equation, an effective value of doping level of the substrate is used, to account for the fact that the boron dopant is partially depleted close to the surface during oxidation processes due to the segregation coefficient between boron-doped silicon and oxide. From the same effect a small shift in voltage, ΔV_{DT}, also must be introduced [6].) For the n-channel device, a fixed substrate bias is usually employed to raise the threshold voltage (with grounded source) up to a nominal level that is adequate for circuit design when one takes into account the spreads in threshold voltage to be expected due to variation in the device parameters. A value of $V_{sub} = -7$V has been used for this purpose.

As indicated in Fig. 1, a parasitic IGFET device is formed when a metal interconnection line crosses two adjacent diffusions. If this device were turned on by the application of sufficient potential to the metal line, a "leakage" path that is deleterious to circuit operation would be formed. To prevent this, the fact that the threshold increases with oxide thickness is utilized by making the oxide under the interconnection lines thick enough to raise the threshold of this "thick oxide" device to a value greater than the highest voltage applied to the circuit. In practice the ratio of "thick oxide" to "thin oxide" thresholds and thicknesses is of the order of 10 to 1 for practical circuit designs. The substrate characteristic of a 6000Å thick oxide device used with the 500Å "thin oxide" device are also shown in Fig. 4.

In most integrated IGFET circuits, certain devices (e.g., a load device) may be best described as operating in a source-follower (grounded-drain) mode; i.e., the drain is held at a constant potential and the source voltage swings. Since the source-to-substrate voltage and thus the device threshold is not constant in this mode, the grounded-source curves of Fig. 1 can be used only by correcting for this effect. Thus it is convenient to present the device characteristics in the source-follower configuration as well. Such characteristics (also called load-device characteristics) are shown in Fig. 5 for given drain and substrate voltages.

The dynamic response of the circuit using IGFET devices is determined essentially by the device transcon-

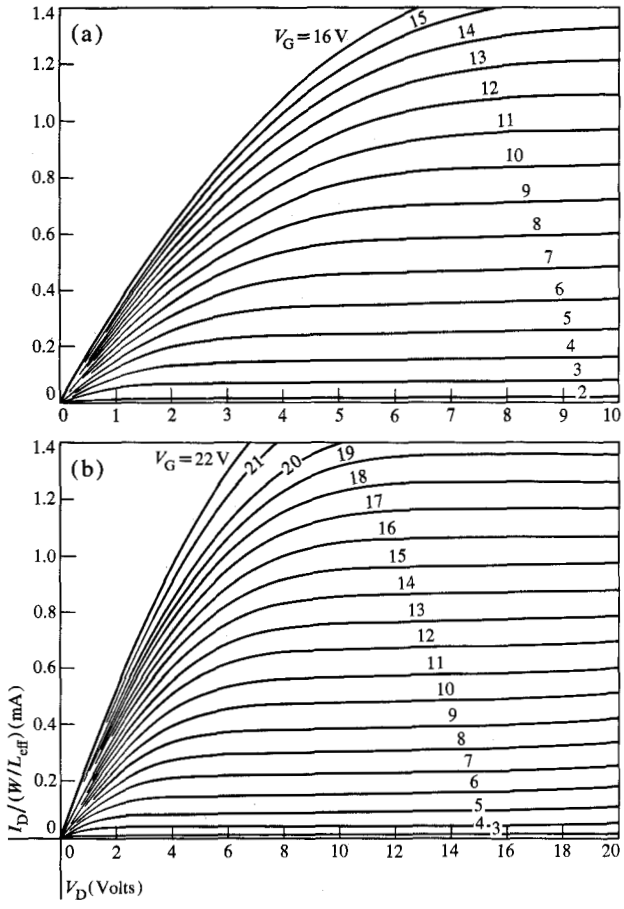


Figure 7 Normalized grounded-source characteristics. (a) 500Å device, $L = 0.35$ mil, $L_{eff} = 0.18$ mil ($R_D W/L_{eff} = 110\Omega$, $R_S W/L_{eff} = 75\Omega$); (b) 1000Å device, $L = 0.5$ mil, $L_{eff} = 0.29$ mil ($R_D W/L_{eff} = 400\Omega$, $R_S W/L_{eff} = 60\Omega$).

ductances and the node capacitances from devices and interconnections. There are no measurable storage delay effects in the speed range of interest (i.e., greater than 1 ns switching time). The pertinent device and interconnection capacitances are illustrated in Fig. 6. The gate of a device is coupled capacitively to the underlying source, drain, and channel regions, particularly in the area where the insulating oxide is thin. The equivalent circuit is complicated by the fact that the ac current path from the input gate terminal to the channel may be completed through either the substrate, source, or drain terminals (or more than one in parallel) depending on the channel conditions determined by the applied voltages. The source and drain diffusions have a capacitance to the substrate which can be evaluated from standard theory on diffused junctions if one takes care to include the sidewalls and lateral diffusion in determining the area of the junction of a narrow diffused line. These device and interconnection capacitances are not unique to the n-channel device and have been treated in the existing literature [7].

Device characteristics

In this section, a more detailed description of the device characteristics is presented. Considerable effort has been spent to characterize devices that are truly representative for the chosen processes and to present the data in a form accurate and complete enough to be used for detailed circuit design. In particular, the grounded source characteristics, the "turn-on" characteristics, effects of source-drain spacing, transconductance scaling with dimensions, and temperature effects will be covered in detail in this section. In addition, the more useful measurement and data analysis techniques are also described where pertinent.

To a first approximation, the FET characteristics can be normalized in the forms

$$I_D/(W/L_{eff}) = \gamma_m(V_{GS} - V_T - \tfrac{1}{2}V_{DS})V_{DS} \quad (1)$$

for $V_{GS} - V_T > V_{DS}$, and

$$I_D/(W/L_{eff}) = \tfrac{1}{2}\gamma_m(V_{GS} - V_T)^2 \quad (2)$$

for $V_{GS} - V_T < V_{DS}$,

where $\gamma_m = \mu_{eff}(\epsilon_0\epsilon_{ox}/t_{ox})$.

The normalized transconductance γ_m is a useful parameter which is, to a first approximation, a constant for a particular device process. (If γ_m were exactly constant, there would be no purpose in presenting experimental curves.) However, γ_m does vary somewhat since it contains the mobility term that generally decreases with increasing gate voltage. The mobility also decreases for short devices at high drain voltage because of saturation velocity effects. Furthermore, devices of short source-drain spacing have some additional loss in γ_m, particularly in the pinch-off region. The philosophy here is to present experimental curves for the lowest practical value of L_{eff}, such as would be used for the majority of devices, and to show in a later section how the characteristics behave for larger values of L_{eff}.

• *Grounded-source characteristics*

Grounded-source characteristics for the 500Å and the 1000Å devices are shown in Fig. 7. A general description of the nomenclature and behavior was given in Fig. 2. These devices have source-drain spacings equal to 0.35 and 0.50 mil, respectively, at the mask level (giving nominal values of effective source-drain spacing of 0.19 and 0.28 mil, as shown later), and both have a width W of 4 mil. The results are presented, however, in a normalized form by dividing the actual current scale by W/L_{eff} to give the characteristics of a device having

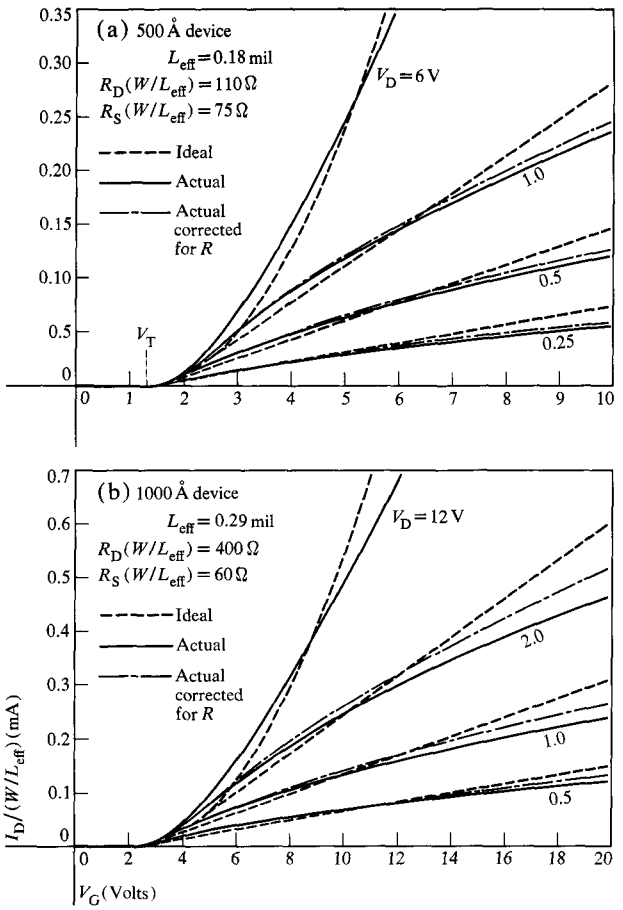


Figure 8 Experimental and idealized transfer characteristics.

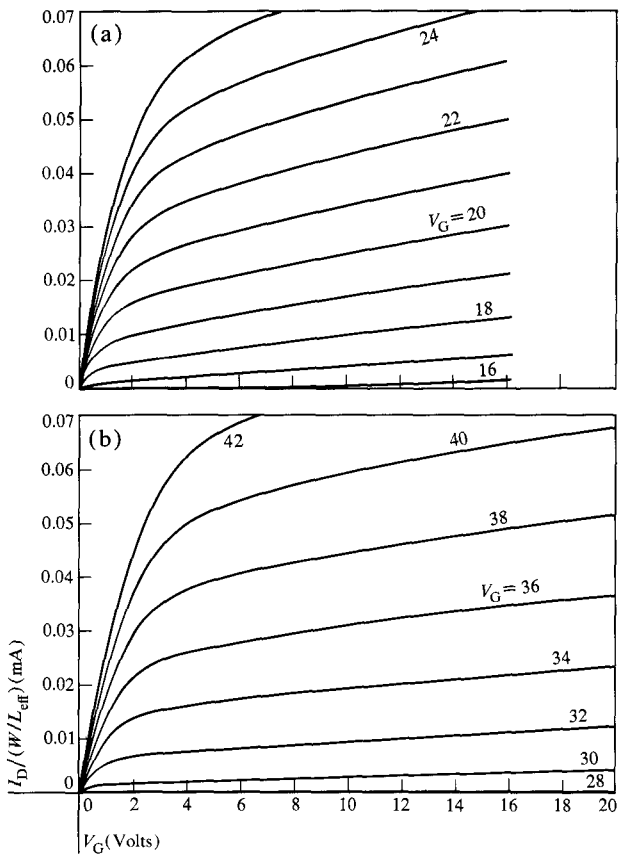


Figure 9 Characteristics of parasitic thick-oxide devices. (a) 6000Å, $L = 0.35$ mil ($L_{eff} = 0.19$ mil, $R_DW/L_{eff} = 800\Omega$, $R_SW/L_{eff} = 8k\Omega$); (b) 10,000Å, $L = 0.50$ mil ($L_{eff} = 0.29$ mil, $R_DW/L_{eff} = 350\Omega$, $R_SW/L_{eff} = 4.1k\Omega$).

$W/L_{eff} = 1$. Thus the curves can be used for general design purposes by multiplying the current scale by the actual W/L_{eff} being used.

The presence of resistances R_D and R_S in series with test devices (due mainly to the sheet resistance of the diffusion), causes an effective drop-off in transconductance at high currents, which produces a crowding of the I_D vs V_D characteristic curves for low drain voltage (below pinchoff). The characteristics above pinchoff are relatively unaffected because the current is independent of the drain voltage (and thus of the voltage dropped across the resistances); the only reduction in drain current is due to the decrease of the applied signal V_{GS} by the amount of the drop across R_S. Notice also that at high power levels (large drain and gate voltages) the power density in these relatively small devices is large enough to cause a temperature rise in the order of 10°C. This effect causes an approximately 5% loss in transconductance.

The transfer characteristics of Fig. 8 are another way of presenting the same data, giving I_D vs V_G for various fixed values of V_D. Corrected curves, removing the effect of R_D and R_S are also shown. If γ_m were constant, the upper portion of these curves (for $V_{GS} - V_T > V_{DS}$) should be a straight line intercepting the V_G axis at $V_G = V_T + (V_D/2)$, according to Eq. (1). Such idealized characteristics are shown for comparison, using the value of γ_m defined at a specification point ($V_D = 0.5$, $V_G - V_T = 5$ for the 500Å and $V_D = 1$, $V_G - V_T = 10$ for the 1000Å device). The amount of error introduced by such an approximation is quite reasonable for many purposes. It can be seen that the actual value of γ_m decreases monotonically with V_G, and it is greater than the specified value for low gate voltage and smaller than the specified value for high gate voltage.

The curves given for the largest value of drain voltage correspond to the pinchoff condition ($V_D > V_G - V_T$) and are compared to the idealized curve given by Eq. (2). In this case it appears that γ_m is dropping off more rapidly with V_G.

Characteristics for parasitic thick-oxide devices for both the 500 and 1000Å processes are given in Fig. 9 for the same device lengths considered above. These curves illustrate that such devices are in an "off" state

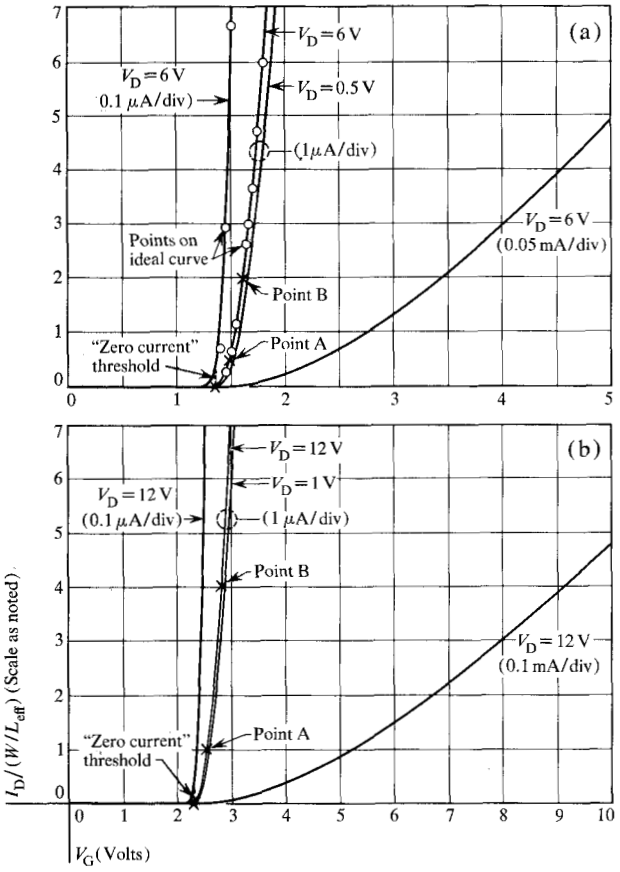


Figure 10 Turn-on characteristics for several current ranges and drain voltages. (a) 500Å device; (b) 1000Å device.

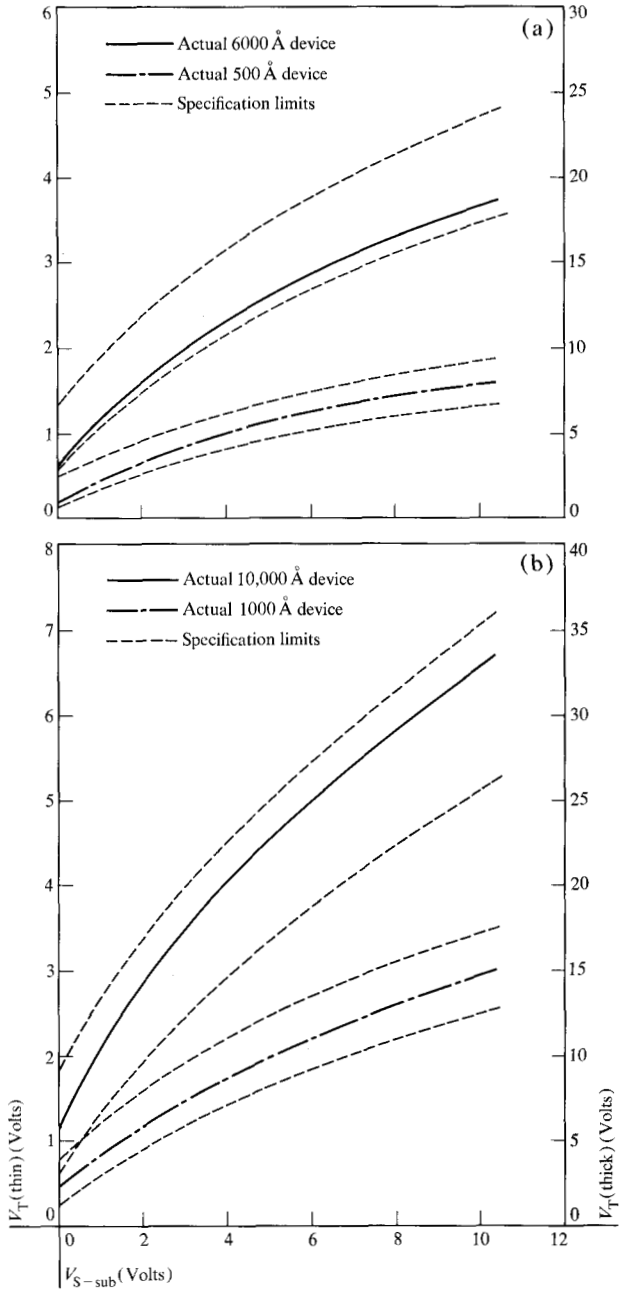


Figure 11 Measured threshold voltage vs source-to-substrate voltage (compared with initial specification limits) for the short-L devices characterized in the preceding figures.

when the applied gate voltage is below a certain level. These curves also show that the current above pinchoff ($V_D > V_G - V_T$) still increases somewhat with the applied drain voltage rather than remaining constant as required by Eq. (2). This increase is greater than that of the thin-oxide device for the same value of $V_G - V_T$ because the lower current level (proportional to $1/t_{ox}$) causes a wider space-charge region near the drain, which becomes appreciably large with respect to the channel length, and the resulting effective decrease in L with applied drain voltage is consistent with the increase in drain current.

• *Turn-on characteristic and definition of zero-current threshold*

Since leakage or "off" currents are very important for memory applications, it is necessary to carefully inspect the characteristics in the region of threshold. In Fig. 10 the transfer characteristic is compared with the calculated parabolic curve [Eq. (2)] at very low current levels. The transfer characteristic of the device is also shown with normal operating voltages for reference purposes. The major effect is that the device starts to turn on slightly below the "zero-current" threshold indicated by the parabola. This occurs because the current approaches zero in an exponential fashion, rather than as a parabola, as the gate voltage is reduced.

The definition of "zero-current" threshold needs some elaboration. Since the current decreases in an exponential fashion for very low values, as seen in Fig. 10, the definition of a true zero-current threshold is rather nebu-

lous. In addition, practical difficulties of instrumentation—especially when junction and surface leakage are present—make such a measurement impractical. The solution to this problem is to utilize the fact that the turn-on characteristic is parabolic over a considerable range of current. A parabola is fitted to the turn-on characteristic and extrapolated to "zero." The two points necessary to define the parabola are taken as $W/L_{\text{eff}} \times 1\mu\text{A}$ and $W/L_{\text{eff}} \times 4\mu\text{A}$ for the 1000Å device.

• *Threshold-substrate characteristics*

The measured threshold voltage as a function of substrate voltage is plotted in Fig. 11 for both the 500 and 1000Å devices and also for the corresponding parasitic thick-oxide devices. Typical design limits are also shown.

Measurements have been made of the transfer characteristics for different values of substrate voltage. These show that the transconductance, γ_m, does not vary significantly with substrate voltage.

• *Surface leakage and guard rings*

One of the problems with the n-channel device has been that of surface leakage. When the charge is high enough to invert the surface, as illustrated in Fig. 12, current flows from the n^+ diffusion to the inversion layer by normal IGFET-type conduction. The current can flow from the inversion layer to the substrate lead by several means:

1) The inversion layer itself has leakage directly to the substrate due to generation of carriers in the depletion layer. (This current is greatly increased by exposing the wafer to light.)
2) The inversion layer can be connected, at or near substrate potential, to other n^+ diffusions on the same substrate which serve essentially as source diffusions with the current flowing to the substrate via junction leakage. This can be significant when only one of a large number of junctions on a wafer is biased, leaving many junctions in parallel to pass leakage current from the inversion layer to the substrate.
3) Crystal defects and damage around the edge of the chips can also provide paths to the substrate.

The classical solution to this surface leakage problem is to surround the n^+ diffusion with a p^+ guard ring. Although effective, this is not desirable in low-cost memory because of the extra p^+ diffusion and the area required.

A different type of guard ring, where a biased n^+ diffusion is used, has been found to be useful for the n-channel IGFET. The structure is illustrated in Fig. 13. The principle of the n^+ guard ring action can be understood by considering the structure of an ungated IGFET

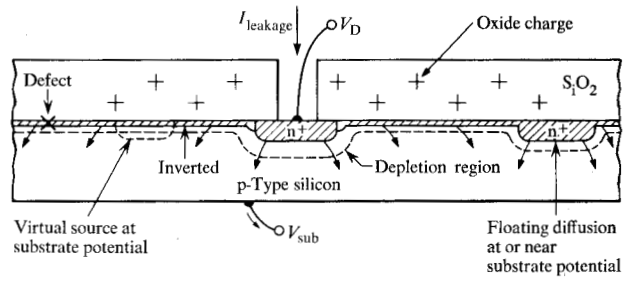


Figure 12 Illustration of surface leakage paths from a diffusion to the substrate through an inverted surface.

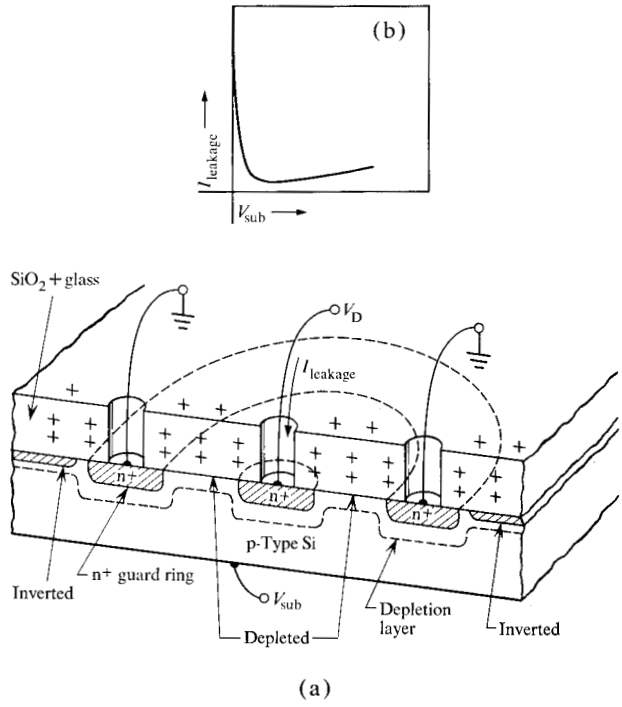
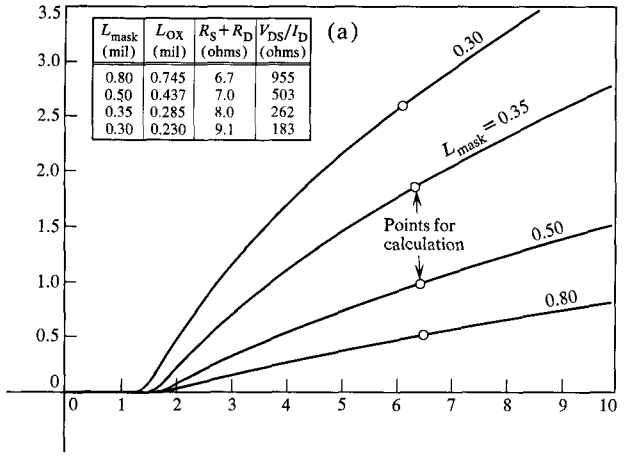


Figure 13 (a) Structure of guard ring using biased n^+ diffusion; (b) leakage current vs substrate voltage for a device with a large surface charge.

with the guard ring serving as a source and the guarded diffusion as a drain. Consider a case where the oxide charge is high enough that the region between the diffusions is inverted when no biases are applied to the structure. If a voltage is applied to the drain, and the source (guard ring) and substrate are grounded, an FET current can flow from drain to source. If a substrate bias is now applied to the device, the region between the diffusions can be depleted, the "threshold" of the device is raised and thus the leakage path is "turned off." This is identical to what happens when a substrate bias is used to turn off a normal IGFET device that was originally turned on. (As with the p^+ guard ring, the effect is to make the



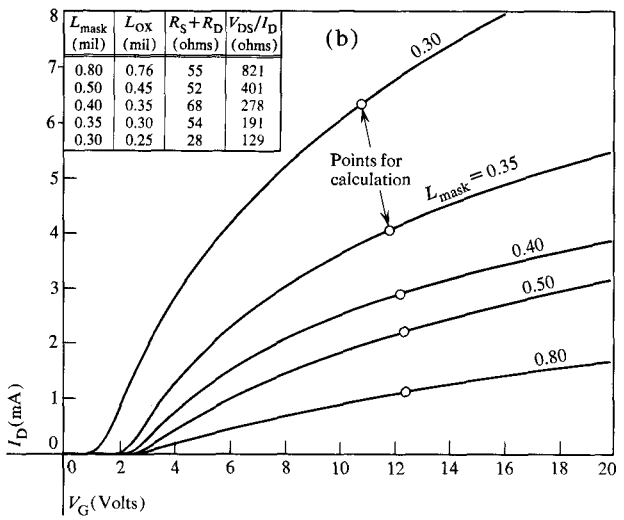


Figure 14 Transfer characteristics for various channel lengths ($W = 4$ mil). (a) 500Å devices, $V_D = 0.5$V; (b) 1000Å devices, $V_D = 1.0$V.

bulk voltage term of the threshold equation large, but in this case, $V_{S\text{-}sub}$ is modified rather than N_a.) A plot of leakage current vs substrate voltage for a device with a large surface charge is shown in Fig. 13(b). For zero substrate bias, the surface is inverted and large leakage current flows. As the substrate bias is increased, the leakage decreases to a minimum as the surface leakage disappears. As the substrate voltage is further increased, the leakage increases again because of increased junction leakage. Outside the guard ring, the surface is still inverted (if the charge is sufficiently large). In this area, the guard ring behaves as a drain while any other diffusion that is not deliberately tied to another potential will seek the substrate potential and act as a source.

In the case of a densely packed array each junction has only a very limited vacant area around it, except around the outside edge of the array. Further, each of the surrounding junctions is also biased above substrate potential (at ground or higher) thereby effectively serving as a guard ring. The net result is that special guard rings are needed only around the edge of the chip.

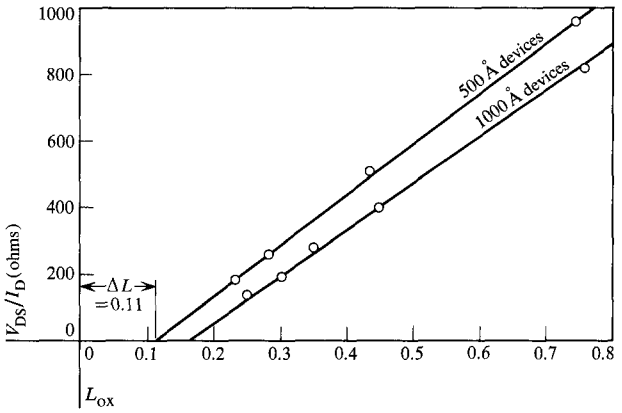


Figure 15 Experimental values from Fig. 14, plotted to allow determination of ΔL.

• *Effects of source-drain spacing*

Over a large range of channel lengths, the transconductance of a device scales approximately in proportion to W/L_{eff} and there are only secondary effects on device threshold and the shapes of the device characteristics. However, as the source and drain are brought into close proximity (about 0.1 to 0.2 mil) these secondary effects become important and place a practical limit on the minimum useful source-drain spacing. In this section, data are given that show the effect of source-drain spacing upon the transconductance, upon the shapes of the grounded source characteristics and upon the threshold voltages for both thick and thin gate oxides. Also, a method is illustrated for determining "ΔL" caused by lateral diffusion under the edges of the oxide diffusion mask.

Transconductance scaling and determination of lateral diffusion The most convenient method of evaluating the scaling of transconductance with channel length and determining the magnitude of the lateral diffusion is to use Eq. (1) to compare the "on resistance" of devices of various lengths below pinchoff. One must take into account the effects due to diffusion and contact resistances on source and drain resistances R_S and R_D. Also, since the effective mobility, μ_{eff}, is a function of the field in the gate oxide, one must be careful to use the same field in all cases. To do this, the gate voltage has been arbitrarily chosen to be 5V above threshold for the 500Å device and 10V above threshold for the 1000Å device. Also, standard V_D values of 0.5 and 1.0V, respectively, have been chosen for the two devices. The transfer characteristics of devices having several different lengths (all with $W = 4$ mils) are shown in Fig. 14, along with a table

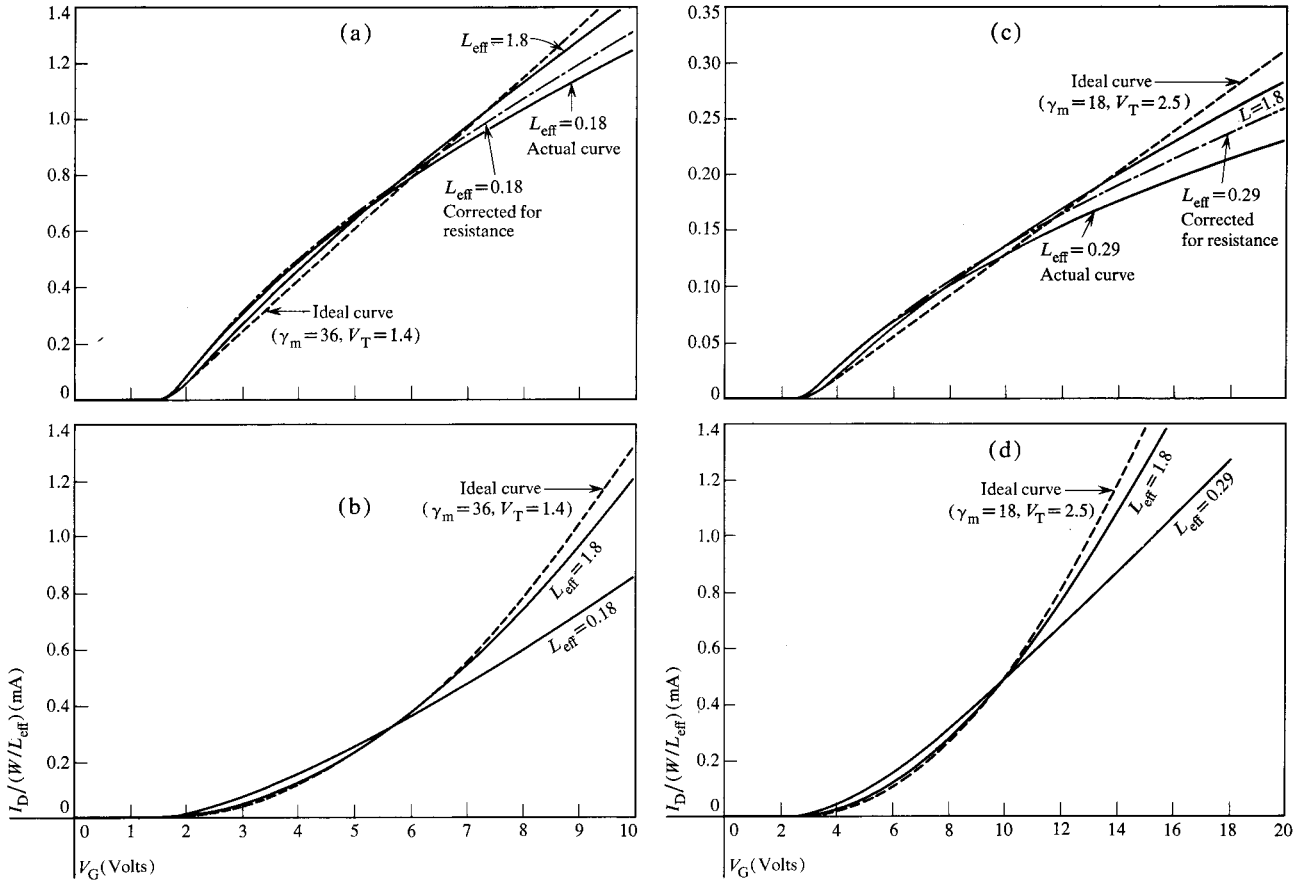


Figure 16 Normalized transfer characteristics above and below pinchoff for long and short channel lengths. (a) 500Å, $V_D = 0.5$V; (b) 500Å, $V_D = 10$V; (c) 1000Å, $V_D = 1.0$V; 1000Å, $V_D = 16$V.

showing the measured source-drain distance between the oxide openings for the diffusion, L_{ox}, the source and drain resistances and the calculated "on resistance," V_{DS}/I_D.

The "on resistance" is given to a good approximation by

$$\frac{V_{DS}}{I_D} = L_{eff}\left[\gamma_m W\left(V_G - V_T - \frac{V_D}{2}\right)\right]^{-1}, \tag{3}$$

where

$$V_{DS} = V_D - I_D(R_D + R_S). \tag{4}$$

If $R_D = R_S$, Eq. (3) is exact.

Lateral diffusion under the oxide causes the actual spacing between the source and drain diffusion, L_{eff}, to be less than the width between oxide openings, L_{ox}, by an amount ΔL. Thus,

$$V_{DS}/I_D = (L_{ox} - \Delta L)\left[\gamma_m W(V_G - V_T - \tfrac{1}{2}V_D)\right]^{-1}. \tag{5}$$

Since the quantity inside the square brackets is held constant in all the measurements given here, a plot of the experimental values of V_{DS}/I_D as a function of L_{ox} should be a straight line, intercepting the L_{ox} axis at ΔL.

The experimental values from Fig. 14 are plotted in this way in Fig. 15. The linearity of the plots indicates that γ_m can be considered constant (within experimental accuracy) over the range of L being considered. The values of ΔL are seen to be 0.11 mil for the 500Å device and 0.17 mil for the deeper diffusion of the 1000Å device. The two plots are also approximately parallel, as they should be, since the quantity in the brackets of Eq. (5) is the same, with γ_m being twice as much for the 500Å device while $(V_G - V_T - \frac{1}{2}V_D)$ has been held at half the value. Values of γ_m are 36μmhos/V and 18μmhos/V, respectively, for the 1000 and 500Å gate thicknesses.

The measured values of ΔL compare reasonably well with the measurements made by cross-sectioning and staining. The only significant difference is that the electrical measurement seems to give a value that is consistently a fraction of a micrometer less than the value obtained by staining. Thick-oxide devices have also been measured for each process, giving about the same or

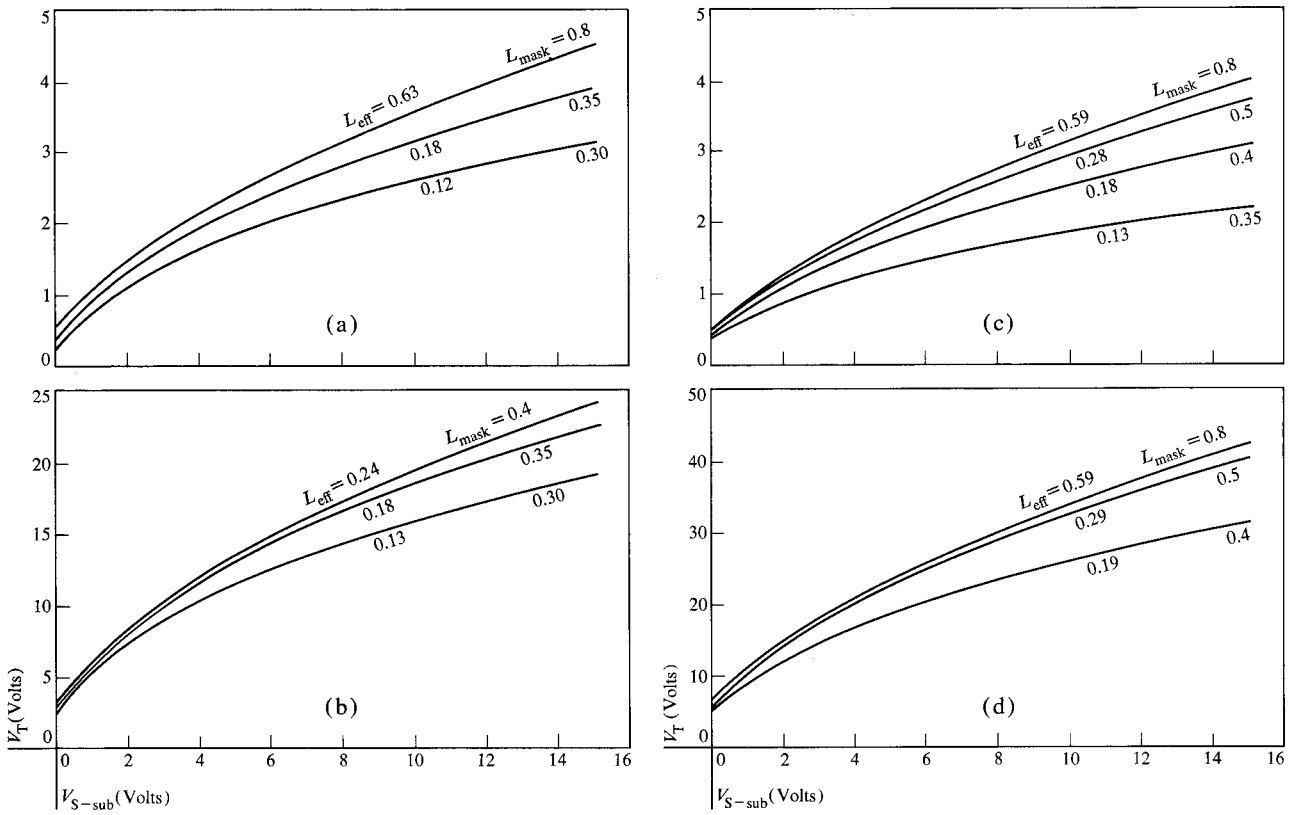


Figure 17 Threshold voltage vs source-to-substrate voltage for various channel lengths. (a) 500Å, $V_D = 6V$; (b) 6000Å, $V_D = 6V$; (c) 1000Å, $V_D = 12V$; (d) 10,000Å, $V_D = 12V$.

slightly higher values than those of the corresponding thin-oxide devices. This is reasonable since the value of ΔL measured in this way does not necessarily correspond exactly to a physical value.

Effect of L on characteristic curves Although it has been seen that the value of γ_m measured at the specification point is essentially independent of L over some range, discernable differences in characteristic curves for different values of L may be seen. The long-L device more closely approaches the "ideal" curves represented by the device equations with a constant value of γ_m. The characteristics of the shorter-L devices of Fig. 7 have positive slope above pinch-off, which is explained by an expansion of the width of the space-charge region at the drain diffusion (with increasing V_D) that is appreciably large in comparison with the channel length [8]. Also, the spacing of the curves in the pinchoff region is closer for the higher values of gate voltages than in the case of the long-L device. This last point can be clearly seen in the normalized transfer characteristics given in Fig. 16 which superimpose results for two different values of L. It can be said either that the device equations do not hold exactly for short-L devices or that the effective mobility, μ_{eff}, falls off more rapidly with V_G for the smaller-L devices, particularly in the pinchoff region. It should be noted that the characterization in pinchoff at high gate voltages corresponds to the maximum current density and power density and that both these factors are magnified in the short-L device. Some of the drop in transconductance is due to local heating of the device. Also, the drain voltage causes a horizontal field that is much higher in the short-L device; at high gate voltages, most of this drain voltage appears across the ohmic channel region and calculations show that electrons are approaching saturation velocity, causing a consequent drop in effective mobility [9].

Effect upon threshold voltage When the source-drain spacing is made very small, the device becomes harder to "turn off." This is manifested in two ways: 1) The substrate characteristic, illustrated in Fig. 17, becomes flatter and 2) the slope of the drain characteristic in pinchoff becomes larger, making the threshold sensitive to drain voltage. These effects are due to a merging of the depletion layer around the drain diffusion with that of

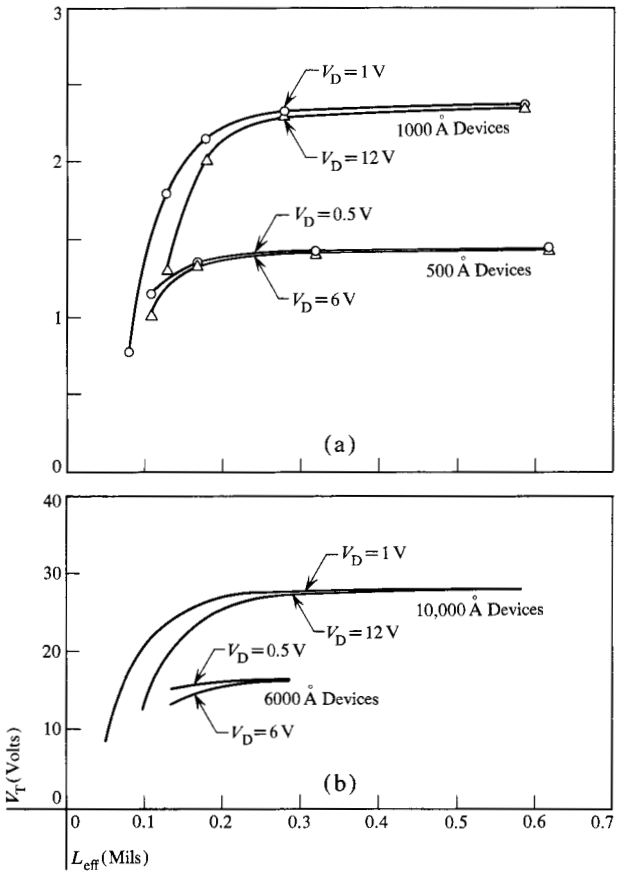


Figure 18 Threshold voltage vs effective source-to-drain spacing for different oxide thicknesses.

the source diffusion, giving a field in the channel region that aids the gate in turning on the device. The standard theory for threshold voltage is based on a one-dimensional analysis and fails in this case.

The experimentally determined threshold voltages at a fixed value of substrate voltage are plotted as a function of channel length for 500, 1000, 6000, and 10,000Å gate oxides in Fig. 18. The effect of source-drain voltage is also illustrated. It is seen that the effect is small for L_{eff} greater than about 0.15 mil for the 500Å process (both 500Å and 6000Å devices), while the 1000Å process behaves well only for L_{eff} greater than about 0.22. This threshold shift is the major factor in determining the minimum source-drain spacing. The effect is less for the 500Å process because the source and drain diffusions are shallower, giving a more favorable field pattern.

• *Temperature effects*

The effect of elevated temperature on the device characteristics is to decrease the mobility and also to slightly lower the threshold. (In addition, long-term drift of the threshold is enhanced; but we are concerned here only

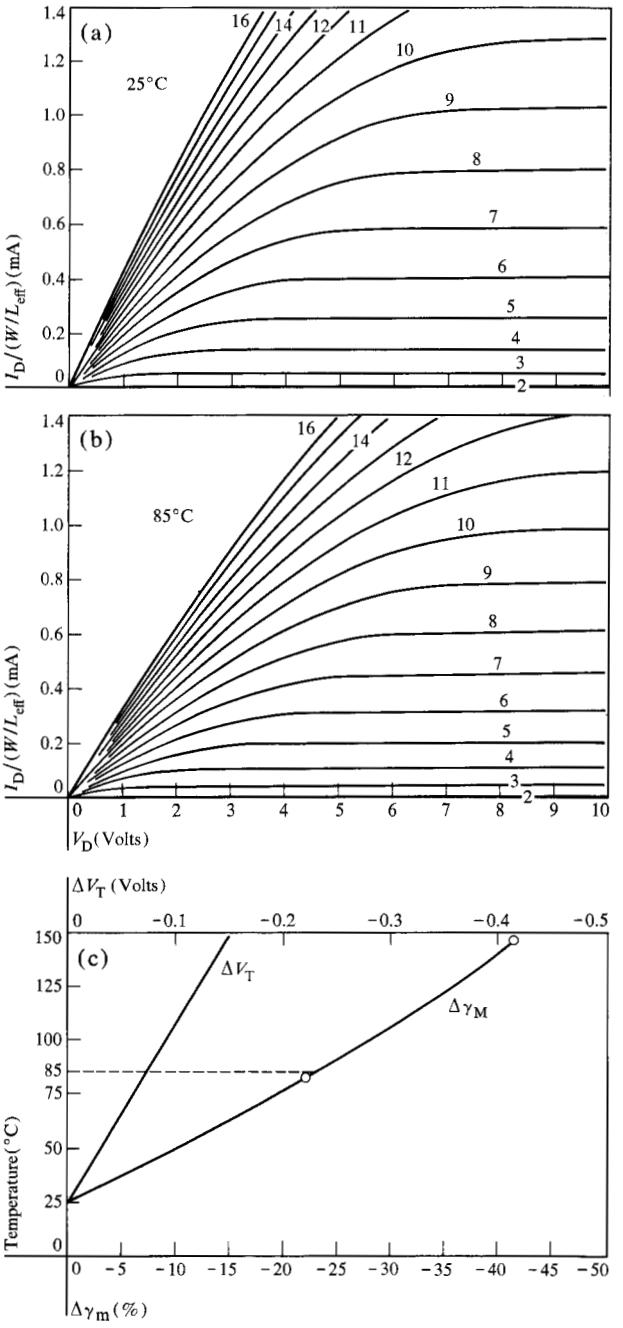


Figure 19 Temperature effects on device parameters for 500 Å device. (a) Grounded-source characteristics at 25°C; (b) grounded-source characteristics at 85°C; (c) threshold voltage and transconductance variations vs temperature.

Table 1 Change in threshold voltage with oxide thickness.

t_{ox}(Å)	ΔV_T @ 85°C relative to 25°C values
500	−0.07
1000	−0.1
6000	−0.3
10,000	−0.4

with immediate effects.) The effects are demonstrated in Fig. 19, where the measured change in transconductance γ_m and threshold ΔV_T is given as a function of temperature up to 150°C for a 500Å device. Measurements on devices of different gate oxide thicknesses give the same general result with γ_m dropping about 22% at 85°C. The value of ΔV_T is a function of oxide thickness as shown in Table 1.

Acknowledgments

Although this paper is devoted to IGFET device and chip design, which was the primary interest of the authors, much of the material is based on the work of others. In particular the contributions of a group headed by W. Liebmann at the IBM Boeblingen Laboratory (West Germany) and the following groups under the management of G. Cheroff are acknowledged: the chemistry group under P. Balk, the silicon planar technology group under E. Wurst, the planar device physics group under A. Fowler and the process control group under A. Brennemann. Particularly, the contributions of V. DiLonardo, C. Y. Duh, P. Evrenidis, F. F. Fang, C. Johnson, E. Peterson, E. Rocher, G. Schottky, J. Shepard, H. Statz, L. Terman and E. Walker, are acknowledged. Special thanks are also due to C. N. Edwards, who measured most of the device characteristics described in this paper.

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