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Digital-to-analog Converter having Common-mode Isolation and Differential Output

Abstract: A digital-to-analog converter (DAC) is described that has transformer-coupled isolation for both power and data inputs and provides a true differential output. The DAC provides a 10-bit, 10.23-V unipolar output of either polarity, depending on which of the two output lines is used as the load reference potential. The common-mode potential may be as large as 250 V, and below 120 Hz the common-mode rejection typically exceeds 100 dB. The isolated, balanced circuit eliminates environmental noise problems and permits long cabling lengths without loss of dc accuracy. The DAC is an analog output feature available on the IBM System/7, a small computer designed for data acquisition and real-time automation applications.

Introduction

Data acquisition systems commonly employ a differential input capability to reject common-mode signals and to maintain high signal accuracy in the presence of environmental noise and ground potential differences. Budzilovitch [1], Schmidt et al. [2], and Willard [3] have described general methods for characterizing and controlling the effects of environmental ground noise in industrial applications. Morrison [4,5] wrote on signal cabling and shielding practices and on the use of differential-input direct-coupled amplifiers for analog input signals. Emphasis has been placed on proper referencing of the signal source, on shielding and grounding, and upon the use of ground isolation in differential receivers to achieve rejection of common-mode signals.

General methods have also included the use of transformer-coupled power supplies and signal paths for ground isolation to improve the common-mode voltage capability over more conventional differential amplifiers such as those described by Morrison [4] and by Brown [6].

The same capability for common-mode voltage rejection is provided in an output digital-to-analog converter (DAC) in the subsystem to be described in this paper. Transformer coupling of both the input data and the power supply is combined with a completely balanced circuit configuration for the DAC to provide a true differential output with 250-V common-mode isolation capability. The DAC resistor network configuration to be described is similar to the binary-weighted ladder described both by Hoeschele [7] and by Schmid [8].

The digital-to-analog converter is provided as a feature on the IBM System/7, along with similarly isolated features for analog and digital input and digital output signals. The IBM System/7 is a small computer system designed with sensor input and output capability for data acquisition and real-time automation applications.

The common-mode voltage problem

The simplified equivalent circuit shown in Fig. 1 provides an understanding of the basic problem encountered in connecting a high-accuracy signal source V_s through a connecting cable, represented at low frequencies by series impedances Z_1 and Z_2, to a load impedance Z_L. If the signal source is active, i.e., if it can supply power, then it must have an input control and a power supply referenced through an internal impedance Z_i to a power supply ground reference potential. A conventional signal source provides a low-impedance direct connection, $Z_i << 1$ ohm, between the signal common lead and the power supply ground. In general, there is also an internal noise voltage V_i generated by the signal source power supply.

The load Z_L at the end of the connecting cable is also grounded or referenced through a ground impedance Z_g to a voltage differing by V_g from the signal-source power supply ground. A common-mode rejection factor, CMR, can be defined to describe the undesired voltage generated at the DAC output due to the ground voltage difference, $V_i + V_g$, occurring between the source and load ground potentials. In this simplified equivalent circuit a voltage $(V_i + V_g)/CMR$ is thus added to the signal source voltage V_S to complete the model for the total output voltage of the DAC. The voltage V_L appearing at the load end of the cable is found to be:

$$V_L = V_S G_1 + (V_i + V_g)\,[(G_1/CMR) + G_2]\,,$$

where

$$G_1 = Z_L(Z_2 + Z_i + Z_g)/[(Z_L + Z_s + Z_1)(Z_2 + Z_i + Z_g) + Z_2(Z_i + Z_g)] \text{ and}$$

$$G_2 = Z_2 Z_1/[Z_2(Z_i + Z_g) + (Z_s + Z_1 + Z_L)(Z_2 + Z_g + Z_i)]\,.$$

G_1 is the network attenuation from V_s to load voltage V_L, and G_2 is the network attenuation from the common mode voltages $V_i + V_g$ to the load voltage V_L.

If nothing can be done to control ground circuit terms V_g and Z_g, there is only one way to transfer the source voltage V_s accurately to the load V_L. The isolation impedance term Z_i must be increased to a very large value, thus decreasing the common-mode network attentuation G_2 to a value sufficiently small to accomplish the desired accuracy. Then the DAC must also provide a high common-mode rejection factor for both V_i and V_g noise sources. Of course, if the load impedance Z_L does not have to be ground referenced but can be floated instead on the cable ground lead, then an effective high ground impedance is created which may reduce gain G_2 to a negligible value. While this latter connection method is common, it severely restricts the application flexibility of a general-purpose digital-to-analog converter.

Requirements for an isolated DAC

Because of the ground noise problem that arises when a high accuracy analog signal source is directly connected to a remote grounded load, it was decided that it would be very desirable to provide a high isolating impedance Z_i in the design of a unipolar 10-bit digital-to-analog converter.

The isolation of the source voltage would greatly simplify installation, cabling, and application problems and would provide general utility to the analog signal source. The isolation would provide an accurate analog load voltage limited primarily by the cable attenuation term G_1, which could itself be made essentially unity for high-impedance loads Z_L.

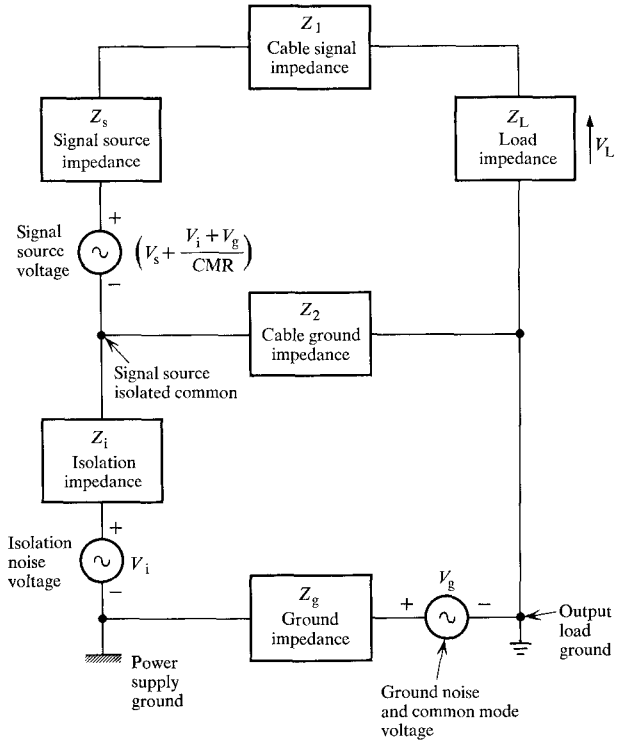


Figure 1 Simplified equivalent circuit of an isolated signal generator, connecting cable, and noise sources.

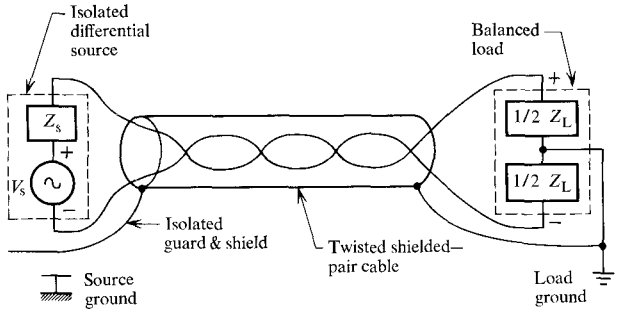


Figure 2 Simplified schematic of DAC showing use of isolated guard and shield for driving balanced load.

Another requirement undertaken in the design of the DAC was to provide a true differential output that could be used with either output lead grounded for obtaining the desired signal polarity from a unipolar design, or to drive a balanced load with a center-connected ground reference. A third isolated shield and guard lead would also be provided to further reduce cable noise sensitivity when using shielded twisted-pair cable, as shown in Fig. 2. Two different isolation impedances and noise sources could be identified on either side of the added shield line in Fig. 2, but the simplified diagram of Fig. 1 is sufficient

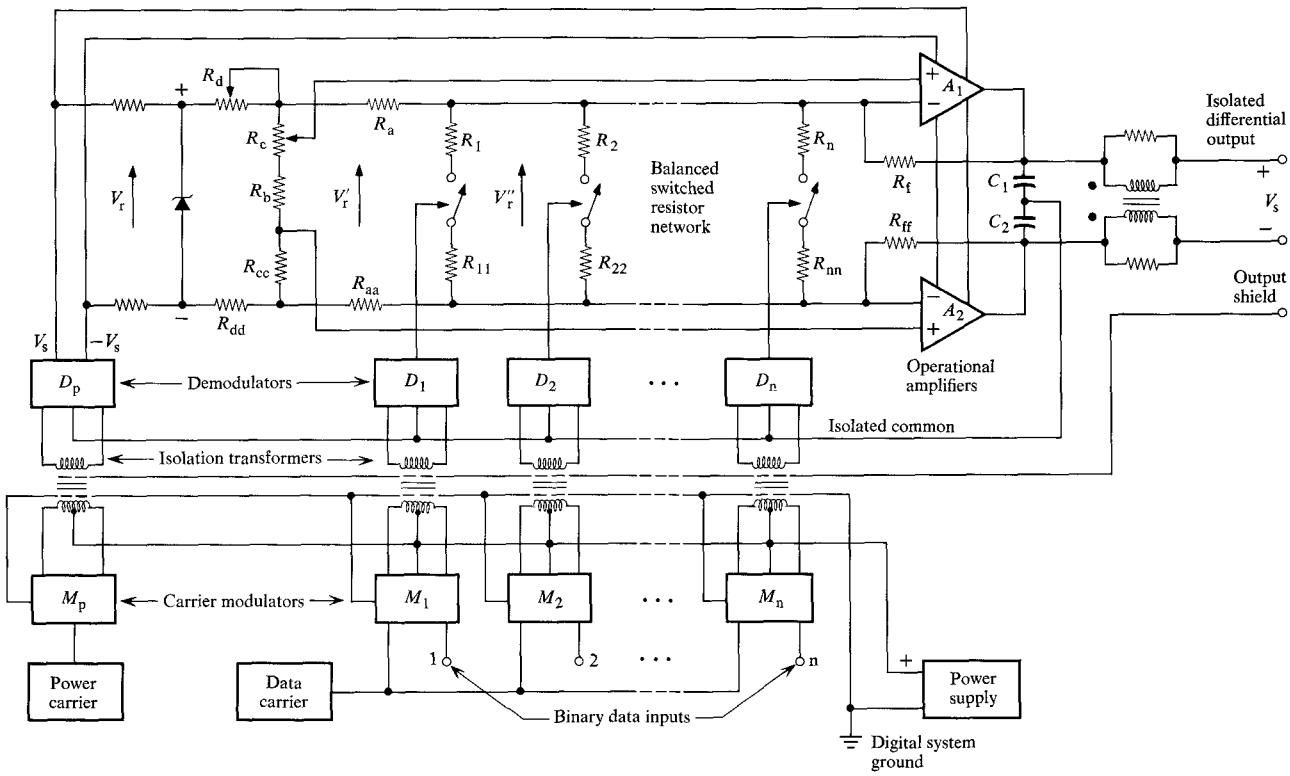


Figure 3 Schematic diagram of balanced and isolated digital-to-analog converter.

to describe the basic common-mode voltage and cabling problem. The isolation circuitry should have a relatively high speed to provide a 50 μsec settling time for a full-scale change.

The DAC circuit

The general circuit schematic of the DAC is shown in Fig. 3, with the nonisolated, binary data input signals connected at points 1, 2, $\cdots$, n, and the isolated analog voltage V_s appearing differentially at the output along with the shield line. The output signal is obtained from the difference in output voltages of two operational amplifiers, A_1 and A_2, connected in a balanced configuration. Feedback resistors R_f and R_{ff} convert the total current entering the negative input modes of the operational amplifiers into output voltages, the input currents being connected from reference potential V_r' through resistors R_a and R_{aa}. When all the analog switches connecting series pairs of binary weighted shunt resistors R_1, R_{11} through R_n, R_{nn} are open, the output voltage V_S is zero. Closing the switches causes the binary weighted precision resistors to shunt current away from feedback resistors R_f and R_{ff} so that the output voltage V_s increases in proportion to the total parallel resistance switched into the circuit.

The reference voltage V_r' is obtained from a reference zener diode and is manually calibrated for control of full-scale output voltage V_s by potentiometer R_D. The output offset voltage is manually adjusted to zero by potentiometer R_c controlling V_r''. The basic expression for the differential output voltage V_s is given by

$$V_s = V_r'' - V_r \frac{R_f + R_{ff}}{R_a + R_{aa}} + V_r''\left(1 + \sum_{j=1}^{n} \frac{R_f + R_{ff}}{R_j + R_{jj}}\right),$$

where the summation over j includes those resistors whose switches are conducting.

The control of each analog switch of the binary resistor network is obtained through amplitude detection of the ac output of a miniature high-frequency isolation transformer driven by a gated 1 MHz carrier, as shown in detail in Fig. 4. Care is taken to use shielded windings on the transformer to balance the primary drive, and to limit high frequency harmonics of the nonsinusoidal drive voltage. Conventional logic elements perform the carrier modulation, which generates a push-pull three-state input to the current-limited drive transistors T_6 and T_7.

The dc output of the rectified and filtered secondary controls a series-connected complementary pair of inverted, saturated switching transistors, T_n and T_{nn}. The

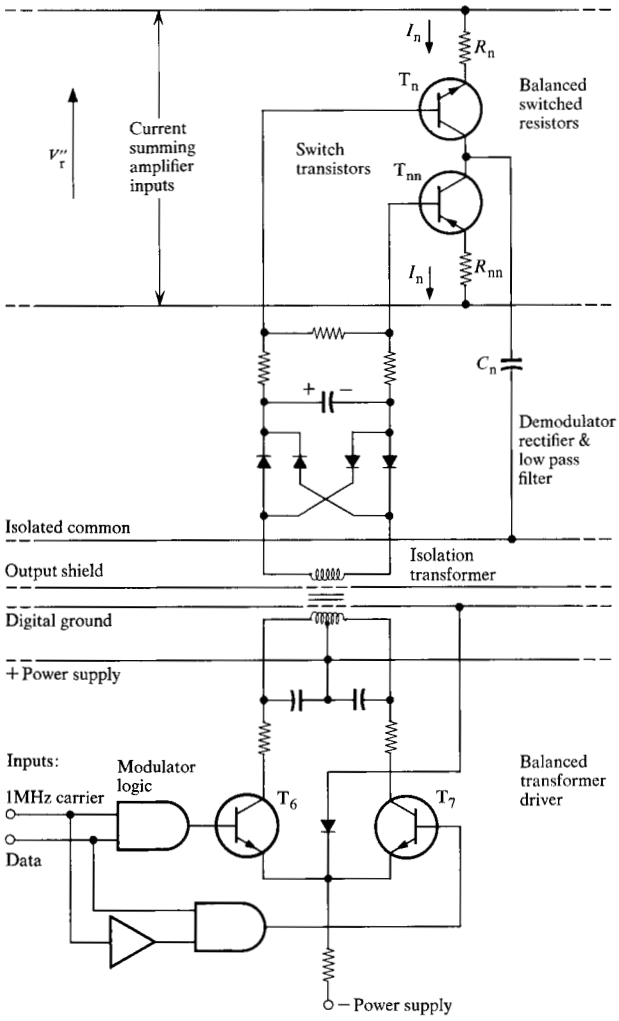


Figure 4 Diagram of one data modulator, isolator, demodulator, and switched resistor.

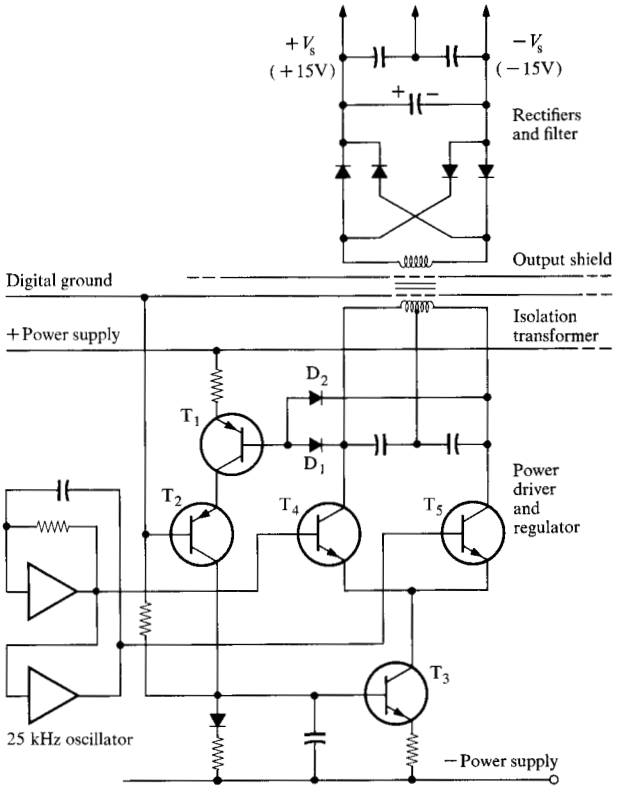


Figure 5 Power supply oscillator, regulator, isolator and rectifiers.

emitter-to-collector offset voltage of each transistor when saturated is less than a millivolt and the dynamic impedance is only a few ohms, thus making conventional bipolar transistors well suited for this application. It is necessary to couple isolated drive power to operate each analog switch, however, thus requiring separate isolation transformers for each bit for this type of configuration. The pair of switch transistors T_n and T_{nn} and the drive circuit are themselves isolated from the rest of the DAC circuit, so that the current flowing in the balanced network of each series pair of precision resistors R_n and R_{nn} is determined only by the sum of their resistances divided into the fixed voltage difference V_r'' existing between the amplifier input current summing lines. A small capacitor C_n provides a high-frequency noise bypass between the switch transistors and the isolated common line, the latter being the ground within the balanced DAC circuit.

The resistor shunting the bases of the switching transistors ensures rapid turn-off when the carrier is gated off. Both emitters become open-circuited, and the current in both resistors R_n and R_{nn} quickly drops to zero without having to charge capacitor C_n. Any common mode and carrier unbalance currents in the transformer interwinding capacitance of the isolation transformer are coupled to the isolated common line and not into either of the operational amplifier input lines.

The power supply oscillator, isolation transformer, and rectifiers (Fig. 5) supply the isolated power of about 1 W for the reference zener diode, the operational amplifiers, and the output signal power. This power oscillator operates with voltage regulation by diodes D_1 and D_2 which rectify the transformer primary ac voltage and drive a noninverted signal through the normally saturated collector of T_1. This signal couples through T_2 and is inverted by T_3 to adjust the emitter current source of the output drive transistors T_4 and T_5 as negative voltage feedback. If a low-impedance load or short circuit exists on the isolated dc secondary of the power supply, the primary ac voltage will no longer be large enough to sat-

Table 1 Summary of digital-to-analog converter specifications.

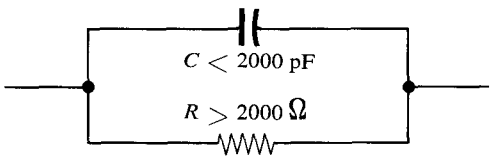
V_s, Output voltage:
0 to 10.23 V

Resolution:
0.010 V; 10 bits binary

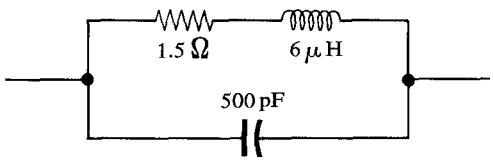
Accuracy:
$\pm$ 0.15%; $\pm$ .004% per degree C.

Settling time to $\pm$ 0.1% of full scale:
40 μsec (max.)

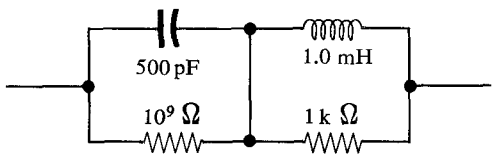
Z_L, Rated load impedance:



Z_s, Source impedance (see Fig. 1):



Z_i, Isolation impedance (see Fig. 1):



V_i, Common–mode isolation noise (see Fig. 1):

< 5 V peak-to-peak at 60 Hz.

< 0.05 V peak-to-peak at 30 kHz.

< 0.05 V peak-to-peak at 1 MHz.

V_g, Allowable external common–mode voltage:

< 250 V dc or peak ac, to 120 Hz.

Z_g, Allowable ground impedance:
any value

urate T_1, causing T_1 to invert the drive signal to T_2 and T_3 and thus reverse the feedback, (i.e., cause it to become positive). This causes the regulator to act as a feedback current limiter and prevents overheating of the drive transistors T_4 and T_5. When the load on the secondary returns to normal, the supply automatically recovers to its normal regulated output voltage.

The frequency of the oscillator does not need to be stable, so it is determined by a simple, single *RC* feedback network around conventional logic inverters. A similar oscillator is employed in the 1 MHz carrier generating circuit of the data modulator of Fig. 4.

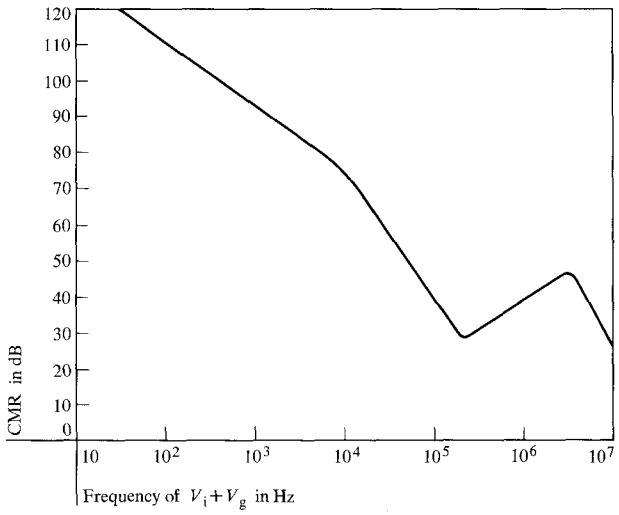


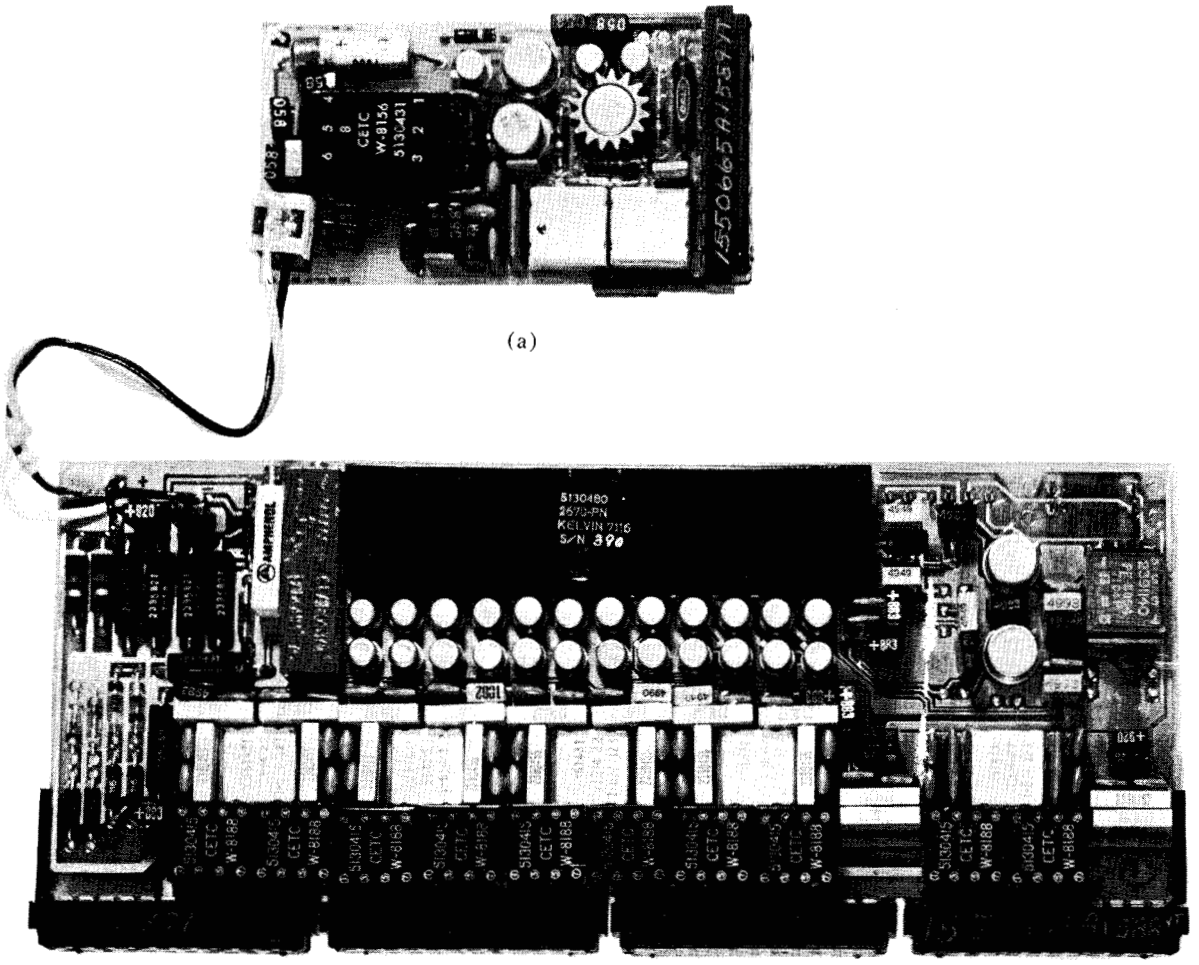
Figure 6 Typical plot of common-mode rejection factor, CMR, as a function of the frequency of $V_i + V_g$.

Performance characteristics of the DAC

The specific implementation of the isolated differential-output DAC which has been designed has a 10-bit resolution with 0.010 V per bit and 10.23 V full scale. It has a typical accuracy of $\pm$0.05%, or approximately one-half of one least-significant bit. It slews and settles to within $\pm$0.1% of the final output value typically in 25 μsec for a full-scale step and is faster for smaller steps. The accuracy of the above DAC is mainly dependent upon the accuracy of the reference voltage, the ladder and the "ON" resistance of the switches. The settling time term is dependent on the speed of the switches and on the amplifier slew rate.

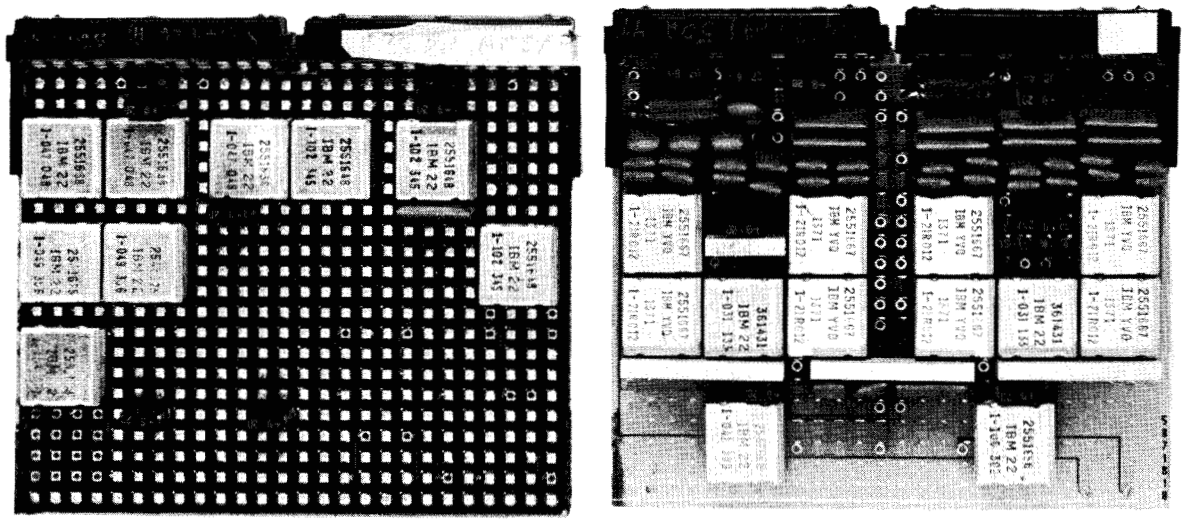
Table 1 summarizes these performance characteristics, the guaranteed specifications being relaxed by about a factor of two compared to typical performance. The isolation impedance Z_i is indicated typically as a 500 pF capacitance at low frequencies, resonating at about 200 kHz with a 1.0 mH series inductance from the damped balun in the output leads. The differential output impedance Z_s remains below 1.5 ohms until hitting a resonance at about 3 MHz, well above the response bandwidth.

The common-mode rejection factor, CMR, $(V_i + V_g/V_s)$ is shown in Fig. 6 to start typically at 120 dB at 60 Hz. It drops to a minimum of 30 dB at the 200 kHz resonance of Z_i, and it remains above 30 dB up to 10 MHz. The open circuit residual carrier noise in the isolation transformers, which results from winding un-



(a)

(b)



(c) (d)

Figure 7 The four circuit cards containing the DAC. (a) isolated power supply; (b) DAC analog circuitry with data isolation transformers; (c) data modulators; (d) input data registers and interface gates.

balances and stray capacitance, has two frequency components, as indicated in Table 1. When the common-mode rejection factor of Fig. 6 is applied at the carrier frequencies of 30 kHz and 1 MHz to these noise voltage components of V_i, only one or two mV peak-to-peak of carrier noise remain as normal mode in the DAC output voltage.

Extremely high speed performance for the DAC was not a design requirement since it is operated under program control of the IBM System/7. A further speed limitation in the binary-weighted resistor ladder results from the unequal turn-on and turn-off times of the transistor switches operating the ladder resistors. The unequal switch response times cause short-duration transients to appear as output signal transitions involving both the turning-on and turning-off of ladder resistors, especially those employed with the most-significant bits. Transients ranging from zero to about 6 V-μsec of area occur, depending on the change in bit pattern.

When very long cables are used with large capacitances loading the output, or when the DAC is used to operate an oscilloscope display, it is advantageous to add a properly selected series resistor and shunt capacitor to the load end of the cable. Such a load acts both as a low-pass filter and as a damping resistor to control the transient response of the DAC. Output overshoot and ringing can result from excessive capacitive loading, and from the transients occurring in this type of DAC at output transitions.

Figure 7 is a photograph of the four circuit cards on which one DAC is constructed, the cards having the format of standard digital logic cards and being packaged in a standard logic-card gate within the computer. No special shielding, grounding, or packaging was required because of the inherently good high-frequency isolation and rejection of logic circuit noise. The upper small card contains the power oscillator for the isolated power supply, while the middle large card contains the data coupling transformers and all the analog circuitry of the DAC itself. The two lower cards contain the logic interface registers and data carrier modulation circuitry.

Conclusions

The transformer-coupled, balanced digital-to-analog converter described here provides a true differential output. The performance at the load end of a cable is inherently independent of the type of cable and the load grounding configuration, including the use of unshielded twisted-pair wire and a grounded load. Very large potential differences between the IBM System/7 ground and the ground potential at the load can be accommodated without signal degradation or circuit overload. The complex cabling, shielding, and load grounding precautions normally required to connect precision dc analog voltages have been eliminated, providing for simple, error-proof installation.

The cost involved in providing this true differential output for a DAC is a tradeoff involving an increased level of circuit complexity, a reduction in installation cost, and the elimination of application restrictions with normal signal loads where a differential input is no longer required.

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