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Steady State Mathematical Theory for the Insulated Gate Field Effect Transistor

Abstract: A two-dimensional mathematical analysis is presented of the mechanisms of operation for an insulated gate field effect transistor (IGFET). Included in this analysis are qualitative and quantitative comparisons between conventional one-dimensional theory and a rigorous two-dimensional computer solution for the IGFET. It is shown that many characteristics of device operation deduced from conventional theory cannot be verified on a two-dimensional basis because of mechanisms not presently taken into consideration by the theory. A modified one-dimensional mathematical theory is therefore proposed, to account for these mechanisms, that is in adequate agreement with a rigorous two-dimensional computer solution for this semiconductor problem.

Introduction

In an early investigation of IGFET operation, Ihantola [1] and Ihantola and Moll [2] imply that electrical conduction in a source-drain channel is attributable to mechanisms similar to those proposed by Shockley in his theory of the unipolar transistor [3]. Briefly, it is implied that electrical conduction within the inversion layer of an IGFET is equivalent to electrical conduction within the channel of a junction field effect transistor (JFET). This concept of IGFET operation has prevailed throughout the technical literature, with little modification. The purpose of this paper is to show that, in contrast to the operation of a JFET, two-dimensional mechanisms contribute in a significant fashion to the operation of an IGFET. In addition, we propose a modified one-dimensional theory that adequately takes into account these two-dimensional mechanisms.

The two-dimensional mathematical methods used in this investigation are based upon a system of differential equations previously outlined by Van Roosbroeck in connection with his studies of hole and electron transport in a semiconductor [4]. Finite difference methods are used, with the aid of an electronic computer. This computational technique provides a means to accurately calculate the electrical and physical properties of numerous different IGFET structures throughout a large range of biasing conditions.

Nomenclature

D_n	diffusion constant for electrons
D_p	diffusion constant for holes
E_G	gate induced electric field
E_S	normal electric field at semiconductor surface of a one-dimensional structure
E_0	electric field at source end of IGFET inversion layer (parallel to the x-axis)
I_D	drain current in an IGFET
J_T	total electric current density
J_n	electric current density due to electrons
J_p	electric current density due to holes
L	channel length (distance between source and drain junctions)
L_C	channel length when $V_G < V_D$
L_l	channel length in an IGFET (effective)
N	net impurity atom density
N_A	acceptor impurity atom density
N_D	donor impurity atom density
Q_d	charge density (charges/cm^2) in gate induced depletion layer
Q_i	charge density (charges/cm^2) in gate induced inversion layer
Q_{i_0}	inversion charge at source end of IGFET
R_n	recombination rate for electrons
R_p	recombination rate for holes
T	temperature (absolute)

V_D drain voltage as measured with respect to charge neutral substrate material
V_G gate voltage as measured with respect to charge neutral substrate material
V_0 V_S at source end of IGFET inversion layer
V_S surface voltage as measured with respect to charge neutral substrate material
V_{SD} applied source-drain biasing voltage
V_{SG} applied source-gate biasing voltage
W width of IGFET
W_i width of insulator
k Boltzmann constant
n mobile electron density
n_i intrinsic carrier density
p mobile hole density
q electron charge
ϵ_0 permittivity of free space
κ dielectric constant
κ_S dielectric constant of semiconductor material
κ_i dielectric constant of insulating material
μ carrier mobility in the inversion layer of an IGFET
μ_n mobility for electrons
μ_p mobility for holes
ρ density of electrostatic charge
ϕ_F Fermi level
ϕ_{Fp} quasi-Fermi level for holes
ψ electrostatic potential
ψ_S electrostatic potential at semiconductor surface
ψ_0 electrostatic potential in charge neutral region of substrate

Computational methods

It has been shown [4] that the hole and electron distributions in semiconductor material are described by the equations:

$$\text{a)} \quad \text{div grad } \psi = \frac{-q}{\kappa\epsilon_0}(N - n + p)\,;$$

$$\text{b)} \quad \mathbf{J}_p = qD_p \text{ grad } p - q\mu_p p \text{ grad } \psi\,;$$

$$\text{c)} \quad \mathbf{J}_n = qD_n \text{ grad } n - q\mu_n n \text{ grad } \psi\,;$$

$$\text{d)} \quad \text{div } \mathbf{J}_p = qR_p\,;$$

$$\text{e)} \quad \text{div } \mathbf{J}_n = qR_n\,;$$

$$\text{f)} \quad \mathbf{J}_T = \mathbf{J}_p + \mathbf{J}_n\,, \qquad (1)$$

assuming no trapping mechanisms within the structure under consideration.

Equation (1a) is Poisson's equation, and it relates the divergence of the electric field ($\mathbf{E} = -\text{grad } \psi$) to the electrostatic charge distribution arising from both mobile charge carriers (holes p and electrons n) and immobile ionized impurity atoms N within the semiconductor lattice.

Equations (1b) and (1c) give the electric current distribution in a semiconductor arising from the transport of mobile holes and electrons. These equations express the dependency of each electric current component ($\mathbf{J}_p$ and $\mathbf{J}_n$) upon the concentration gradients of holes and electrons, the mobility of these charge carriers, and the electrostatic potential gradient (electric field) within the semiconductor material.

The present investigation is directed toward a study of physical mechanisms involved in IGFET operation, rather than a quantitative calculation of the electrical characteristics attributable to any particular semiconductor device. For this reason, a simplified view is taken concerning the mobility of carriers within the inversion layer of an IGFET. In particular, no consideration is given to scattering mechanisms that are known to be associated with the interface between a semiconductor and an insulator. Similarly, the mobility of these inversion layer carriers is assumed to be constant and independent of velocity. It is fully recognized that these assumptions represent only a crude approximation of the mechanisms actually encountered in IGFET operation. Nevertheless, a more accurate model for the carrier mobility in an inversion layer would complicate this problem of analysis without contributing significantly to the discussions presented here.

Equations (1d) and (1e), the continuity equations for holes and electrons in a semiconductor, are based upon an unspecified mechanism for carrier generation and recombination. For simplicity, the present analysis is based upon the assumption of an infinite minority carrier lifetime within the semiconductor material: $R_p = R_n = 0$. This simplification is presumed reasonable because the amount of recombination and generation encountered in modern silicon material has little influence upon important mechanisms contributing to the steady-state operation of an IGFET. Therefore, the manner in which IGFET operation is influenced by minority carrier recombination and generation is not considered here.

Equation (1f) states that the total electric current density $\mathbf{J}_T$ is a vector sum of the electric current densities due to holes $\mathbf{J}_p$ and electrons $\mathbf{J}_n$.

Finite difference methods are used to solve this system of equations for a mathematical model used to approximate an IGFET. In particular, the current equations (1b) and (1c) are transformed into differential equations for electrical flow lines within this semiconductor structure, and these flow line equations are numerically solved (in conjunction with Poisson's equation) for an array containing a minimum of 1200 spatial locations. The details of this computational technique will be presented in a later publication on this topic [5].

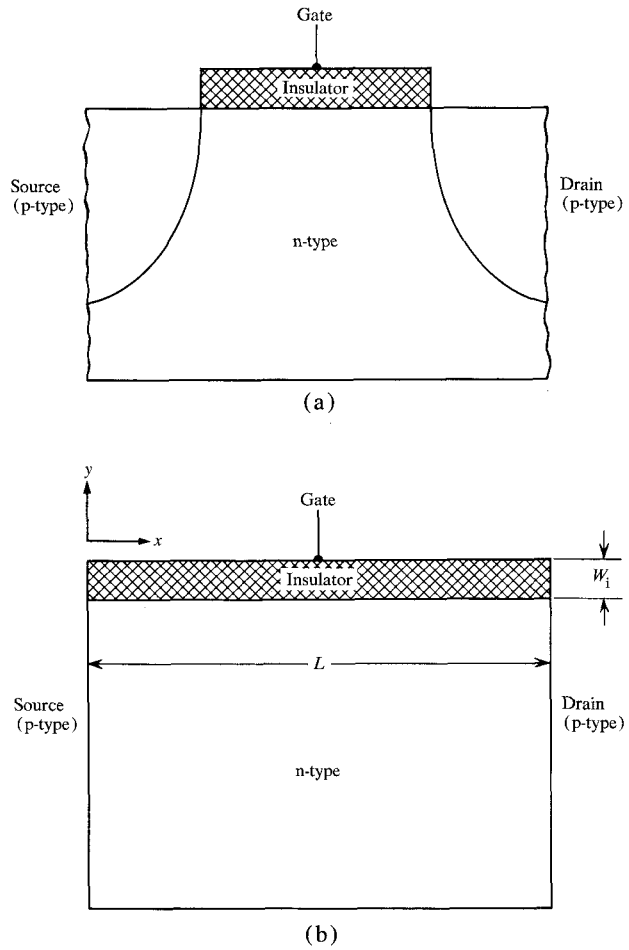


Figure 1 Analytical model for an IGFET: (a) representative geometry; (b) idealized.

Throughout this mathematical investigation particular emphasis is placed upon the selection of boundary conditions that introduce a minimum of error into the calculated results. The boundary conditions used in this analysis approximate the physical and electrical properties at the outer periphery of this semiconductor device, rather than at the internal boundaries established by those physical or electrical properties. A homogeneous impurity atom distribution is assumed within both the n-type and p-type semiconductor material. The exposed semiconductor surface is assumed to be an ideal electrical insulator; i.e., no electric current is permitted in a direction normal to these bounding surfaces. In all calculations of IGFET operation presented here, the ohmic contacts are located a sufficient distance from the active regions of the structure to have a negligible influence upon its electrical properties.

The computer calculations presented here are based upon an analytical model, Fig. 1(a), containing physical and geometrical properties representative of a typical IGFET. Source and drain region impurity atom densities of 10^{19} atoms/cm^3 (p-type) are assumed to form ideally abrupt p-n junctions in association with a substrate doping of 2×10^{15} atoms/cm^3 (n-type); when a different substrate doping is used it is so stated in the text. Most calculations are based upon a source to drain distance of 10.0 μm, although a limited number of calculations have been conducted for both longer and shorter channel lengths. It is assumed that an insulating layer of SiO_2 exists between the semiconductor surface and the gate electrode ($W_i = 1000$ Å). Rather than a model of the source and drain junction shapes shown in Fig. 1(a), the simplified rectangular model shown in Fig. 1(b) has been used to approximate an IGFET. The geometric differences between the two models shown in Fig. 1 are unlikely to have a significant influence upon the conclusions derived from this investigation.

Conventional theory of IGFET operation

Conventional IGFET theory is based upon an early treatment by Ihantola and Moll [2], the main elements of which are as follows: Gauss' law assures the continuity of gate induced electric field with the total space-charge at a semiconductor and insulator interface:

$$\frac{\kappa_i \epsilon_0}{W_i} (V_G - V_S) = Q_d + Q_i, \tag{2}$$

assuming for simplicity of discussion that no surface state charges are present. It has been shown [6] that the inversion charge Q_i in an IGFET resides within a very thin layer along the silicon and insulator boundary; therefore, from the depletion layer theory for a p-n junction Q_d can be approximated by [7]

$$Q_d = (2\kappa_s \epsilon_0 N_D q V_S)^{\frac{1}{2}} \tag{3}$$

and, from Eqs. (2) and (3), the inversion charge in an IGFET can be approximated by

$$Q_i(V_S) = \left[\frac{\kappa_i \epsilon_0}{W_i} (V_G - V_S) - (2\kappa_s \epsilon_0 N_D q V_S)^{\frac{1}{2}}\right]. \tag{4}$$

It is generally assumed that the source-drain electric current in an IGFET is attributable to drift mechanisms alone [8]:

$$I_D = \mu W Q_i(V_S) \frac{dV_S}{dx}, \tag{5}$$

where the inversion charge $Q_i(V_S)$ is given by Eq. (4) and μ represents the carrier mobility within this inversion layer. Because the source-drain electric current must exhibit continuity (i.e., must exhibit spatial independence), an expression for the volt-ampere characteristic of an IGFET is obtained by intergrating Eq. (5):

$$I_D \int_0^L dx = \mu W \int_0^{V_D} Q_i(V_S) dV_S . \tag{6}$$

There are physical mechanisms implied by this treatment that should be considered. For example, the electric current in Eq. (5) maintains continuity only when the surface potential V_S and the inversion charge Q_i satisfy the equality

$$\frac{d^2V_S}{dx^2} = -\frac{1}{Q_i}\frac{dQ_i}{dV_S}\left(\frac{dV_S}{dx}\right)^2 . \tag{7}$$

Equation (7) could be viewed in two different ways: First, this expression could be viewed as a *one-dimensional* Poisson equation with an electrostatic charge distribution biven by

$$\rho(x) = \frac{\kappa_s \epsilon_0}{Q_i}\frac{dQ_i}{dV_S}\left(\frac{dV_S}{dx}\right)^2 , \tag{8}$$

or, second, it could be viewed as the x-axis component of a *two-dimensional* potential distribution within the channel where

$$\frac{\partial^2\psi}{\partial x^2} + \frac{\partial^2\psi}{\partial y^2} \approx 0 . \tag{9}$$

It is recognized that the two-dimensional potential distribution in an inversion layer must be rigorously described by Poisson's equation, which takes into account electrostatic charges residing within this region of the structure. As in any solution of Poisson's equation, the complete solution is composed of two parts: a solution for an inhomogeneous part of the differential equation and the solution for a homogeneous part (Laplace's equation). The physics of IGFET operation show that the inhomogeneous part of Poisson's equation yields an electric field component directed substantially normal to the insulator and semiconductor interface; this component contributes little to the source-drain electric current. Similarly, the homogeneous part of this differential equation also yields an electric field component directed substantially normal to the insulator and semiconductor interface; this electric field component is attributable to uncompensated silicon ions residing within the gate induced depletion layer. Both these sources of electric field are neglected in Eq. (9). Instead, Eq. (9) describes that component of the potential distribution within a channel which arises from an applied source-drain voltage, and therefore represents the principal reason for a drain current in IGFET operation.

The derivation of Eq. (4) is based upon an assumption that the electric field produced by substantially all inversion charges is directed perpendicular to the semiconductor-insulator interface; therefore, substantially no inversion layer charges are available to modify the electric field parallel to this interface. For this reason, the first interpretation of Eq. (7) is not applicable to a one-dimensional treatment of the IGFET. Also implied by this treatment is that the inversion layer must be viewed as a two-dimensional electrical conductor of essentially constant conductivity. Any significant variation of channel conductivity would (from Gauss' law) require the availability of electrostatic charges within the channel to produce a significant variation of electric field parallel to the x-axis of this structure. Therefore, Eq. (7) must be viewed as the x-axis component of a two-dimensional potential distribution that satisfies Laplace's equation, Eq. (9); this is equivalent to Shockley's gradual channel approximation [3] for a junction field effect transistor. (Any change in electrical conductance between the source and drain must, according to the present one-dimensional theory, arise predominantly from a change in physical dimensions, rather than from a change in mobile carrier density, within the inversion layer of an IGFET.)

The adequacy of this approximation method is placed in question through a one-dimensional solution of Poisson's equation in a direction perpendicular to the semiconductor-insulator interface,

$$\frac{d^2\psi}{dy^2} = -\frac{q}{\kappa_s \epsilon_0}(N_D - N_A + p - n) . \tag{10}$$

Assuming the applicability of Boltzmann statistics,

$$\text{a)} \qquad p = n_i \exp\left[-\frac{q}{kT}(\psi - \phi_{Fp})\right];$$

$$\text{b)} \qquad n = n_i \exp\left[\frac{q}{kT}(\psi - \phi_F)\right], \tag{11}$$

we obtain from Eq. (10),

$$\frac{d^2\psi}{dx^2} = -\frac{q}{\kappa_s \epsilon_0}\left\{N_D + n_i \exp\left[-\frac{q}{kT}(\psi - \phi_{Fp})\right] - n_i \exp\left[\frac{q}{kT}(\psi - \phi_F)\right]\right\}, \tag{12}$$

when the substrate material is n-type.

Equation (12) can be integrated once between the charge neutral substrate material and the semiconductor-insulator interface yielding

$$\frac{1}{2}E_S^2 = \frac{q}{\kappa_s \epsilon_0}\left\{N_D(\psi_S - \psi_0) + \frac{kT}{q} n_i \exp\left[-\frac{q}{kT}(\psi_S - \phi_{Fp})\right]\right\} \tag{13}$$

and, therefore, the hole density p_S at this interface is adequately approximated by

$$p_S = \frac{q}{kT}\left(\frac{\kappa_s \epsilon_0}{2q} E_S^2 - N_D V_S\right). \tag{14}$$

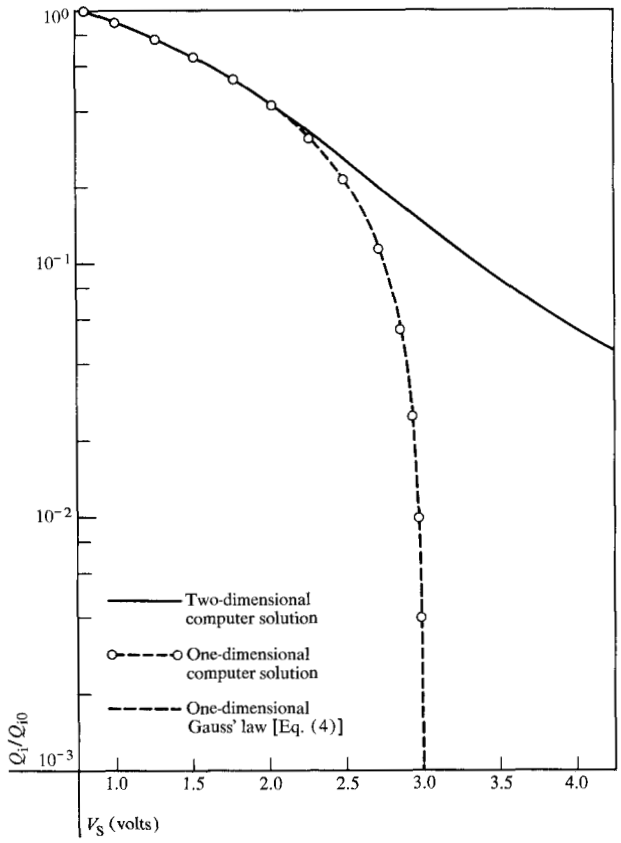


Figure 2 Calculated inversion charge Q_i in an IGFET.

Equation (14) shows that the assumption of essentially constant channel conductivity (which is implied by conventional IGFET theory) is inconsistent with a one-dimensional solution of Poisson's equation. From Eq. (14), inversion layer carriers located at the semiconductor-insulator boundary exhibit a change of density that is proportional to both V_S and E_S^2. As a consequence, any variation of Q_i between the source and the drain of an IGFET must be viewed as a density variation of inversion layer carriers; Gauss' law therefore requires that some carriers must exist within this inversion layer without contributing to the gate induced electric field. An additional implication arising from this density variation is that thermal diffusion must also be taken into consideration in any rigorous calculation of the source-drain current.

A computational experiment was used to verify that Eq. (4) does not adequately describe the inversion charge distribution in an IGFET. This computational experiment consisted of calculating $Q_i(V_S)$ for an IGFET under two different biasing conditions. For the first calculation of $Q_i(V_S)$ conventional biasing conditions were assumed upon the drain and gate: $V_D = 6.3V$, $V_G = 4.3V$. For the second calculation an electrical connection was assumed between the source and drain regions, and a substrate bias was introduced into the mathematical model; this reduces the model to a one-dimensional structure.

From Fig. 2, the one-dimensional computer calculation of $Q_i(V_S)$ is in substantial agreement with Eq. (4) but, in contrast, significant differences exist between Eq. (4) and the two-dimensional calculation of $Q_i(V_S)$. In particular, Eq. (4) agrees with this two-dimensional calculation only in the vicinity of the source junction (where V_S is small). Furthermore, it is shown (Fig. 2) that Eq. (4) predicts a channel pinch-off mechanism in the region where $V_S \approx 3.0V$; the two-dimensional calculation shows no indication of pinch-off at that location. It should be noted that a careful examination of these computer calculations shows that a two-dimensional IGFET can depart from Eq. (4) and, at the same time, continue to satisfy Gauss' law: The gate-induced electric field determines the constant total electrostatic charge Q_T in the semiconductor material.

Two-dimensional mechanisms in IGFET operation

The inadequacy of a one-dimensional model for IGFET operation arises from two different two-dimensional mechanisms encountered in this structure. The first mechanism provides a means whereby the one-dimensional form of Gauss' law can (with good approximation) establish the inversion charge distribution and, simultaneously, maintain the continuity of the drain current I_D. This situation is observed near the source junction of an IGFET (Fig. 2). The second mechanism provides a means whereby the inversion charge distribution can differ significantly from Eq. (4) but, simultaneously, satisfy both the requirements for electric current continuity and the requirements imposed by Gauss' law.

The one-dimensional form of Gauss' law, Eq. (4), implies that all electrostatic charges within the inversion layer of an IGFET produce an electric field component directed parallel to the y-axis of coordinates (Fig. 1); this implication is only partially correct. A more rigorous derivation of this equation, which assumes Eq. (4) represents a one-dimensional approximation for an essentially two-dimensional situation, shows that regions of an inversion layer which appear to satisfy Eq. (4) can contain a small number of electrostatic charges not predicted by this equation. Further, from Gauss' law, any variation of inversion charge density between source and drain requires that a prescribed number of charges within this inversion layer contribute to an electric field component directed parallel to the semiconductor surface. Throughout regions of an IGFET where the spatial variations of Q_i are small, the number of charges contributing to this x-axis component of electric field is small, when com-

pared to Q_i. For this reason, although the inversion charge distribution throughout regions of an IGFET may appear to satisfy Eq. (4), there resides within those regions a small number of mobile charges that are not associated with the gate-induced electric field. This small number of charges produces the electric field distribution required to maintain electric current continuity between the source and drain. From our two-dimensional computer calculations, the magnitude and distribution of charges in the inversion layer not given by Eq. (4) have been estimated from calculations of the electric field divergence parallel to the x-axis.

In contrast, a second two-dimensional mechanism exists in IGFET operation for which the inversion charges produced by the gate-induced electric field are not given by Eq. (4). Poisson's equation for the gate and drain depletion regions of this structure has the form

$$\frac{\partial^2\psi}{\partial x^2}+\frac{\partial^2\psi}{\partial y^2}=\frac{-qN_D}{\kappa_s\epsilon_0}, \tag{15}$$

where the x-axis and y-axis are taken to be parallel and perpendicular to the semiconductor-insulator interface, respectively. Because the gate electrode and the drain junction are geometrically perpendicular, a region exists within the depletion layers in an IGFET where ionized impurity atoms must be shared. Ions that are electrostatically associated with the drain junction do not contribute to the gate depletion charge. Similarly, ions that are electrostatically associated with the gate electrode do not contribute to the drain space-charge layer. For this reason, the substrate doping N_D in Eq. (4) cannot be considered a constant; the magnitude and distribution of N_D in this equation represents only those substrate ions available for the gate-induced space-charge layer.

This interaction mechanism between the gate and drain produces a situation for which the depletion charge (Q_d in Eq. 3) cannot be easily defined for a given surface voltage V_S. The voltage supported by this depletion region is determined by both the quantity and distribution of uncompensated impurity atoms *available* for the gate depletion region (from Poisson's equation) and, therefore, drain junction interaction provides a means whereby the surface inversion charge Q_i can assume a wide range of values for a given surface voltage V_S. For this reason, it is suggested that Eq. (4) approximates the mechanisms encountered in the operation of an IGFET only in the vicinity of the source junction (where drain interaction is a minimum).

Further evidence of this mechanism is observed in two-dimensional computer calculations of the electric field distribution within the gate induced depletion layer of an IGFET. In two spatial dimensions, a region of interaction between the gate and drain depletion layers can be determined from the direction and magnitude of the space-charge electric field. Regions of space-charge interaction between the gate and drain exhibit two electric field components: one parallel and one perpendicular to the oxide-semiconductor interface. The electric field component parallel to this interface is attributable to the drain junction and the perpendicular component is attributable to the gate electrode. There is no quantitative way to establish the drain junction depletion layer edge in this region of interaction, although from our two-dimensional IGFET computations this depletion layer edge has been established in a qualitative fashion. Figure 3 shows calculated contours of constant electric field arising from the drain junction in an IGFET.

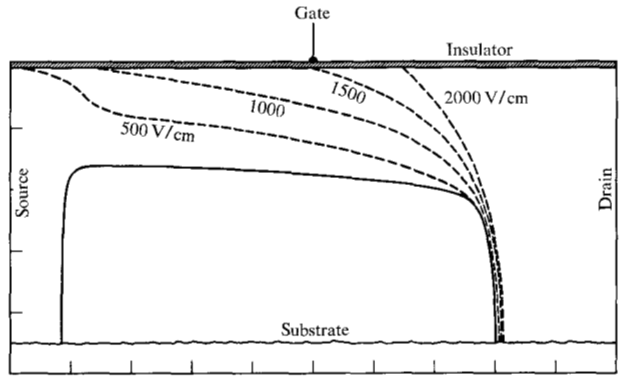


Figure 3 Calculated contours of constant electric field component produced by drain junction penetration in a 10-μm IGFET.

These two-dimensional mechanisms provide a means whereby electric current continuity can be attained between the source and drain of an IGFET. In the vicinity of a source junction (where gate-drain interaction is minimal) the inversion layer charge distribution $Q_i(V_S)$ is approximated by a one-dimensional application of Gauss' law, Eq. (4). In this region of the structure a small quantity of mobile carriers can become electrostatically dissociated from the gate electrode and produce the electric field distribution necessary to maintain electric current continuity. In contrast, near the drain junction there is significant two-dimensional interaction between the gate and drain; this interaction produces an inversion charge distribution $Q_i(V_S)$ that is poorly approximated by Eq. (4) (see Fig. 2). Many factors contribute to the location of the region in which the inversion charge distribution exhibits a transition between these two influencing factors (channel length, drain biasing voltage, substrate doping, etc.).

This rigorous calculation of ion sharing between the gate and drain (Fig. 3) was made using a two-dimensional model of an IGFET. A good approximation for the influence of these two-dimensional mechanisms can be accounted for by a simplified one-dimensional analysis of

this situation. In this method of analysis, which is described in the next section, we recognize that Eq. (4) represents a poor approximation for the inversion charge distribution $Q_i(V_S)$ in an IGFET, and that the maintenance of electric current continuity represents a more fundamental constraint upon this distribution. It will be shown that the previously described two-dimensional mechanisms encountered in IGFET operation provide the necessary degree of freedom for the magnitude and distribution of inversion charges to attain electric current continuity between the source and drain.

Electrical conduction in the inversion layer of an IGFET

In the inversion layer of an IGFET the source-drain electric current is assumed to result from both drift and diffusion,

$$I_D = W\mu\left(Q_i\frac{dV_S}{dx} - \frac{kT}{q}\frac{dQ_i}{dx}\right). \tag{16}$$

Therefore, electric current continuity between the source and drain is assured only if Eq. (16) satisfies the relation

$$0 = \frac{\partial I_D}{\partial x} = Q_i\frac{d^2V_S}{dx^2} + \frac{dQ_i}{dV_S}\left(\frac{dV_S}{dx}\right)^2 - \frac{kT}{q}\frac{d^2Q_i}{dx^2}. \tag{17}$$

Equation (17) can be rewritten into a more convenient form by introducing the substitutions

$$\text{a)}\quad \frac{dQ_i}{dx} = \frac{dQ_i}{dV_S}\frac{dV_S}{dx};$$

$$\text{b)}\quad \frac{d^2Q_i}{dx^2} = \frac{dQ_i}{dV_S}\frac{d^2V_S}{dx^2} + \frac{d^2Q_i}{dV_S{}^2}\left(\frac{dV_S}{dx}\right)^2, \tag{18}$$

giving

$$\frac{d^2V_S}{dx^2}\left(\frac{dV_S}{dx}\right)^{-2} = -\left(\frac{dQ_i}{dV_S} - \frac{kT}{q}\frac{d^2Q_i}{dV_S{}^2}\right)\left(Q_i - \frac{kT}{q}\frac{dQ_i}{dV_S}\right)^{-1}. \tag{19}$$

Equation (17), and hence Eq. (19), establish the condition necessary to attain electric current continuity in the source-drain channel of an IGFET. By direct substitution, it is easily shown that Eq. (4) is incapable, in its present form, of satisfying this requirement of continuity. The present discussion is directed toward the development of new one-dimensional equations for IGFET operation, based upon an assumption that the substrate doping, N_D in Eq. (4), is not invariant but, instead, attains the effective value necessary to achieve electric current continuity.

It has been shown that the inversion charge Q_i in an IGFET is not necessarily related to the surface voltage V_S through an elementary one-dimensional relation. Throughout the present analysis it is assumed that the two-dimensional mechanisms associated with IGFET operation provide a means whereby electric current continuity can be attained in the source-drain channel of an IGFET. Briefly, this interaction mechanism provides the degrees of freedom necessary for $Q_i(x)$ and $V_S(x)$ in Eq. (17) to attain the one-dimensional spatial distributions required to satisfy this equation at all locations between the source and drain.

From a mathematical point of view, the foregoing implies the separability of Eq. (19),

$$\text{a)}\quad \frac{d^2V_S}{dx^2} - \lambda(E_G)\left(\frac{dV_S}{dx}\right)^2 = 0;$$

$$\text{b)}\quad \frac{d^2Q_i}{dV_S{}^2} + \left[\lambda(E_G) - \frac{q}{kT}\right]\frac{dQ_i}{dV_S} - \frac{q}{kT}\lambda(E_G)\,Q_i = 0, \tag{20}$$

where $\lambda(E_G)$ is a parameter of separation.

In Eq. (20), the separation parameter $\lambda(E_G)$ depends upon the gate-induced electric field. If this gate field could be maintained constant between the source and drain, the only constraint upon the solution equations for Eq. (20a) and (20b) $[V_S(x), Q_i(V_S)]$ is the previously stated requirement for electric current continuity. In this situation the separation parameter would be constant between the source and drain junctions. If, instead, the gate-induced electric field is a spatial variable, the inversion charge distribution (and, hence, the voltage distribution) is modified by this gate field distribution. Therefore, the solutions for Eqs. (20a) and (20b) that are applicable to a typical IGFET structure are subject to the constraint imposed by a variable gate-induced electric field in addition to the constraint imposed by the requirement of electric current continuity; in this situation the separation parameter is a variable. The solution equations applicable to this device are as follows [9]:

$$\text{a)}\quad Q_i = Q_{i_0}\exp\left(\frac{q}{kT}V_s\right)\left\{\exp\left(-\frac{q}{kT}V_0\right) - \left(\frac{q}{kT} - \frac{1}{Q_{i_0}}\frac{dQ_{i_0}}{dV_S}\right)\int_{V_0}^{V_S}\exp\left[-\frac{qU}{kT} + \Omega(U)\right]dU\right\};$$

$$\text{b)}\quad E_0\,(x - x_0) = \int_{V_0}^{V_S}\exp\left[-\Omega(U)\right]dU, \tag{21}$$

where

$$\Omega(U) = -W_i\int_{U_0}^{U}\lambda(E_G)\,dE_G. \tag{22}$$

For the IGFET structure considered in this mathematical investigation it is necessary to establish the separation parameter $\lambda(E_G)$ in Eq. (20). From Eq. (20b), the magnitude of this parameter is given by

$$\lambda(E_G) = \left(\frac{1}{Q_i}\frac{dQ_i}{dV_S}\right)\left[1 - \frac{kT}{q}\frac{d^2Q_i}{dV_S^2}\left(\frac{dQ_i}{dV_S}\right)^{-1}\right]$$

$$\left(1 - \frac{kT}{q}\frac{1}{Q_i}\frac{dQ_i}{dV_S}\right)^{-1}. \qquad (23)$$

A manipulation of Eq. (23), in combination with Eq. (16), shows this expression can be rewritten into the form

$$\lambda(E_G) = \frac{q}{kT}\frac{I_{diff}}{I_D}\left[1 - \frac{kT}{q}\frac{d}{dV_S}\left(\log\frac{dQ_i}{dV_S}\right)\right], \qquad (24)$$

where I_{diff} is the diffusion component of the total drain current I_D.

A modified theory for IGFET operation

From Eq. (4), a well defined pinch-off of the inversion layer should exist at $V_S \approx 3.0V$, although the two-dimensional computer calculation shows little evidence of pinch-off at this location (see Fig. 2). It is proposed that the two-dimensional mechanisms suggested here provide a means whereby the inversion charge distribution in an IGFET becomes essentially independent of the surface voltage V_S; as a consequence, channel pinch-off cannot take place. Throughout the pinch-off region, as defined by traditional one-dimensional theory, the necessity of maintaining electric current continuity between source and drain is presumed to establish the computer-calculated inversion charge distribution.

Despite the absence of channel pinch-off in IGFET operation, the source-drain distance L can differ from the channel length L_C. If the applied gate biasing voltage exceeds the drain voltage, Fig. 4(a), the gate-induced electric field has the same direction at all locations between the source and drain junctions. If, instead, the applied drain voltage exceeds the gate voltage, Fig. 4(b), at some location along the semiconductor surface $V_S = V_G$ and, hence, the gate-induced electric field becomes zero. Between the source junction and this zero-field location the gate-induced electric field produces an inversion layer along the semiconductor-insulator interface. In contrast, between the drain junction and this zero-field location the gate-induced electric field forces carriers away from the semiconductor surface. Therefore, throughout the present investigation this zero-field location is considered to be the point of channel termination in an IGFET.

Channel termination in an IGFET must occur within the drain junction depletion layer. At this location the gate-induced electric field is zero and, therefore, no electrostatic charges are associated with the gate electrode. Furthermore, the voltage distribution between this channel termination point and the drain junction is adequately approximated by conventional p-n junction theory (for the particular device under consideration);

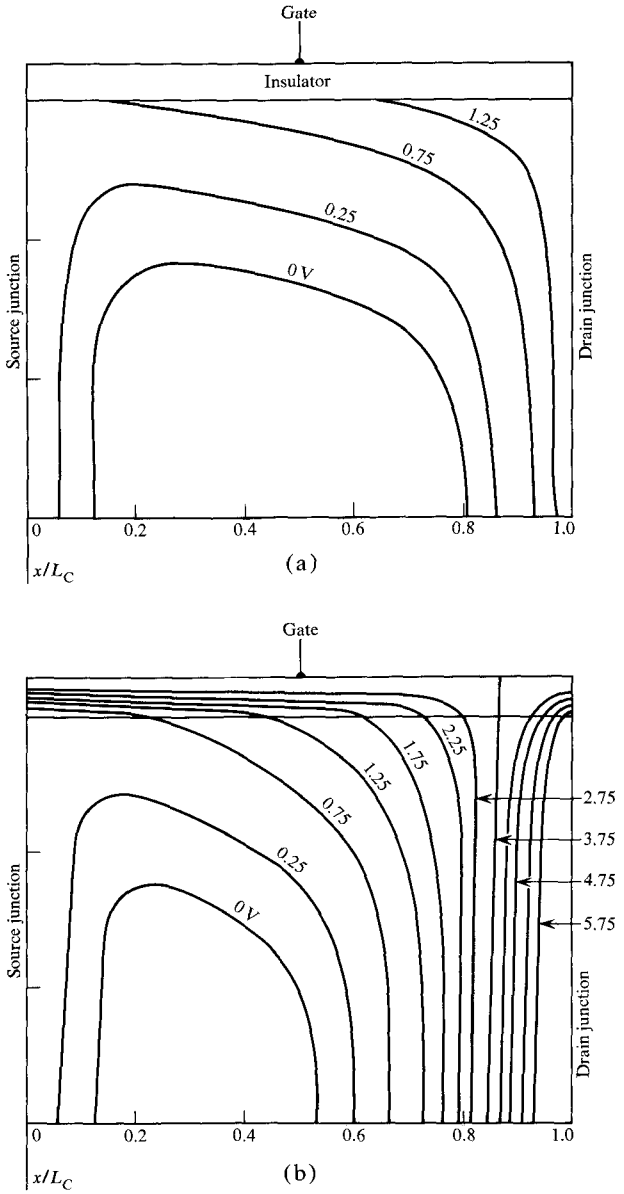


Figure 4 Computer calculated potential distribution in an IGFET for $V_G = 3.75$ V and $V_D =$ (a) 1.75 V and (b) 6.75 V.

this situation arises from a relative absence of mobile carriers along the semiconductor surface. Throughout this region of the structure the gate-induced electric field forces mobile carriers away from the semiconductor surface and, therefore, the drain junction space-charge layer is attributable almost entirely to ionized impurity atoms. The relative absence of mobile carriers between this channel termination point and the drain junction is illustrated by a two-dimensional calculation of the electric flux distribution in an IGFET (Fig. 5).

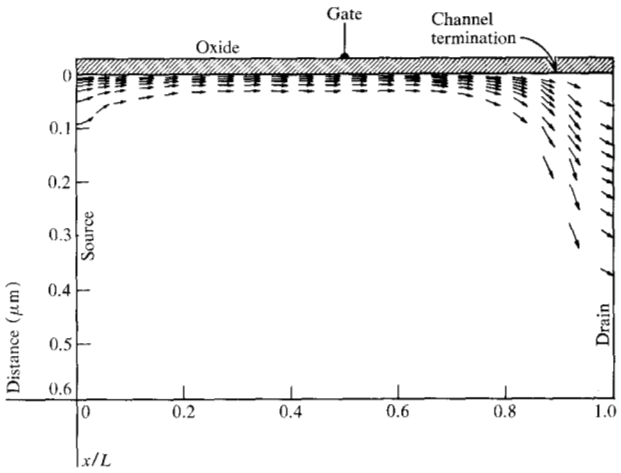


Figure 5 Calculated electric current distribution in an IGFET for constant carrier mobility, $V_{SG} = 3.0$V and $V_{SD} = 6.0$V.

In an IGFET the gate-induced electric field decreases with an increase in distance from the source junction. This change of electric field produces a similar change of inversion charge density and, therefore, the separation parameter $\lambda(E_G)$ in Eq. (20) cannot be considered a constant. One consequence of this situation is that neither the diffusion nor the drift component of source-drain electric current maintains continuity, although the total current I_D exhibits continuity everywhere within the structure.

From Fig. 2 and Fig. 3(a), the two-dimensional mechanisms described here are least effective in the vicinity of the source junction. Therefore, in this region of the structure it is presumed that Eq. (4) provides a satisfactory approximation for the inversion charge distribution and, hence, a means to establish the separation parameter $\lambda(E_G)$ in Eq. (22). By taking the first two terms of a Taylor series expansion for Eq. (23) near the source junction, and thereafter substituting Eq. 4 into this expansion, $\lambda(E_G)$ can be approximated by

$$\lambda(E_G) = \frac{\lambda_0}{1 - A(V_S - V_0)} \tag{25}$$

where

$$\lambda_0 = \frac{(\kappa_i\epsilon_0/W_i) + (1/2)\ (2\kappa_s\epsilon_0 q N_D/V_0)^{\frac{1}{2}}}{(\kappa_i\epsilon_0/W_i)\ (V_G - V_0) - (2\kappa_s\epsilon_0 q N_D V_0)^{\frac{1}{2}}}. \tag{26}$$

A more general equation for λ_0 is obtained through a solution for Poisson's equation for the potential distribution between the semiconductor surface and the charge neutral regions of the IGFET [10]. This solution shows that a decrease in V_G to a value below threshold produces a rapid increase in λ_0, and that λ_0 attains a limiting magnitude of q/kT for conditions of weak inversion. For this reason, it is presumed that $\lambda(E_G)$ approaches this same limit near the channel termination point of an IGFET (where $V_S = V_G$) and, therefore,

$$A = (1 - kT\lambda_0/q)\ (V_G - V_0)^{-1}. \tag{27}$$

After substituting Eq. (25) into Eqs. (21a) and (21b) we obtain*

$$\text{a)} \qquad Q_i \approx Q_{i0}\ [1 - A(V_S - V_0)]^{\frac{\lambda_0}{A}};$$

$$\text{b)} \qquad V_S = V_0 + \frac{1}{A}\left\{1 - [1 - (\lambda_0 + A)\ E_0 x]^{\frac{A}{\lambda_0 + A}}\right\}. \tag{28}$$

The drain current in this device can be specified in terms of physical parameters near the source junction:

$$\frac{I_D}{W} = \mu Q_{i0}\left[E - \frac{kT}{q}\left(\frac{1}{Q_i}\frac{dQ_i}{dx}\right)\right]_{x=0}. \tag{29}$$

From Eq. (28b) we have

$$E_0 = \frac{1}{(\lambda_0 + A)L_l}\left\{1 - [1 - A(V_D - V_0)]^{\frac{\lambda_0 + A}{A}}\right\} \tag{30}$$

and, therefore,

$$\frac{I_D}{W} = \frac{\mu Q_{i0}}{(\lambda_0 + A)L_l}\left(1 + \frac{kT}{q}\lambda_0\right) \times \left\{1 - [1 - A(V_D - V_0)]^{\frac{\lambda_0 + A}{A}}\right\}. \tag{31}$$

Equation (31) can be shown to be in satisfactory agreement with the computer calculated properties of an IGFET throughout the triode region of its volt-ampere characteristic.

It is interesting to note from Eq. (31) that under conditions of weak inversion, the transition into electric current saturation becomes exponential,

$$\frac{I_D}{W} = \frac{\mu Q_{i0}}{L_l}\left(\frac{1}{\lambda_0} + \frac{kT}{q}\right)\{1 - \exp\ [-\lambda_0(V_D - V_0)]\}. \tag{32}$$

This conclusion is consistent with recent publications [11, 12] describing weak inversion in an IGFET. A rigorous evaluation of Eq. (32) shows that this expression provides only a qualitative evaluation of I_D vs V_D under conditions of weak inversion. Although I_D does indeed exhibit the predicted exponential behavior, its magnitude in saturation, as given by Eq. (32), is excessive. This situation is known to arise from two-dimensional mechanisms not considered in the present investigation.

*An exact solution for $Q_i(V_S)$ is given by

$$Q_i = Q_{i0}\left\{1 - \left(1 + \frac{kT}{q}\lambda_0\right)Z_0^{\frac{A0}{A}} \times \exp\ (Z_0)\left[\Gamma\left(1 + \frac{\lambda_0}{A}; Z_0\right) - \Gamma\left(1 + \frac{\lambda_0}{A}; Z\right)\right]\right\},$$

where $Z = \frac{q}{kT}\left(V_S - V_0 - \frac{1}{A}\right)$; $Z_0 = -\left(\frac{q}{kT}\right)\frac{1}{A}$.

A comparison between Eq. (31) and the two-dimensional computer calculations shows a slight difference between the physical source-to-drain-junction distance L in an IGFET and the effective distance L_l. The two-dimensional computer calculations indicate that this situation results from mechanisms encountered between inversion layer charge carriers and the space-charge regions of the source and drain junctions. For the mathematical models used in this investigation it was found necessary to introduce into Eq. (31) an effective channel length L_l that is 4.0% less than the source-to-drain-junction distance ($L = 10.0$ μm; $L_l = 9.6$ μm). The mechanisms producing this slight reduction of channel length are not fully understood at the present time.

As previously stated, if in IGFET operation the applied drain voltage V_D exceeds the applied gate voltage V_G, at some location between the source and drain the gate-induced electric field becomes zero. At this location the surface inversion layer is terminated, and the channel length L_C becomes less than the effective source-to-drain-junction distance L_l. Furthermore, the total voltage applied across this modified length is $(V_G - V_0)$; thus, Eq. (32) has the form

$$\frac{I_D}{W} = \frac{\mu Q_{i_0}}{(\lambda_0 + A)L_C}\left\{1 - [1 - A(V_G - V_0)]^{\frac{\lambda_0 + A}{A}}\right\}, \qquad (33)$$

where

$$L_C = L_l - \left\{W - \left[W^2 - \frac{2\kappa_s\epsilon_0}{qN_D}(V_D - V_G)\right]^{\frac{1}{2}}\right\} \qquad (34)$$

and

$$W^2 = \frac{2\kappa_s\epsilon_0}{qN_D}V_D. \qquad (35)$$

Equations (34) and (35) are based upon an assumption that the drain junction is an abrupt asymmetrical type of structure [7].

Figure 6 presents a comparison between the computer calculated distribution of surface voltage $V_S(x)$ and Eq. (28b). Satisfactory agreement is obtained between these two calculations except in the immediate vicinity of the source and drain junctions (regions not shown in Fig. 6) where $0 < x/L < 0.1$ and $0.9 < x/L < 1.0$. Near these junctions this voltage distribution becomes modified by previously mentioned channel termination mechanisms: source and drain junction space-charge layer interaction with the inversion layer.

Figure 7 presents a comparison between the computer calculated volt-ampere characteristics for this device and similar calculations using Eq. (31) (when $V_D < V_G$) and Eq. (33) (when $V_G < V_D$). This comparison shows that satisfactory agreement exists between a rigorous two-dimensional computer calculation of these electrical characteristics and the approximation methods proposed here. Similar comparisons have been repeated throughout a range of assumed values of substrate doping; these comparisons show an agreement similar to that indicated by Figs. 6 and 7.

Comparisons have also been made between the equations presented here and two-dimensional computer calculations throughout a range of assumed source-drain junction distances. These comparisons show satisfactory agreement for structures containing a long source-drain

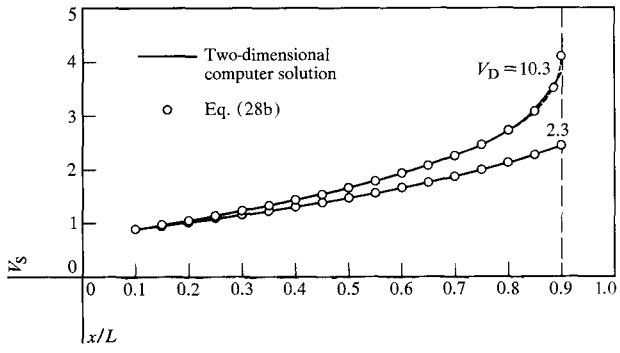
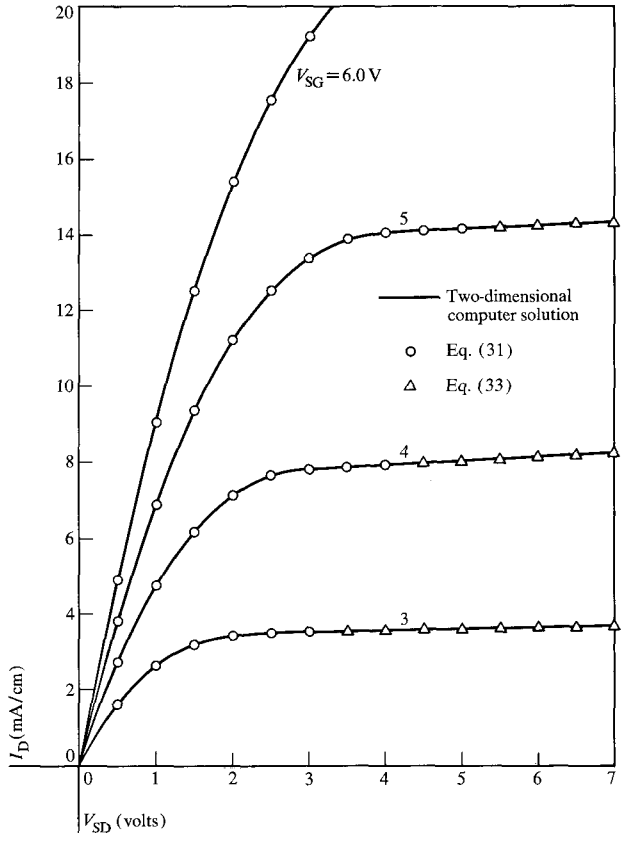


Figure 6 Calculated distribution of V_S for $V_G = 4.3$ V.

Figure 7 Calculated volt-ampere characteristics for an IGFET.



channel (10.0 μm $\leq L$). In contrast, similar comparisons for an assumed channel length of 5.0 μm clearly indicate the presence of mechanisms not considered in this analysis; "short-channel" mechanisms of IGFET operation represent a topic for further investigation.

Summary

Conventional theory of IGFET operation is based upon an assumption that the mobile carrier distribution in an inversion layer (between the source and drain) can be mathematically described by a one-dimensional application of Gauss' law. Resulting from this assumption is the concept of channel pinch-off and the association of this pinch-off mechanism with electric current saturation. Rigorous two-dimensional computer calculations, however, do not confirm these conventional concepts of IGFET operation. Instead, these computer calculations show that conventional one-dimensional IGFET theory represents a satisfactory approximation only in the vicinity of the source junction. Further, they show the presence of two-dimensional mechanisms that significantly influence the inversion-layer charge distribution in an IGFET.

A modified one-dimensional theory for IGFET operation is proposed as a means to approximate the two-dimensional mechanisms encountered in this semiconductor device. In particular, this modified theory is based upon an assumption that both the mobile carrier and voltage distributions in an inversion layer (between source and drain) are established by the requirement of electric current continuity. From this assumption, theoretical equations have been derived for the volt-ampere characteristic of an IGFET that appear to be in satisfactory agreement with rigorous two-dimensional calculations for this semiconductor problem. In addition, these equations are in qualitative agreement with recent publications on the topic of electrical conduction in an IGFET operating under conditions of weak inversion.

Some insight has been gained into the problem of mathematically approximating the physical and electrical properties of a short-channel IGFET. The two-dimensional mechanisms described here become increasingly important with a decrease in source-drain distance. These mechanisms, in combination with complications arising from a field-dependent carrier mobility, indicate the necessity for additional investigation before an adequate theoretical treatment is available for short-channel IGFET operation.

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