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Analytical and Experimental Thermal Analysis of Multiple Heat Sources in Integrated Semiconductor Chips

Abstract: Because of the complexity and interconnection density of today's integrated circuit chips, experimental measurement of individual transistor or diode junction temperatures under typical powered conditions has become increasingly difficult. In order to provide meaningful thermal data, other approaches have had to be devised. In the work described by this paper, an analytical model has been used to determine the steady state junction temperature rise on an integrated circuit chip. The effect on junction temperature of heat source size, geometry, and number of adjacent heat sources has been studied. Experimental testing on specially prepared chips has verified the analytical results.

Introduction

Two of the major factors that must be considered in any functional circuit design are power dissipation and subsequent heat removal. Heat generation occurs at all levels of packaging, ranging from the basic transistor, diode or resistor to the complete system. Therefore, to maintain critical component temperatures below specified limits for reliability and component life, and to insure the desired electrical characteristics in temperature-sensitive components, both power and thermal requirements must be considered.

The degree of integration reached with the advent of monolithic memories has clearly shown the importance of knowing the thermal characteristics of highly integrated chips. Heat dissipating components are at least one order of magnitude smaller than the devices in the Solid Logic Technology (SLT) family [1]. Although the piece of silicon into which the active devices are diffused is roughly 16 times larger than the basic SLT chip, there can be as many as 1400 components within it. Thermal evaluation of such components is further hampered because, unlike single-component SLT chips, complete circuits are interconnected on a single chip and no individual component can be contacted from outside the package. Thus, medium and large scale integration brings about basic changes in the thermal characteristics of a system that make it much more difficult, if not impossible, to actually measure the temperature rise of a component.

The purpose of the work described in this paper was to provide meaningful thermal data for devices at current levels of integration. The study was undertaken to provide both analytical and experimental evaluation for components of various sizes and geometries whose location is very close to other, similar components on the same chip.

Experimental evaluation

Special semiconductor chips were constructed for this investigation. Each chip had eleven active components which could be contacted separately for electrical and thermal testing. Among the eleven components, there were eight different device geometries. Individual devices, some of which are shown in Fig 1, had from two to twelve emitter stripes in a range of stripe widths between 0.0002 and 0.00075 inch. In addition, there were devices that had similar emitter geometries but different spacings between stripes. The ratio L_E/W_E of individual emitter length to emitter width, the ratio W_S/W_E of spacing between emitter stripes to emitter width, and the individual emitter area A_E are noted in Table 1 for each device in the Figure.

For testing purposes, the chips were gold eutectic bonded to gold plated copper studs mounted on specially prepared headers. The copper studs extended through the bases of the headers. To test one or more individual devices, flying leads were attached to those terminals of

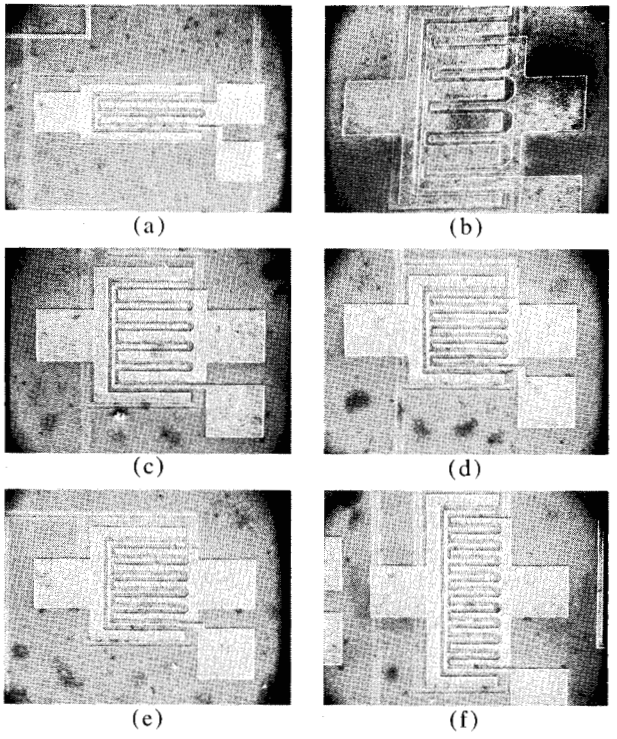

Figure 1 Examples of individual devices on the test chip. The number of emitter stripes is (a) 2; (b)-(e) 5; (f) 10. Other dimensions are given in Table 1.

Table 1 Dimensions of experimental devices shown in Fig. 1.

Device	*Number of emitter stripes*	A_E $(in^2 \times 10^{-6})$	L_E/W_E	W_S/W_E
(a)	2	2.5	12.9	1.14
(b)	5	2.5	12.5	3.6
(c)	5	4.0	6.25	1.0
(d)	5	2.0	12.5	2.0
(e)	5	2.5	10.0	1.6
(f)	10	1.28	8.0	2.0

Table 2 Comparison of experimental and analytical results based on $P_J = 0.2$ W.

Device	*Experimental* $\Delta T_{av}(°C)$	*Analytical* ΔT_{av} *(°C)*	*Difference: Analytical vs Experimental (percent)*
(a)	8.1	8.0	1.3
(b)	6.9	6.8	1.5
(c)	6.8	6.1	10.3
(d)	8.2	8.7	6.1
(e)	8.3	8.1	2.4
(f)	6.0	6.5	8.3

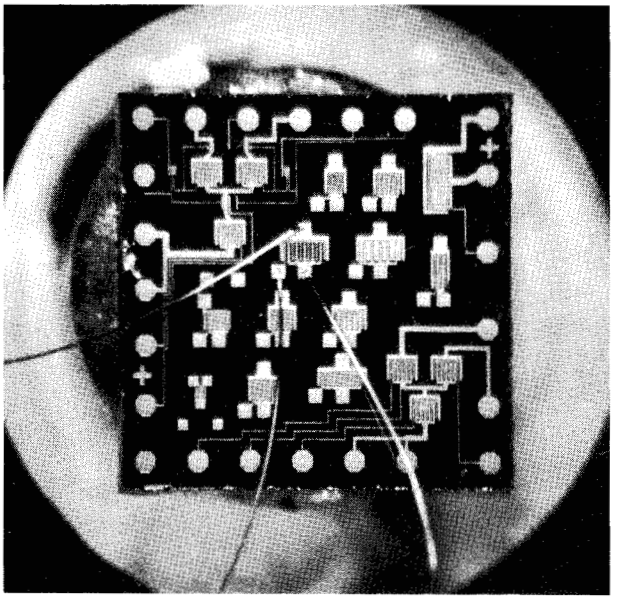

Figure 2 Test chip with flying leads, mounted on the copper stud header.

the header that were connected to the selected devices before the headers were sealed. Figure 2 shows a test chip mounted on the copper stud with flying leads attached. Through use of the copper-stud headers and a pulsed collector test technique described by Schlig[2], it was possible to measure the thermal resistance from the junction of a device to the back of the header. Since the thermal resistance of copper is very low, this measurement could be used as the thermal resistance from the device junction to the back of the chip. Therefore, given this thermal resistance and the power dissipated during the test, it was possible to calculate the average stripe temperature rise of the heat generating device for the ambient test conditions. Thus:

$$R_{T_{J\text{-}C}} = (T_J - T_C)/P_J, \text{ or}$$

$$\Delta T_{J\text{-}C} = P_J R_{T_{J\text{-}C}}, \quad (1)$$

where T_J is junction temperature in °C, T_C is the temperature of the back of the chip in °C, P_J is device power in watts, and $R_{T_{J\text{-}C}}$ is the thermal resistance between the junction and the chip back in °C/W.

Analytical model

Ever-increasing chip complexity and miniaturization have made experimental testing difficult and tedious. Even when testing is possible, only a relatively few selected device geometries and configurations can be investigated. As a result, the need for an analytical model becomes increasingly important in predicting thermal performance for a device of any size.

The mathematical investigation of integrated circuits suggests that a chip be divided into small volumes, or nodes, where the regions of greatest concern contain many small nodes compared with other regions on the chip. By assuming that each volume has homogeneous properties [3], a conduction heat balance can be performed for each node. The three-dimensional Poisson equation, given below, expresses this basic heat transfer relationship, where each node must be classified as to whether heat is generated internally ($Q_I = Q$) or not ($Q_I = 0$):

$$\left[KA\left(\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}\right)\right]_{in} - \left[KA\left(\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}\right)\right]_{out} + Q_I = 0, \quad (2)$$

where K is the thermal conductivity of the material, A is the effective heat transfer area, T is temperature, and Q_I is the amount of internal heat generation.

Figure 3 shows a typical nodal breakdown for a chip of nominal size. It is important to note the very small thickness of the heat source as well as the fine breakdown along its perimeter. Both the volume and the surface area of the heat source must be well defined in order to accurately determine the effective heat transfer area A for each plane of the heat source nodes.

Also essential to the analytical model is the selection of the proper value of thermal conductivity K for each node. In this study, $K = 1.21$ W/cm°C was used for the entire silicon chip except for the emitter or heat source areas. Due to the impurity concentration of the emitter areas, Slack[4] suggests that $K = 0.1$ W/cm°C be used.

Additional boundary conditions necessary to describe the analytical model can be summarized as:

1) An adiabatic surface on all four of the chip edges and along the $Z = 0$ plane except for the heat source areas:

$$\dot{Q} = -KA\frac{\partial T}{\partial n} = 0;$$

2) an isothermal surface (constant temperature) across the bottom of the chip;

3) a maximum power dissipation of 0.040 W/mil^2. At high currents the model may have to be modified to include the effects of current crowding and Joule heating in the collector.

Results

The comparison between experimental and analytical results given in Table 2 indicates agreement of approximately 10 % or better for the six device configurations shown in Fig. 1.

Additional study of the experimental and analytical results has revealed that individual heat source area, A_E, ratio of the emitter length to the emitter width, L_E/W_E, and ratio of the space width between emitters to the emitter width, W_S/W_E, are the parameters that have the most influence on $R_{T_{J\text{-}C}}$ and $\Delta T_{J\text{-}C}$. For example, the temperature rise of a device with a small heat source area can be compensated by increasing L_E/W_E and W_S/W_E. Results also indicate that the $R_{T_{J\text{-}C}}$ of an individual stripe is independent of the number of heat source stripes while $\Delta T_{J\text{-}C}$ is inversely proportional to the number of stripes for constant device power on multistripe devices.

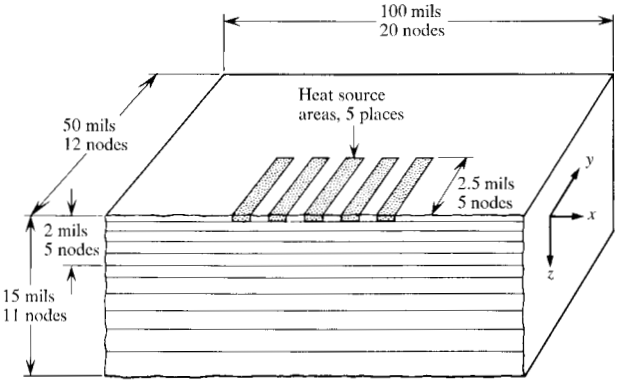

Figure 3 Cross-section of a chip showing typical dimensions and nodal breakdown.

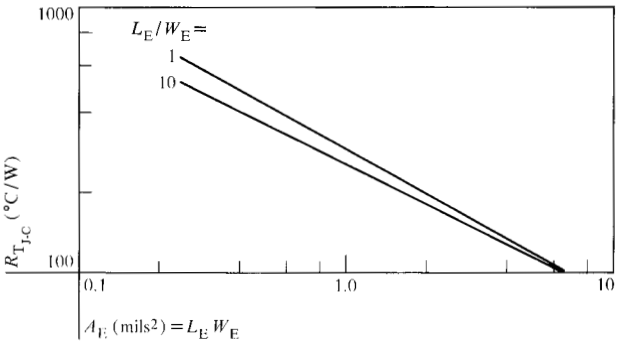

Figure 4 $R_{T_{J\text{-}C}}$ for $W_S/W_E = 5.0$ with L_E/W_E values of 1.0 and 10.0.

Generalized curves to predict $R_{T_{J\text{-}C}}$ for multiple heat source chips can be obtained as functions of A_E, L_E/W_E, and W_S/W_E by applying these basic principles. Figure 4 shows two such curves as a function of A_E for two values of L_E/W_E when $W_S/W_E = 5.0$. For configurations with $W_S/W_E < 5.0$, Table 3 shows the necessary correction factor which must be added to the value of $R_{T_{J\text{-}C}}$ at $W_S/W_E = 5.0$. For values of $W_S/W_E > 5.0$, there is only a slight decrease in $R_{T_{J\text{-}C}}$. Since Fig. 4 and Table 3 can be applied to devices with multistripe heat sources, conservative values of $R_{T_{J\text{-}C}}$ should be expected for devices

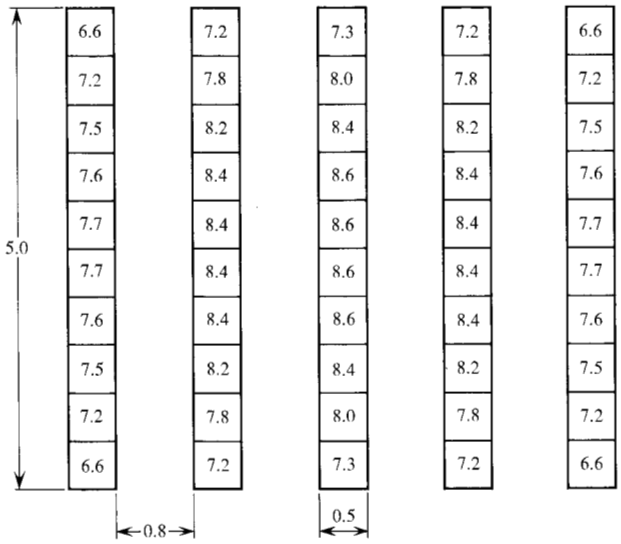

Figure 5 Typical heat source pattern giving $\Delta T_{J\text{-}C}$ in °C and dimensions in mils for a device power of 0.2 W.

Table 3 Increase in R_T for $W_S/W_E < 5.0$ for any given A_E.

W_S/W_E	*Increase in $R_{T_{J\text{-}C}}$ (percent)* $L_E/W_E = 1.0$	*10*
0	80	105
0.4	50	75
1.0	30	50
2.0	17	25
3.0	9	13

with less than three heat sources. For example, the value for a five-stripe heat source with $A_E = 1.0$, $L_E/W_E = 10$ and $W_S/W_E = 1.0$ can be calculated from the generalized curves. From Fig. 4, $R_{T_{J\text{-}C}}$ is 268 °C/W and from Table 2 for $W_S/W_E = 1.0$ the increase in $R_{T_{J\text{-}C}}$ is 50 percent. Therefore,

$$R_{T_{J\text{-}C}}\ (W_S/W_E = 1.0) = 268 + 0.5(268) = 402\ °C/W$$

for this example.

The choice between experimental measurement of special devices and analytical characterization by means of the model depends very much upon how the results will be applied. The experimental approach is more accurate at present and is necessary in order to adjust the analytical model. On the other hand, the model can be used to predict results even when hardware is not available for testing, or when the comparison of many device configurations is necessary. The analytical model also locates the position and the magnitude of the maximum $\Delta T_{J\text{-}C}$ as well as the average value, while the experimental approach gives only an average $\Delta T_{J\text{-}C}$. Figure 5 shows the temperature gradient obtained along the heat sources of the device in Fig. 1(e) using the analytical model.

Conclusions

The results from the experimental testing indicate close agreement with the results obtained from an analytical model for which the location, shape, size and thermal conductivity of the heat source areas were the essential variables.

Figure 4 and Table 3 allow the calculation of average $R_{T_{J\text{-}C}}$ and $\Delta T_{J\text{-}C}$ values for any device with three or more heat sources where A_E and the ratios L_E/W_E and W_S/W_E describe the size and spacing of the heat sources.

Acknowledgments

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References and footnotes

1. E. M. Davis, W. E. Harding, R. S. Schwartz and J. J. Corning, *IBM J. Res. Develop.* **8,** 102 (1964).
2. E. S. Schlig, "The Measurement of Transient Junction Temperature in Very Small Bipolar Transistors," *Research Report RC 2679*, IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598.
3. It is acknowledged that any particular chip may show structural irregularities due to intrinsic defects, impurities, etc., and that the resulting variation in physical properties (for example, isolated regions of different thermal conductivity) will be manifest as experimental deviations, usually small and randomly located, from the calculated temperature profile. This does not affect the utility of our assumption for the general case, however, and the model as applied to a specific device can be readily modified to account for any such irregularity whose location is known. For design purposes that much precision is seldom necessary, since it must be assumed that the given device material and fabrication process will have already been selected to minimize the likelihood of irregularities.
4. G. A. Slack, *J. Appl. Phys.* **35,** 3460 (1964).

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