

V. J. Silvestri
T. B. Light
H. N. Yu
A. Reisman

Ge Epitaxial Refill Deposition Techniques for Fabricating Pedestal Transistor Structures

Abstract: An etch-epitaxial refill technique is described for the fabrication of integrated high-speed Ge transistor structures having a pedestal configuration. The device areas surrounding 0.1 ohm-cm mesa structures were refilled with Ge having a resistivity range of 1 to 10 ohm-cm, providing low parasitic capacitance in the passive area of the base-collector junction. Processes and techniques were developed for minimizing the ridge that tends to form at the edge of the deposited SiO_2 mask. Electrical properties and junction characteristics of the epitaxial regions are discussed and some device results presented.

Introduction

The selective deposition of semiconductors through masks has interested a number of investigators. Most of the work previously reported was done in Si vapor deposition systems using SiO_2 as a mask [1-5]. The interest in these techniques has been to create novel device structures or integrated arrays of such structures. The general approach has been to refill holes created in an oxide mask where generally the oxide-to-Si surface area ratio was large. This approach has been for the most part unsuccessful because of two problems encountered in attempting to backfill holes, namely, 1) planar surfaces are not readily obtained and 2) control of the crystalline quality and electrical characteristics of the material is difficult. One experiences rather different effects in attempting to refill holes compared to those effects that have been established for the epitaxial growth of a film on an undisturbed surface. In the $\text{GeCl}_4\text{-H}_2$ system, for instance, one finds that for the conditions which yield film growth on an unmasked Ge surface, one obtains no growth and may even obtain etching in holes surrounded by an oxide mask. Our approach circumvents some of these problems by refilling on surfaces that more closely resemble an unmasked Ge surface, i.e., where the SiO_2 -to-Ge surface area ratio is small. The process also minimizes difficulties with respect to material quality and electrical characteristics, this being important because the refill material for this device application has a high resistivity and requires close doping control.

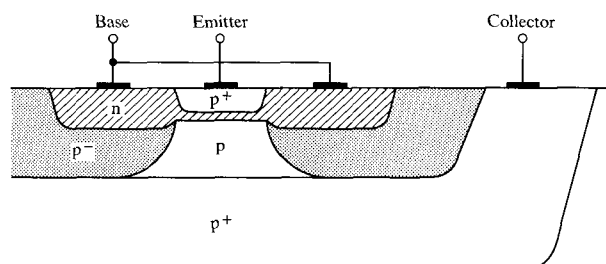


Figure 1 A low capacitance transistor structure.

Pedestal structure and fabrication

The object of this investigation was to produce low capacitance transistor structures by using a pedestal configuration (Fig. 1) [6], which is designed to enhance device performance in circuits in which the capacitive effect has an important role. The reduction of collector capacitance in this configuration is achieved through the reduction of parasitic capacitance in the passive area of the base-collector junction. Structurally, the transistor is made by providing a region of more highly doped material surrounded by a higher resistivity material in which a large portion of the base-collector junction is located. We were interested in fabricating 0.1 ohm-cm mesas surrounded by 1 to 10 ohm-cm Ge. To produce this configuration, the procedures depicted in Fig. 2 were followed.

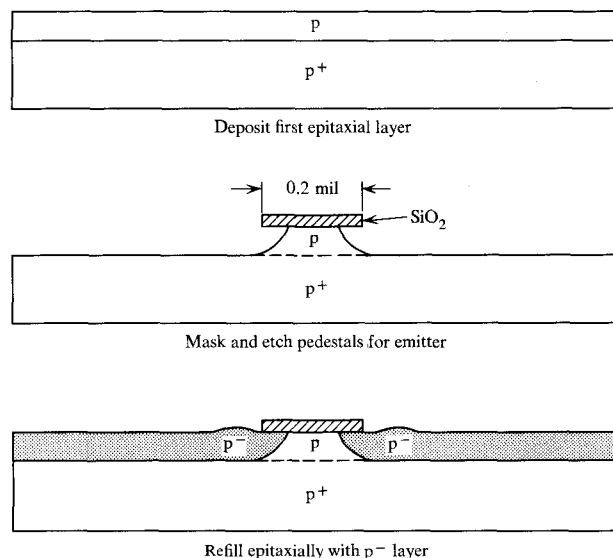
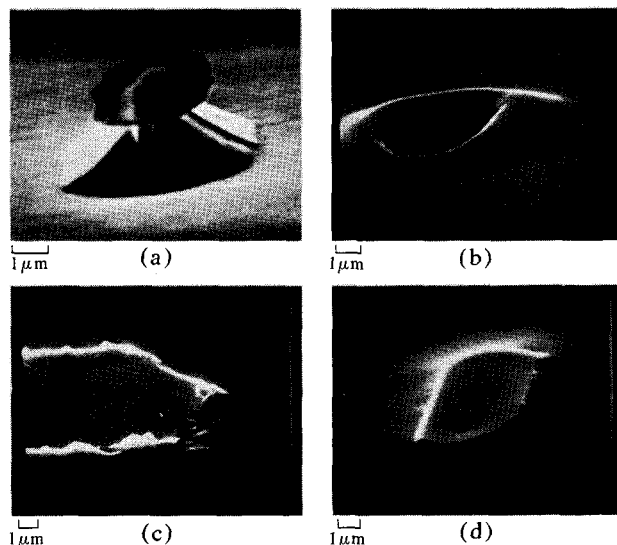


Figure 2 Epitaxial-etch-epitaxial refill method for fabricating pedestal structures.

Figure 3 Scanning electron microscope photographs: (a) mesa structure formed after etching, photograph taken at 80° from normal; (b) refilled structure showing ridge growth, at 80° from normal; (c) structure refilled using the GeH₄ process showing attached polycrystalline germanium surrounding mesas, at 70° from normal; (d) refilled structure with minimal ridge formation, at 75° from normal.



The surface of a 0.1 ohm-cm p-type epitaxial film 2 μm thick, which had been deposited on a p⁺ (0.0001 ohm-cm) Ge wafer (a collector contact), was first masked with a 2000-Å film of SiO₂. This film was deposited on the surface at 800°C by pyrolysis of tetraethyl orthosilicate. Through appropriate photoresist techniques, oxide stripes were then delineated on the surface of the substrate.

Next the exposed germanium surface surrounding the oxide areas was etched selectively, using an H₂O₂-H₂O solution, to a depth of 1 μm to produce 0.1 ohm-cm mesas. Each individual mesa after etching retained the oxide cover, which was undercut to approximately the depth of etching, thereby creating an overhanging oxide [Fig. 3(a)]. This oxide protects the mesa surface, destined to be used as the active device area, and reduces the extent of nonplanar growths.

The object is then to refill around these mesa structures with high resistivity Ge and thereby imbed the 0.1 ohm-cm pedestals in a high resistivity matrix. Prior to putting the substrates into a conventional vertical GeCl₄-H₂ reduction system[7], they were given a 3 to 4 second cleaning in a 3:1 H₂O:5%NaOCl solution and rinsed under flowing deionized water for five minutes. The refill depositions were initially made at temperatures ranging from 700 to 800°C at a Ge-to-H₂ concentration ratio of 3.6 × 10⁻⁴. Diborane gas mixed with H₂ was introduced into the reactor to obtain the 1 to 10 ohm-cm refill material.

Ridge growth

In attempting to refill around the pedestal structures in the reduction system, it was found that 1) Ge did not nucleate or deposit on the oxide and 2) there was a buildup of Ge on the Ge surface adjacent to the oxide, forming a "ridge" [Fig. 3(b)]. These effects have been noted by both Doo[8] and Sirtl[5] on partially masked substrates in the SiCl₄-H₂ system. The ridge height varied from 0.25 to 3 μm, depending on the experimental conditions. These nonplanar surfaces made further device processing steps impractical.

An analysis of the ridge structure[9] indicates that the ridge forms as a result of diffusion of a Ge-bearing species across the SiO₂ surface (where Ge does not nucleate). The low nucleation rate on the SiO₂ surface occurs over a wide range of growth conditions, including those that are considered "normal" operating conditions, i.e., conditions which provide reasonable growth rates (0.1 to 0.2 μm/min) and yield smooth surfaces.

A number of approaches were taken to minimize the ridge formation. In one, materials such as sputtered Ge, W, and Mo were deposited on the oxide to provide a better nucleation surface for Ge over the oxide stripe. This idea worked in principle, but could not be used successfully in practice.

Refill depositions were also carried out by decomposition of GeH₄[10] at 700°C. In this system, nucleation of Ge on the oxide occurs readily over a wide range of growth conditions. With the simultaneous nucleation of Ge on the oxide, enhanced growth of Ge at the exposed Ge surface adjacent to the oxide was reduced. The success of this process, however, depends on the removal

of the SiO_2 masking material along with any growth attached to it. The complete removal of the polycrystalline layer was unsuccessful, since a polycrystalline layer remained bound to the adjacent epitaxial layer. Figure 3(c) shows the nature of this bound material.

The approach used to refill via the $\text{GeCl}_4\text{-H}_2$ process involved control of the ridge growth through control of the process parameters, temperature and concentration. Systematic variation of temperature and concentration established that virtual elimination of the ridge formation could be accomplished for epitaxial growth conditions approaching that of the surface rate limited region. An example of reduction in ridge growth to less than $0.1\text{ }\mu\text{m}$ is shown in Fig. 3(d); the ridge height in Fig. 3(b) approaches $1\text{ }\mu\text{m}$.

Figure 4 shows the conditions of temperature and concentration under which ridgeless structures are obtained. (The growth kinetics which can be derived from this plot have been described previously[6].) The dashed curve essentially demarks mass transport limited growth (growth rate independent of substrate temperature, region B) from surface limited growth (growth rate dependent on substrate temperature, region A). The temperature-concentration combinations that were found to favor the elimination of the ridge lie close to this dashed line.

Mass transport limited growth conditions have been shown to be more desirable from the point of view of obtaining smooth surfaces. Ridgeless structures, on the other hand, are more highly favored in surface rate limited growth conditions. It was also observed that near the transition region the smoothness of the epitaxial layer obtained was very sensitive to the cleaning procedure used. We found that additional care in cleaning, along with an $\text{H}_2\text{O}_2\text{-H}_2\text{O}$ etch as a final cleaning step, resulted in device quality surfaces that were ridgeless.

Electrical properties and transistor characteristics

The resistivity of the refill material could be varied from 1 to 10 ohm-cm by using B_2H_6 as a dopant. A typical doping profile for a refill layer, obtained from differential capacitance measurements, is shown in Fig. 5. The two lower curves are for as-grown wafers, whereas the upper curve represents a sample which has been heat treated to simulate subsequent device fabrication steps.

Post-alloy-diffused transistors fabricated with this structure have had low collector capacitance, as anticipated. For a base-collector junction area of 0.72 mil^2 , the total collector capacitance was reduced by a factor of two compared to a conventional structure. Since the apparent reduction ratio of the collector junction depended upon the relative capacitances of the active and the passive portions of the collector junction, as well as on the parasitic contact pad capacitance, a reduction ratio of two would yield a resistivity of 1 to 2 ohm-cm for the refilled

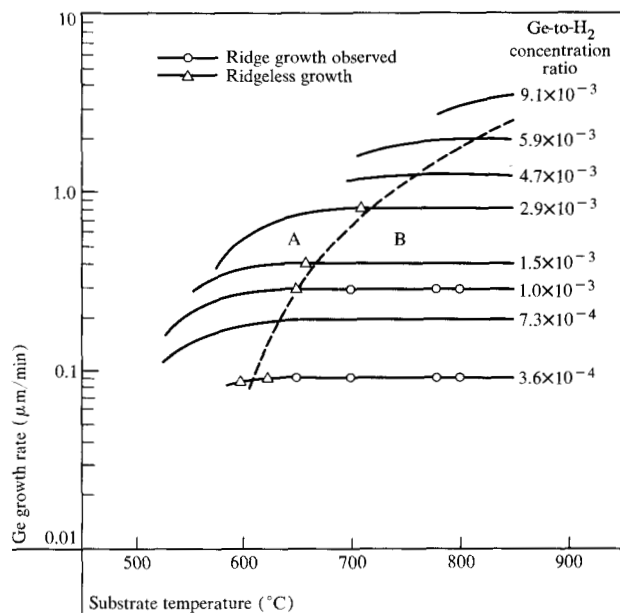
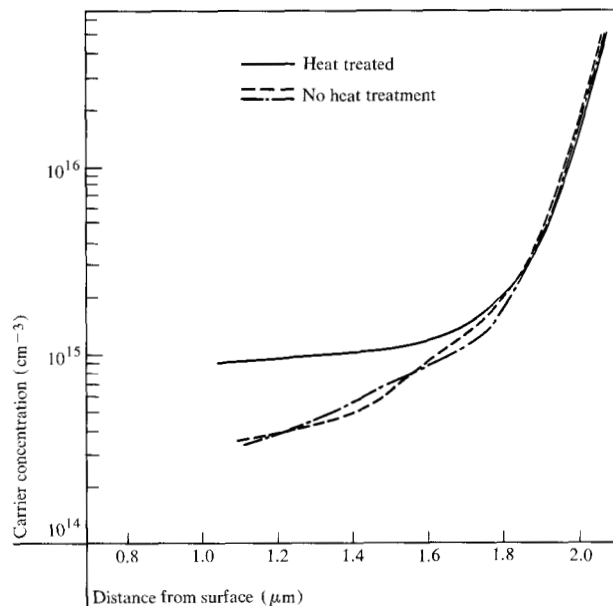


Figure 4 Temperature and concentration conditions for refill growth.

Figure 5 Carrier concentration profile for the epitaxial refill material.



region. Figure 6 shows a comparison of the collector capacitances of a conventional and a low capacitance transistor structure. For collector voltage biases of less than 0.5 V, anomalous collector capacitances due to surface inversion occur. The anomalous capacitance is not a characteristic parameter of the device, since it depends to a large extent on the surface characteristics surrounding the collector junction. The output $I-V$ charac-

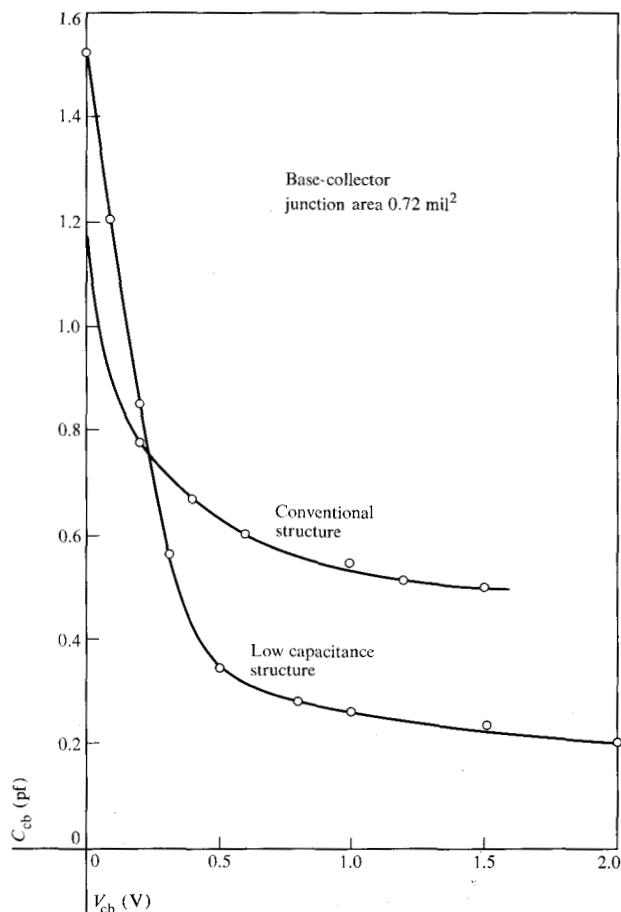


Figure 6 Comparison of collector capacitances.

teristics and the frequency response of such a device structure are shown in Figs. 7 and 8, respectively. These properties are, in general, similar to those of a conventional transistor.

Summary

This work has demonstrated that an etch-epitaxial refill technique can be used to fabricate high-speed germanium transistors in a pedestal configuration as an alternative to a diffusion-epitaxy process [11]. The problem of ridge formation resulting from the refill process was solved by choosing appropriate growth conditions.

Acknowledgments

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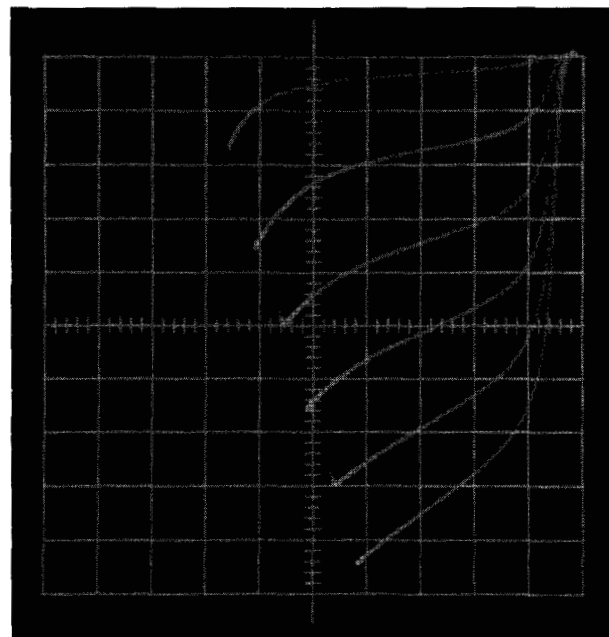
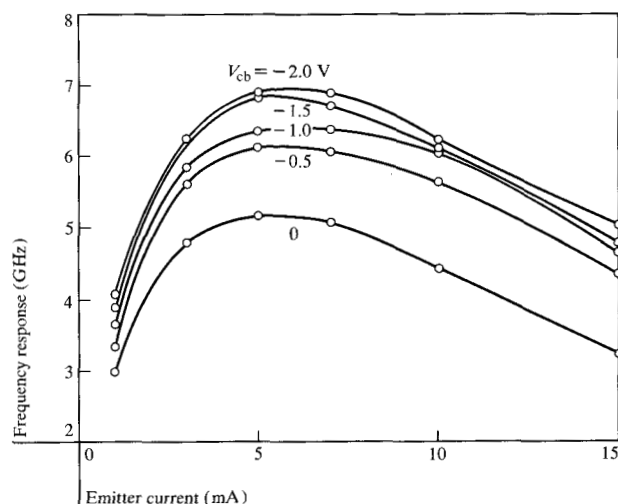


Figure 7 Output I - V characteristics of a low capacitance transistor structure. I , vertical scale, 1 mA/division; V , horizontal scale, 0.5 V/division; base current, 0.02 mA/step.

Figure 8 Frequency response for low capacitance transistor structure.



Cowher for electrical measurements, and O. C. Wells and C. G. Bremer for scanning electron microscope photographs.

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The authors are located at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598.